GUJARAT TECHNOLOGICAL UNIVERSITY

Program Name: Diploma Engineering
Level: Diploma
Branch: Electronics & Communication Engineering / Information & Communication Technology
Subject Code : DI05000021
Subject Name : VLSI System

w. e. f. Academic Year:	2026-27
Semester:	5th
Category of the Course:	PCC

Prerequisite:	Students should have basic knowledge of (1) Basic Electronics (Understanding of diodes, transistors and electronic components (2) Digital Electronics (Logic gates, Boolean algebra, Combinational and Sequential circuits (3) Semiconductor Physics (Basic concepts of semiconductor materials and PN junctions) (4) Basic Knowledge of Computer and Simulation tools.
Rationale:	Very-Large-Scale -Integration (VLSI) technology is widely used in modern electronics devices such as computers, mobile phones, and embedded systems. This course helps diploma students to understand the basic concepts of IC design, fabrication and CMOS technology. It also introduced hardware description languages like Verilog. The course develops the basic knowledge and practical skills required for working in the electronics and semiconductor industry.

Course Outcome:
After Completion of the Course, Student will able to:

No	Course Outcomes	RBT Level
01	Describe working of MOSFET.	R, U
02	Describe the operation of MOS Inverter with different load configurations.	U
03	Design of Combinational and Sequential circuits using MOSFET.	A
04	Describe fabrication process for MOS	U
05	Develop Verilog code for combinational and sequential design.	A

**Revised Bloom's Taxonomy (RBT)*

Teaching and Examination Scheme:

Teaching Scheme (in Hours)			Total Credits L+T+ (PR/2)	Assessment Pattern and Marks				Total Marks
				Theory		Tutorial / Practical		
L	T	PR	C	ESE (E)	PA(M)	PA(I)	ESE (V)	
3	0	2	4	70	30	20	30	150

Course Content:

Unit No.	Content	No. of Hours	% of Weightage
1.	**MOS TRANSISTOR** 1.1 Explain Energy band diagram and structure of MOS 1.2 MOS system under external bias 1.3 Symbols for different MOSFET 1.4 Structure and operation of MOSFET 1.5 Channel formation 1.6 Gradual channel Approximation 1.7 MOSFET Current-Voltage characteristics 1.8 Needs of scaling 1.9 Full-Voltage Scaling, Constant-Voltage Scaling. 1.10 Effect of Scaling 1.11Dual Gate MOSFET: Concept, Structure, Advantages and Limitations 1.12Silicon on Insulator(SOI): Concept, Structure, Advantages and Limitations 1.13 High-K metal gate MOSFET: Concept, Structure, Advantages and Limitations 1.14 FIN-FET: Concept, Structure, Advantages and Limitations 1.15 Gate All Around(GAA) FET: Concept, Structure, Advantages and Limitations	9	20
2.	**MOS INVERTERS** 2.1 Concept and working of Ideal Inverter 2.2 Noise Margin and Noise Immunity 2.3 Voltage Transfer Characteristic of Ideal Inverter 2.4 Working and VTC of Resistive Load Inverter (without derivation) 2.5 Working and VTC of Depletion load Inverter (without derivation) 2.6 Working and VTC of CMOS inverter (without derivation)	7	17

3.	**MOS CIRCUIT** 3.1 Two Input NAND and NOR Gate with depletion NMOS load 3.2 Combinational MOS logic circuits with Depletion nMOS Loads 3.3 Two input NAND and NOR Gate using CMOS logic. 3.4 AOI and OAI complex Logic circuits using CMOS 3.5 Simple XOR/XNOR function using CMOS logic 3.6 Complex logic circuits using CMOS logic 3.7 NOR gate based SR latch using CMOS logic 3.8 NAND gate based SR latch using CMOS logic 3.9 Clocked NOR based SR latch using CMOS logic 3.10Clocked NOR based JK latch using CMOS logic 3.11Clocked NOR based D latch using CMOS logic	11	25
4.	**FABRICATION OF MOSFET** 4.1 VLSI design flow representation using Y chart 4.2 Define terms: Hierarchy, Regularity, Modularity, Locality 4.3 FPGA: Architecture, Characteristics, Advantages, Application and Limitations 4.4 CMOS Fabrication using CMOS n- Well Process 4.5 Diffusion 4.6 Ion implantation 4.7 Oxidation 4.8 Photolithography 4.9 Etching 4.10Deposition	6	15

5.	**INTRODUCTION TO VERILOG** 5.1 Basic Features of Verilog HDL 5.2 Module Definition 5.3 Data types: wire, reg, constants 5.4 AND, OR, NOT, XOR, XNOR, NAND and NOR gate implementation using dataflow, structural and behavioural modelling in Verilog 5.5 Verilog code for Adder and Subtractor circuits : Half Adder, Full Adder, Half Subtractor, Full Subtractor, Full Adder using Half Adder, 4 bit full adder 5.6 Verilog Programs related to Combinational circuits: Multiplexer and Demultiplexer, Decoder and Encoder, Parity Generator and Parity Checker 5.7 Test bench: Structure, instantiation of design module in testbench, stimulus generation. 5.8 Use of initial, always and forever blocks in testbench for applying inputs. 5.9 Simple testbench example for Basic gates. 5.10 Verilog programs related to basic Sequential circuits : SR latch, D F/F, T F/F, JK F/F, Parallel Input Parallel Output Shift Register, 4- Bit Binary Up Counter/ Down counter	12	23
	Total	**45**	**100**

Suggested Specification Table with Marks (Theory):

Distribution of Theory Marks (in %)					
R Level	**U Level**	**A Level**	**N Level**	**E Level**	**C Level**
26	**31**	**43**	-	-	-

Where R: Remember; U: Understanding; A: Application, N: Analyze and E: Evaluate C: Create (as per Revised Bloom's Taxonomy)

References/Suggested Learning Resources:

(a) Books:

1. CMOS Digital Integrated Circuits by Sung Mo Kang, TMH Publication
2. VLSI Design by Deepak Garg Katson Pulishers
3. Introduction to VLSI Circuits and Systems by Uyemura J.P., Willey India Pvt. Ltd. Publication
4. VLSI Design by Das Debaprasad, OXFORD Publication
5. CMOS Circuit Design, Layout, and Simulation by Baker, Li, Boyce, Willey Publication

6. Verilog HDL : A Guide to Digital design and Synthesis by Samir Palnitkar, SunSoft Press
7. A Verilog HDL Primer by Bhasker J., BSP Professional books

(b) Open source software and website:

1. Icarus as compiler and GTKWave for waveform generator
2. QUARTUS-II-ALTERA EVAL VERSION
3. ModelSim® HDL simulator
4. ISE design suite
5. https://dldv-iiith.vlabs.ac.in/
6. https://fsp2-iiith.vlabs.ac.in/exp/mos-capacitance/simulation.html
7. https://www.edaplayground.com/
8. https://eda.sw.siemens.com/en-US/
9. https://nptel.ac.in/courses/117106092
10. https://nptel.ac.in/courses/103106075
11. nptel.ac.in/courses/108103179
12. nptel.ac.in/courses/106103358
13. https://archive.nptel.ac.in/courses/113/106/113106062/

Suggested Course Practical List:

Sr	Experiment	No of Hours
1	To develop the source code for all basic logic gates by using VERILOG Dataflow and Structural/Gate level style and obtain the simulation	**2**
2	To develop the source code for Universal Gates by using VERILOG Dataflow and Structural/Gate level style and obtain the simulation .	**2**
3	To develop the source code for XOR and XNOR Gates by using VERILOG Dataflow and Structural/Gate level style and obtain the simulation.	**2**
4	To develop the source code for Half adder and Full adder using Verilog Dataflow and Structural/Gate level style and obtain the simulation.	**2**
5	To develop the source code for Half Subtractor and Full Subtractor using Verilog Dataflow and Structural/Gate level style and obtain the simulation	**2**
6	To develop the source code for full adder using two half Adder using Verilog Structural/Gate level style and obtain the simulation	**2**
7	To develop the source code for four-bit parallel adder using Verilog Structural/Gate level style and obtain the simulation	**2**
8	To develop the source code for 4 x1 multiplexer using Verilog Dataflow, Structural/Gate level and Behavioural style and obtain the simulation.	**2**
9	To develop the source code for 1 x 4 de-mux using (1) if-else statement and (2) case statement in Behavioural Verilog Style and obtain the simulation.	**2**
10	To develop the source code for 3 : 8 decoder using Behavioural Verilog	**2**

	Style and obtain the simulation.	
11	To develop the source code for 8 : 3 encoder using (1) Dataflow (2) Structural/Gate level (3) Behavioural (4) With Enable Behavioural Verilog Style and obtain the simulation.	**2**
12	To develop the source code for (1) 3 bit Even Parity generator (2) 4 bit odd Parity Generator (3) 3 Bit Even Parity Checker and (4) 4 bit odd checker using Verilog Structural/Gate level style and obtain the simulation	**2**
13	To develop the source code for (1) D- flip-flop with reset (2) T flip flop (3) SR Flip Flop with reset (4) JK flip with negative reset using Verilog behavioural style and obtain the simulation.	**2**
14	To develop the source code for(1) 4 bit binary Up counter and (2) 4 bit Binary Down Counter using Verilog and obtain the simulation.	**2**
15	To develop the source code for 4 bit Parallel In Parallel Out shift register using Verilog and obtain the simulation	**2**
16	To Design and Simulate Testbench for 2:4 Decoder using Verilog	**2**
17	To Design and Simulate CMOS Inverter	**2**
18	To Design and Simulate (1) 2 input CMOS NAND gate and (2) 2 input CMOS NOR Gate	**2**
19	Synthesis, Place , Route and Implement any of the above Digital Circuit into FPGA.	**2**
	Total	**38 Min 30**

List of Laboratory/Learning Resources Required:

- Computer/laptop
- Verilog editor and simulator (ModelSim/Icarus Verilog/Xilink/Altera Max Plus 2 etc.)
- FPGA development board, USB Cable

Suggested Project List:

MICRO PROJECT 1: Prepare following Items.

1. Prepare graph showing relationship between feature size, number of transistors year (Silicon Roadmap).
2. Prepare graph showing various design methodology.

MICRO PROJECT 2: These Projects usually include :Schematic Design, Simulation, Layout Design & VerificationDesign

1. Binary to Gray Code Converter
2. Traffic Light Controller using VLSI logic: implement using Finite State Machine (FSM)
3. Digital Clock Circuit Design

4. 4-Bit ALU Design
5. Ring Counter using CMOS
6. Johnson Counter Design
7. Low Power CMOS Logic Design
8. Design and Implement Water Level Indicator/controller circuit
9. Design and Implement Room Temperature Monitor/Controller System.

MICRO PROJECT 3: Prepare following Items.

1. Prepare chart indicating the types of etching processes used with its application.
2. Prepare chart indicating the deposition processes with its application.
3. Prepare a survey report on the types of transistors used in memory elements.
4. Prepare Report on basic fabrication steps of CMOS VLSI circuits
5. Prepare Charts for Block Diagram of VLSI Fabrication Process (Shows complete steps from wafer preparation to packaging
6. Prepare CMOS Fabrication Process Flow Chart (N-well/P-well fabrication steps)
7. Prepare Photolithography Process Chart (Mask-UV exposure-Developing-Pattern transfer)
8. Prepare Application of VLSI Technology Chart (Use in processors, memory, smartphones, etc.)

Suggested Activities for Students: Other than the laboratory learning, following are the suggested student-related co curricular activities which can be undertaken to accelerate the attainment of the various outcomes in this course: Students should conduct following activities in group and prepare reports of each activity.

□□□□□□□ Prepare chart to represent the CMOS design process

- Prepare chart to represent the technological advancements in CMOS technology starting from transistors to current technology
- Project- Build a small ASIC for your Home /Community.
- Prepare chart showing the types of FPGA technology
- List out methods used in industries for each step used in CMOS design process.

These are sample strategies, which the teacher can use to accelerate the attainment of the various outcomes in this course:

- Show Video/ Animation film explaining VLSI Design which are available on internet.
- Arrange expert lecture on Verilog programming for real life applications.
- Massive open online courses (MOOCs) may be used to teach various topics/sub topics.
- Guide students for using latest Technical Magazine.
- Visit industries where equipment/gadgets using VLSI are being manufactured/ assembled. vii. Guide student(s) in undertaking micro-projects.

* * * * * * *