Eca (DI02011011) - Problem Solver

Antigravity AI

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Eca

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To my students,
who constantly inspire me to find new analogies,
break down complex theories, and make learning
an engineered science.

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Preface

About this Book

Welcome to **Computer Networks**! This textbook is meticulously designed to serve as a comprehensive problem solver and study companion. It provides a robust and intuitive foundation in the core principles of this subject, bridging the gap between theoretical models and practical applications. A unique feature of this book is its focus on decoding complex concepts using clear, step-by-step methodologies and real-world analogies.

Target Audience

This book is intended for students and professionals looking to master the concepts of Computer Networks. Whether you are revising for exams, seeking to solidify your fundamental understanding, or looking for practical examples to clarify abstract concepts, this book has been structured to support your learning journey. It serves as an accessible guide designed to remove the fear of complex topics, replacing it with an appreciation for the underlying mechanics.

Scope and Coverage

The coverage is divided logically to follow standard academic curriculums. Each chapter focuses on key topics, breaking them down into digestible sections:

- **Theoretical Insights** – Core concepts explained intuitively.
- **Method Blocks** – Standardized, step-by-step procedures for solving specific types of problems.
- **Worked Examples** – Fully solved problems that apply the methods in practice.

We hope this resource proves invaluable in your studies and helps you achieve excellence in **Computer Networks**. Happy learning!

Acknowledgments

Writing a comprehensive book that connects the fundamental forces of Chemistry with practical engineering applications requires more than just academic knowledge—it requires a community of support. I would like to express my sincere gratitude to everyone who contributed to the realization of this project.

Specially, I extend my heartfelt gratitude to the **Department of Technical Education (DTE), Government of Gujarat**, and **Government Polytechnic, Palanpur**, for providing an environment that fosters innovation, academic rigor, and continuous professional development.

I am deeply thankful to my family for their unwavering patience and support during the countless hours spent researching, formatting, and refining these chapters.

Finally, my deepest appreciation goes to my students. Your curiosity, challenging questions, and continuous feedback are the true driving force behind the unique analogies and streamlined structure of this book. This textbook was engineered for you.

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About the Author

Milav Jayeshkumar Dabgar is an engineering educator and R&D professional with over 9 years of experience in electronics hardware development, embedded systems, AI/ML, and full-stack software engineering. He currently serves as a **Lecturer (Class - II) & Innovation Leader** at Government Polytechnic, Palanpur, under the Education Department of the Government of Gujarat.

Milav holds a Master of Engineering (ME) in Communication Systems from L.D. College of Engineering and a Bachelor of Engineering (BE) in Electronics & Communication. He is also currently pursuing a **BS in Data Science and Applications from IIT Madras**, where he has completed both the **Diploma in Programming** and the **Diploma in Data Science** with distinction.

Most recently, he completed the **AICTE QIP PG Certificate Program in Deep Learning from SVNIT Surat** with a **perfect 10/10 CGPA**, topping his batch.

A dedicated mentor, Milav has guided numerous student teams in securing over **INR 45 lakhs** in innovation funding, including INR 25 lakhs from Shark Tank India and INR 20 lakhs through iHub Gujarat, resulting in two student patents. He is recognized as an **NPTEL Evangelist** and **NPTEL Discipline Star** in Computer Science, reflecting his commitment to continuous learning and academic excellence.

His technical expertise spans from embedded systems (8051, STM32, Arduino) to modern web technologies (Next.js, Python, PostgreSQL) and Data Science (TensorFlow, PyTorch). Through this textbook, he aims to simplify complex Engineering Chemistry concepts by integrating relatable, real-world analogies drawn from modern tech and engineering landscapes.

Milav is also an active content creator, running a popular **YouTube channel** (@milav.dabgar) where he shares technical tutorials and academic resources. He maintains a personal blog and resource hub at milav.in and can be reached for professional collaborations on LinkedIn.

CHAPTER 1

Field Effect Transistors

1.1 JFET

Methodology:

JFET Drain Current and Transconductance Calculation The Junction Field Effect Transistor (JFET) is a voltage-controlled device. Its operation in the saturation region is defined by Shockley's equation.

1. Identify the maximum drain current I_{DSS} and the pinch-off voltage V_P. Note that V_P is negative for an n-channel JFET and positive for a p-channel JFET.
2. Determine the gate-to-source voltage V_{GS} applied to the device.
3. Calculate the drain current I_D using Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

4. Calculate the maximum transconductance g_{m0} using the formula:

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

5. Calculate the transconductance g_m at the specific operating point V_{GS}:

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

Worked Example:

Calculate JFET Drain Current and Transconductance An n-channel JFET has a maximum drain current $I_{DSS} = 12$ mA and a pinch-off voltage $V_P = -4$ V. Calculate the drain current I_D and the transconductance g_m when the gate-to-source voltage $V_{GS} = -2$ V.
Step 1: Identify given parameters $I_{DSS} = 12$ mA $= 12 \times 10^{-3}$ A $V_P = -4$ V $V_{GS} = -2$ V
Step 2: Calculate Drain Current I_D Using Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 12 \text{ mA}\left(1 - \frac{-2}{-4}\right)^2$$

$$I_D = 12 \text{ mA}\,(1 - 0.5)^2$$

$$I_D = 12 \text{ mA}(0.5)^2 = 12 \times 0.25 = 3 \text{ mA}$$

Step 3: Calculate maximum transconductance g_{m0}

$$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$

$$g_{m0} = \frac{2 \times 12 \text{ mA}}{|-4 \text{ V}|} = \frac{24 \text{ mA/V}}{4 \text{ V}} = 6 \text{ mA/V} = 6 \text{ mS}$$

Step 4: Calculate transconductance g_m at $V_{GS} = -2$ V

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$$

$$g_m = 6 \text{ mS}\left(1 - \frac{-2}{-4}\right)$$

$$g_m = 6 \text{ mS}\,(1 - 0.5) = 6 \times 0.5 = 3 \text{ mS}$$

1.2 MOSFET

Methodology:

MOSFET General Operating Modes and Conductivity Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs) operate similarly to JFETs but have an insulated gate. The general method for determining states involves checking V_{GS} against the threshold or pinch-off limits.

1. Identify the type of MOSFET (Depletion-type or Enhancement-type).
2. For Depletion-type, the device conducts when $V_{GS} = 0$ V and can operate in both depletion mode ($V_{GS} < 0$ for n-channel) and enhancement mode ($V_{GS} > 0$ for n-channel).
3. For Enhancement-type, the device is normally off and only conducts when $|V_{GS}| > |V_T|$, where V_T is the threshold voltage.

1.3 Depletion type MOSFET

Methodology:

Drain Current in Depletion Type MOSFET The D-MOSFET follows the same Shockley's equation as the JFET but allows for both positive and negative values of V_{GS} (for n-channel).

1. Identify I_{DSS} and V_P from the datasheet.
2. Determine the applied V_{GS}. For an n-channel D-MOSFET, V_{GS} can be negative (depletion mode) or positive (enhancement mode).
3. Use Shockley's equation to find the drain current:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Worked Example:

Calculate Drain Current for D-MOSFET in Both Modes An n-channel D-MOSFET has $I_{DSS} = 10$ mA and $V_P = -4$ V. Calculate the drain current for $V_{GS} = -2$ V and $V_{GS} = +2$ V.

Step 1: Calculate I_D for $V_{GS} = -2$ V (Depletion Mode)

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$I_D = 10 \text{ mA}\left(1 - \frac{-2}{-4}\right)^2$$

$$I_D = 10 \text{ mA}(1 - 0.5)^2 = 10 \text{ mA} \times 0.25 = 2.5 \text{ mA}$$

Step 2: Calculate I_D for $V_{GS} = +2$ V (Enhancement Mode)

$$I_D = 10 \text{ mA}\left(1 - \frac{+2}{-4}\right)^2$$

$$I_D = 10 \text{ mA}(1 - (-0.5))^2$$

$$I_D = 10 \text{ mA}(1.5)^2 = 10 \text{ mA} \times 2.25 = 22.5 \text{ mA}$$

1.4 Enhancement type MOSFET

Methodology:

Drain Current in Enhancement Type MOSFET The E-MOSFET does not conduct until V_{GS} exceeds a threshold voltage V_T. The drain current is determined using a conduction parameter k.

1. Identify the threshold voltage V_T (sometimes denoted as $V_{GS(th)}$) and a specified on-state point $(I_{D(on)}, V_{GS(on)})$.
2. Calculate the device parameter k using the on-state values:

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

3. For any given V_{GS} where $V_{GS} > V_T$ (for n-channel), calculate the drain current I_D:

$$I_D = k(V_{GS} - V_T)^2$$

Worked Example:

Calculate Parameter k and Drain Current for E-MOSFET An n-channel E-MOSFET has a threshold voltage $V_T = 2$ V. The datasheet specifies $I_{D(on)} = 8$ mA at $V_{GS(on)} = 6$ V. Determine the device parameter k and calculate the drain current I_D at $V_{GS} = 4$ V.

Step 1: Calculate the device parameter k

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

$$k = \frac{8 \text{ mA}}{(6 \text{ V} - 2 \text{ V})^2}$$

$$k = \frac{8 \text{ mA}}{(4 \text{ V})^2} = \frac{8 \text{ mA}}{16 \text{ V}^2} = 0.5 \text{ mA/V}^2$$

Step 2: Calculate Drain Current I_D at $V_{GS} = 4$ V

$$I_D = k(V_{GS} - V_T)^2$$

$$I_D = 0.5 \text{ mA/V}^2 \times (4 \text{ V} - 2 \text{ V})^2$$

$$I_D = 0.5 \times (2)^2 = 0.5 \times 4 = 2 \text{ mA}$$

1.5 Comparison of BJT, JFET, MOSFET

Methodology:

Evaluating Transistor Performance Metrics When choosing between BJT, JFET, and MOSFET devices for a specific application, several key computational parameters must be compared.

1. **Input Impedance (Z_{in}):** Calculate or evaluate the input impedance. BJTs have relatively low Z_{in} (e.g., 1 kΩ to 50 kΩ). JFETs have very high Z_{in} (e.g., $10^9\Omega$). MOSFETs have exceptionally high Z_{in} (e.g., $10^{12}\Omega$ to $10^{15}\Omega$).

2. **Current/Voltage Control:** BJT is a current-controlled device ($I_C = \beta I_B$). FETs are voltage-controlled devices (I_D depends on V_{GS}).

3. **Transconductance (g_m):** BJT generally yields higher transconductance compared to FETs, leading to higher voltage gains in equivalent amplifier configurations. $g_{m(BJT)} = \frac{I_C}{V_T}$, whereas $g_{m(FET)}$ is dependent on I_{DSS} and V_P.

Worked Example:

Comparing Input Current Requirements A circuit requires controlling a 10 mA output current. Compare the required input current for a BJT with $\beta = 100$ and a JFET with an input resistance of 1000 MΩ driven by a 5 V input signal.
Step 1: Calculate input current for the BJT The output current is the collector current $I_C = 10$ mA. The required base current I_B is:

$$I_B = \frac{I_C}{\beta} = \frac{10\text{ mA}}{100} = 0.1\text{ mA} = 100\,\mu\text{A}$$

Step 2: Calculate input current for the JFET The JFET is driven by an input voltage $V_{GS} = 5$ V. The gate current I_G is given by Ohm's law using the input resistance:

$$I_G = \frac{V_{GS}}{R_{in}} = \frac{5\text{ V}}{1000 \times 10^6\Omega} = 5 \times 10^{-9}\text{ A} = 5\text{ nA}$$

Conclusion: The BJT requires 100 μA of input current, whereas the JFET requires only 5 nA. This illustrates the vastly superior input impedance of the FET compared to the BJT.

1.6 FET applications

Methodology:

FET as a Voltage Variable Resistor A common application of a JFET is operating as a Voltage-Variable Resistor (VVR) in its ohmic (linear) region. This occurs when V_{DS} is very small (typically $V_{DS} \ll V_{GS} - V_P$).

1. Identify the minimum channel resistance R_0 (at $V_{GS} = 0$ V). This is given by:

$$R_0 = \frac{|V_P|}{2I_{DSS}}$$

2. Calculate the dynamic drain-to-source resistance r_d at a specific V_{GS} using the formula:

$$r_d = \frac{R_0}{1 - \frac{V_{GS}}{V_P}}$$

This equation is valid for the ohmic region, allowing the FET to act as a variable resistor controlled by V_{GS}.

Worked Example:

Calculate Resistance of FET in Ohmic Region An n-channel JFET has $I_{DSS} = 8$ mA and $V_P = -4$ V. It is used as a voltage-variable resistor. Calculate the drain-to-source resistance r_d at $V_{GS} = 0$ V and at $V_{GS} = -2$ V.

Step 1: Calculate minimum resistance R_0 at $V_{GS} = 0$ V

$$R_0 = \frac{|V_P|}{2I_{DSS}}$$

$$R_0 = \frac{|-4\text{ V}|}{2 \times 8\text{ mA}} = \frac{4}{16 \times 10^{-3}}\Omega$$

$$R_0 = \frac{1}{4 \times 10^{-3}}\Omega = 0.25 \times 10^3\Omega = 250\Omega$$

Thus, the resistance at $V_{GS} = 0$ V is 250Ω.

Step 2: Calculate resistance r_d at $V_{GS} = -2$ V

$$r_d = \frac{R_0}{1 - \frac{V_{GS}}{V_P}}$$

$$r_d = \frac{250}{1 - \frac{-2}{-4}}$$

$$r_d = \frac{250}{1 - 0.5}$$

$$r_d = \frac{250}{0.5} = 500\Omega$$

By changing V_{GS} from 0 V to -2 V, the resistance increases from 250Ω to 500Ω.

CHAPTER 2

Transistor Biasing Circuits and Thermal Stability

2.1 Biasing of Amplifier and Operating Point

Transistor biasing is the process of setting a fixed level of direct current (DC) voltage and current in a transistor circuit. This establishes the Operating Point (or Q-point) in the active region for linear amplification.

Methodology:

DC Load Line and Q-Point Analysis To determine the operating point (Q-point) and draw the DC load line for a Common Emitter (CE) amplifier:

1. **Determine Base Current (I_B):** Apply Kirchhoff's Voltage Law (KVL) to the input (base-emitter) loop. Assume $V_{BE} = 0.7$ V for a silicon transistor unless specified otherwise.
2. **Calculate Collector Current (I_C):** Use the relation $I_C = \beta I_B$, where β (or h_{FE}) is the DC current gain.
3. **Determine Collector-Emitter Voltage (V_{CE}):** Apply KVL to the output (collector-emitter) loop to solve for V_{CE}. The Q-point is (V_{CEQ}, I_{CQ}).
4. **Plot DC Load Line:** The DC load line connects the two extreme operating limits on the output characteristic curve:
   - **Saturation Point (y-intercept):** Set $V_{CE} = 0$ to find maximum current, $I_{C(sat)} = V_{CC}/(R_C + R_E)$.
   - **Cut-off Point (x-intercept):** Set $I_C = 0$ to find maximum voltage, $V_{CE(off)} = V_{CC}$.

Worked Example:

Q-Point and DC Load Line Calculation A fixed bias circuit has $V_{CC} = 12$ V, base resistor $R_B = 240$ kΩ, collector resistor $R_C = 2.2$ kΩ, and $\beta = 50$. Assume a silicon transistor ($V_{BE} = 0.7$ V). Calculate the Q-point and the DC load line endpoints.

Step 1: Calculate Base Current I_B Applying KVL to the base loop:

$$V_{CC} - I_B R_B - V_{BE} = 0$$

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \frac{11.3}{240 \times 10^3} \approx 47.08\,\mu\text{A}$$

Step 2: Calculate Collector Current I_C

$$I_C = \beta I_B = 50 \times 47.08\,\mu\text{A} = 2.35\text{ mA}$$

Step 3: Calculate Collector-Emitter Voltage V_{CE} Applying KVL to the collector loop:

$$V_{CE} = V_{CC} - I_C R_C = 12\text{ V} - (2.35\text{ mA})(2.2\text{ k}\Omega) = 12 - 5.17 = 6.83\text{ V}$$

The Q-point is $(6.83\text{ V}, 2.35\text{ mA})$.

Step 4: DC Load Line Endpoints

- Cut-off (x-intercept): $V_{CE} = V_{CC} = 12\text{ V}$ (at $I_C = 0$)
- Saturation (y-intercept): $I_C = V_{CC}/R_C = 12/2.2\text{ k}\Omega = 5.45\text{ mA}$ (at $V_{CE} = 0$)

2.2 D.C. and A.C. Load Lines

While the DC load line represents the steady-state conditions without an input signal, the AC load line defines the dynamic operation of the amplifier when an AC signal is applied.

Methodology:

AC Load Line Analysis To determine the AC load line parameters for an amplifier with a load resistor R_L coupled via a capacitor:

1. **Determine AC Load Resistance (r_L):** In AC equivalent circuits, DC sources are shorted to ground and coupling/bypass capacitors act as short circuits. The effective AC load on the collector is $r_L = R_C \parallel R_L$.
2. **Calculate Maximum AC Collector Current Swing:** The peak maximum current (y-intercept of AC load line) is $I_{C(max)} = I_{CQ} + \frac{V_{CEQ}}{r_L}$.
3. **Calculate Maximum AC Collector Voltage Swing:** The peak maximum voltage (x-intercept of AC load line) is $V_{CE(max)} = V_{CEQ} + I_{CQ}r_L$.
4. **Draw the AC Load Line:** The AC load line passes through the Q-point (V_{CEQ}, I_{CQ}) and intersects the axes at $I_{C(max)}$ and $V_{CE(max)}$. It is always steeper than the DC load line since $r_L < R_{DC}$.

Worked Example:

AC Load Line Endpoints An amplifier has a Q-point of $V_{CEQ} = 5\text{ V}$ and $I_{CQ} = 2\text{ mA}$. The collector resistor is $R_C = 4\text{ k}\Omega$ and it drives a load resistor $R_L = 4\text{ k}\Omega$. Find the AC load line endpoints.

Step 1: Determine AC load resistance

$$r_L = R_C \parallel R_L = \frac{4\text{ k}\Omega \times 4\text{ k}\Omega}{4\text{ k}\Omega + 4\text{ k}\Omega} = 2\text{ k}\Omega$$

Step 2: Maximum current swing on AC load line

$$I_{C(max)} = I_{CQ} + \frac{V_{CEQ}}{r_L} = 2\text{ mA} + \frac{5\text{ V}}{2\text{ k}\Omega} = 2\text{ mA} + 2.5\text{ mA} = 4.5\text{ mA}$$

Step 3: Maximum voltage swing on AC load line

$$V_{CE(max)} = V_{CEQ} + I_{CQ}r_L = 5\text{ V} + (2\text{ mA})(2\text{ k}\Omega) = 5\text{ V} + 4\text{ V} = 9\text{ V}$$

The AC load line passes through $(5\text{ V}, 2\text{ mA})$ and terminates at $(9\text{ V}, 0\text{ A})$ and $(0\text{ V}, 4.5\text{ mA})$.

2.3 Biasing Methods

Several biasing methods exist, offering varying degrees of stability against changes in temperature and transistor parameters (β).

Methodology:

Voltage Divider Bias Analysis Voltage divider biasing (or emitter bias) is the most widely used biasing circuit due to its excellent stability. We use Thevenin's Theorem to simplify the base circuit.

1. **Calculate Thevenin Voltage (V_{TH}):** $V_{TH} = V_{CC}\frac{R_2}{R_1+R_2}$
2. **Calculate Thevenin Resistance (R_{TH}):** $R_{TH} = \frac{R_1R_2}{R_1+R_2}$
3. **Apply KVL to Base-Emitter Loop:**

$$V_{TH} - I_BR_{TH} - V_{BE} - I_ER_E = 0$$

Substituting $I_E = (\beta+1)I_B$:

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta+1)R_E}$$

4. **Find Output Values:** $I_C = \beta I_B$. Use KVL on the collector loop: $V_{CE} = V_{CC} - I_CR_C - I_ER_E \approx V_{CC} - I_C(R_C + R_E)$.

Worked Example:

Voltage Divider Bias Computation A voltage divider bias circuit has $V_{CC} = 22$ V, $R_1 = 39$ kΩ, $R_2 = 3.9$ kΩ, $R_C = 10$ kΩ, $R_E = 1.5$ kΩ, and $\beta = 140$. Calculate the Q-point.

Step 1: Thevenin Voltage and Resistance

$$V_{TH} = 22 \times \frac{3.9}{39+3.9} = 2 \text{ V}$$

$$R_{TH} = \frac{39 \times 3.9}{39+3.9} \text{ kΩ} = 3.55 \text{ kΩ}$$

Step 2: Base Current

$$I_B = \frac{2 \text{ V} - 0.7 \text{ V}}{3.55 \text{ kΩ} + (141)(1.5 \text{ kΩ})} = \frac{1.3}{3.55 + 211.5} = \frac{1.3}{215.05} \approx 6.05\,\mu\text{A}$$

Step 3: Collector Current and Collector-Emitter Voltage

$$I_C = \beta I_B = 140 \times 6.05\,\mu\text{A} = 0.847 \text{ mA}$$

$$I_E \approx I_C = 0.847 \text{ mA}$$

$$V_{CE} = V_{CC} - I_CR_C - I_ER_E = 22 - 0.847(10) - 0.847(1.5) = 22 - 8.47 - 1.27 = 12.26 \text{ V}$$

The Q-point is $(12.26 \text{ V}, 0.847 \text{ mA})$.

Methodology:

Collector to Base Feedback Bias Analysis In this method, the base resistor R_B is connected directly to the collector instead of V_{CC}, introducing negative DC feedback.

1. **Input Loop Equation:** KVL yields $V_{CC} - (I_C + I_B)R_C - I_BR_B - V_{BE} - I_ER_E = 0$.
2. **Calculate I_B:** Approximating $I_C \approx I_E \approx \beta I_B$, we get:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + \beta(R_C + R_E)}$$

3. **Calculate V_{CE}:**

$$V_{CE} = V_{CC} - I_C(R_C + R_E)$$

2.4 Stability Factor

The stability of the Q-point is quantified by the Stability Factor (S). It measures how sensitive the collector current (I_C) is to changes in the reverse saturation current (I_{CO}). A smaller value of S implies better thermal stability.

Methodology:

Evaluating Stability Factor S The general formula for stability factor S is derived using partial differentiation:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

Depending on the bias circuit, $\frac{\partial I_B}{\partial I_C}$ takes different forms:

- **Fixed Bias:** $\frac{\partial I_B}{\partial I_C} = 0 \implies S = 1+\beta$. (Very poor stability)
- **Collector Feedback Bias:** $S = \frac{1+\beta}{1+\beta\frac{R_C}{R_C+R_B}}$
- **Voltage Divider Bias:** $S = (1+\beta)\frac{1+\frac{R_{TH}}{R_E}}{1+\beta+\frac{R_{TH}}{R_E}}$

Worked Example:

Calculating Stability Factor S A voltage divider bias circuit has $R_1 = 50\ \text{k}\Omega$, $R_2 = 10\ \text{k}\Omega$, $R_E = 2\ \text{k}\Omega$, and $\beta = 100$. Calculate the stability factor S.

Step 1: Calculate R_{TH}

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2} = \frac{50 \times 10}{50 + 10} = \frac{500}{60} = 8.33\ \text{k}\Omega$$

Step 2: Calculate Ratio R_{TH}/R_E

$$\frac{R_{TH}}{R_E} = \frac{8.33\ \text{k}\Omega}{2\ \text{k}\Omega} = 4.165$$

Step 3: Compute S

$$S = (1+100)\frac{1+4.165}{1+100+4.165} = 101 \times \frac{5.165}{105.165} = 101 \times 0.0491 \approx 4.96$$

The stability factor is approximately 4.96 (much better than fixed bias where $S = 101$).

2.5 Compensation Techniques for Bias Stability

When passive biasing circuits are insufficient to counter temperature variations (especially in V_{BE} and I_{CO}), active compensation techniques using temperature-sensitive devices are employed.

Methodology:

Thermistor and Diode Compensation These techniques involve adding non-linear elements to the bias network.

1. **Thermistor Compensation:** A thermistor (NTC - Negative Temperature Coefficient) is placed in the base circuit (e.g., replacing R_2 in voltage divider bias).
   - As Temperature (T) increases, I_C increases.
   - Thermistor resistance R_T decreases, dropping the voltage at the base.
   - This decreases I_B, pulling I_C back down and stabilizing the Q-point.

2. **Diode Compensation for V_{BE}:** A forward-biased diode of the same material as the transistor is placed in the bias network.
    - As T increases, both transistor V_{BE} and diode voltage V_D drop by approximately 2.5 mV/°C.
    - By placing the diode such that its voltage drop opposes the bias voltage, the effective base bias adjusts automatically to keep I_C constant.

2.6 Thermal Stability and Thermal Runaway

Power dissipation at the collector junction generates heat, raising the junction temperature (T_J). If the heat is not dissipated faster than it is generated, T_J increases, raising I_C and thus generating even more heat. This positive feedback loop can destroy the transistor, a condition known as **Thermal Runaway**.

Methodology:

Thermal Resistance and Temperature Calculations The relationship between power dissipation, thermal resistance, and junction temperature dictates safe operation:

1. **Calculate Power Dissipation (P_D):**
$$P_D \approx V_{CE} I_C$$
2. **Calculate Junction Temperature (T_J):**
$$T_J = T_A + \theta_{JA} P_D$$
Where T_A is the ambient temperature, and θ_{JA} is the total thermal resistance from junction to ambient (°C/W).
3. **Expand Thermal Resistance Elements:** If a heat sink is used:
$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$
Where:
    - θ_{JC} = Junction-to-Case thermal resistance.
    - θ_{CS} = Case-to-Sink thermal resistance (mica washer, thermal paste).
    - θ_{SA} = Sink-to-Ambient thermal resistance (the Heat Sink itself).
4. **Condition for Thermal Stability:** To prevent thermal runaway, the rate of heat removal must exceed the rate of heat generation:
$$\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$$

Worked Example:

Junction Temperature and Heat Sink Sizing A power transistor dissipates $P_D = 20$ W in an ambient temperature of $T_A = 40$°C. The transistor's maximum allowable junction temperature is $T_{J(max)} = 150$°C. Given $\theta_{JC} = 1.5$°C/W and $\theta_{CS} = 0.5$°C/W, calculate the maximum permissible thermal resistance of the heat sink (θ_{SA}).

Step 1: Determine Maximum Total Thermal Resistance (θ_{JA}) Using the temperature formula $T_J = T_A + \theta_{JA} P_D$, rearrange for θ_{JA}:

$$\theta_{JA} = \frac{T_{J(max)} - T_A}{P_D} = \frac{150°\text{C} - 40°\text{C}}{20\ \text{W}} = \frac{110}{20} = 5.5°\text{C/W}$$

Step 2: Calculate Required Heat Sink Resistance (θ_{SA}) Since $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$:

$$\theta_{SA} = \theta_{JA} - \theta_{JC} - \theta_{CS}$$

$$\theta_{SA} = 5.5 - 1.5 - 0.5 = 3.5°\text{C/W}$$

A heat sink with a thermal resistance of 3.5°C/W or lower must be selected to guarantee safe operation.

Methodology:

Heat Sink Types To achieve the required θ_{SA}, heat sinks are mechanically attached to the transistor case to increase the surface area for heat dissipation. Common types include:

1. **Stamped Heat Sinks:** Made from stamped metal sheets. Used in low-power applications. Low cost but higher θ_{SA}.
2. **Extruded Heat Sinks:** Aluminum pushed through a die to create complex fin shapes. The most common type for moderate-to-high power dissipations.
3. **Bonded/Folded Fin Heat Sinks:** Fins are bonded to a base plate, allowing for very dense fin spacing. Used in high-performance applications where space is limited.

CHAPTER 3

Frequency Response of Transistor Amplifier

3.1 Amplifier Gain and Decibels

The performance of an amplifier is often evaluated by its gain, which represents its ability to increase the amplitude of an electrical signal. Gain is frequently expressed on a logarithmic scale using decibels (dB) because it compresses a wide range of values into a manageable scale and allows for the simple addition of cascaded gains.

Methodology:

Calculating Amplifier Gain in Decibels To calculate the voltage, current, or power gain in decibels, use the following definitions:

1. **Linear Gain Equations:**
   - Voltage Gain: $A_v = \frac{V_{out}}{V_{in}}$
   - Current Gain: $A_i = \frac{I_{out}}{I_{in}}$
   - Power Gain: $A_p = \frac{P_{out}}{P_{in}}$
2. **Decibel (dB) Gain Equations:**
   - Voltage Gain in dB: $A_{v(dB)} = 20 \log_{10}(|A_v|)$
   - Current Gain in dB: $A_{i(dB)} = 20 \log_{10}(|A_i|)$
   - Power Gain in dB: $A_{p(dB)} = 10 \log_{10}(|A_p|)$
3. **Conversion from dB back to Linear Gain:**
   - $A_v = 10^{\frac{A_{v(dB)}}{20}}$
   - $A_p = 10^{\frac{A_{p(dB)}}{10}}$

Worked Example:

Calculate Gains for a Single Stage Amplifier An amplifier has an input voltage of 50 mV and an output voltage of 2 V. The input current is 10 μA and the output current is 2 mA. Calculate the voltage gain in dB, current gain in dB, and power gain in dB.

Step 1: Calculate linear voltage and current gains.

$$A_v = \frac{V_{out}}{V_{in}} = \frac{2 \text{ V}}{50 \times 10^{-3} \text{ V}} = 40$$

$$A_i = \frac{I_{out}}{I_{in}} = \frac{2 \times 10^{-3} \text{ A}}{10 \times 10^{-6} \text{ A}} = 200$$

Step 2: Calculate linear power gain. Since $P = V \times I$, the power gain is the product of voltage and current gains.

$$A_p = A_v \times A_i = 40 \times 200 = 8000$$

Step 3: Convert linear gains to dB.

$$A_{v(dB)} = 20\log_{10}(40) = 20 \times 1.602 = 32.04 \text{ dB}$$

$$A_{i(dB)} = 20\log_{10}(200) = 20 \times 2.301 = 46.02 \text{ dB}$$

$$A_{p(dB)} = 10\log_{10}(8000) = 10 \times 3.903 = 39.03 \text{ dB}$$

3.2 Bandwidth of Single Stage Amplifier

The bandwidth (BW) of an amplifier is the range of frequencies over which the amplifier's gain remains relatively constant. The boundaries of this range are defined by the cut-off frequencies, which are the points where the power gain drops to half its midband value (or voltage gain drops by 3 dB).

Methodology:

Calculating Bandwidth and Half Power Frequencies Follow these steps to find the amplifier's bandwidth:

1. Identify the **lower cut-off frequency** (f_L) and the **upper cut-off frequency** (f_H). At these frequencies, the voltage gain is:

$$A_{v(cut-off)} = \frac{A_{v(mid)}}{\sqrt{2}} \approx 0.707 \cdot A_{v(mid)}$$

2. Alternatively, identify these points as where the dB gain falls by exactly 3 dB from the maximum midband gain.

3. Compute the **Bandwidth**:

$$BW = f_H - f_L$$

Note: If f_H is much larger than f_L (i.e., $f_H \gg f_L$), then $BW \approx f_H$.

Worked Example:

Determining Amplifier Bandwidth from Given Limits A transistor amplifier has a maximum voltage gain of 100 at mid-frequency. Its gain drops to 70.7 at a lower frequency of 50 Hz and an upper frequency of 200 kHz. Calculate the midband gain in dB, the decibel gain at the cut-off frequencies, and the total bandwidth.

Step 1: Calculate midband gain in dB.

$$A_{v(mid,dB)} = 20\log_{10}(100) = 20 \times 2 = 40 \text{ dB}$$

Step 2: Check the gain at the stated frequencies. At 50 Hz and 200 kHz, the gain is 70.7. $\frac{100}{\sqrt{2}} \approx 70.7$. Thus, 50 Hz is f_L and 200 kHz is f_H. The dB gain at cut-off is:

$$A_{v(cut-off,dB)} = 20\log_{10}(70.7) \approx 37 \text{ dB}$$

Observe that 40 dB − 3 dB = 37 dB.

Step 3: Calculate the bandwidth.

$$BW = f_H - f_L = 200,000 \text{ Hz} - 50 \text{ Hz} = 199,950 \text{ Hz} = 199.95 \text{ kHz}$$

3.3 Gain Bandwidth Product

For many amplifiers, especially internally compensated operational amplifiers and basic transistor stages, there is a fundamental trade-off between the gain and the bandwidth. The product of the two remains constant.

Methodology:

Using the Gain Bandwidth Product The Gain-Bandwidth Product (GBW or GBP) is a constant figure of merit for an amplifier.

1. **Constant GBW Formula:**
$$GBW = A_{mid} \times BW$$
2. **Trade-off Application:** If negative feedback is used or circuit parameters are changed such that the gain is decreased to a new value A'_{mid}, the new bandwidth BW' increases proportionally:
$$A_{mid} \times BW = A'_{mid} \times BW'$$

Note: Ensure the gain used in the GBW product formula is the linear voltage gain, not the gain in dB.

Worked Example:

Calculating Modified Bandwidth using GBW An amplifier has an open-loop voltage gain of 500 and a bandwidth of 20 kHz. If negative feedback is introduced to reduce the gain to 50, calculate the new bandwidth of the amplifier.

Step 1: Calculate the Gain-Bandwidth Product (GBW).

$$GBW = A_{mid} \times BW = 500 \times 20,000 \text{ Hz} = 10,000,000 \text{ Hz} = 10 \text{ MHz}$$

Step 2: Equate the GBW to the new gain and bandwidth.

$$GBW = A'_{mid} \times BW'$$

$$10,000,000 = 50 \times BW'$$

Step 3: Solve for the new bandwidth.

$$BW' = \frac{10,000,000}{50} = 200,000 \text{ Hz} = 200 \text{ kHz}$$

The new bandwidth expands to 200 kHz when the gain is reduced by a factor of 10.

3.4 Effect of Emitter Bypass and Coupling Capacitor

The low-frequency response of a transistor amplifier is primarily dictated by the coupling capacitors (C_C) and the emitter bypass capacitor (C_E). At very low frequencies, their capacitive reactance ($X_C = 1/2\pi fC$) becomes significant, acting as an open circuit and reducing the gain.

Methodology:

Critical Low Cut off Frequencies due to Capacitors Each capacitor forms a high-pass RC filter with the equivalent resistance of the circuit. The cut-off frequency created by each capacitor is computed independently.

1. **Input Coupling Capacitor (C_{c1}):**
$$f_{L1} = \frac{1}{2\pi(R_s + R_{in})C_{c1}}$$
where R_s is the source resistance and R_{in} is the input resistance of the amplifier.
2. **Output Coupling Capacitor (C_{c2}):**
$$f_{L2} = \frac{1}{2\pi(R_C + R_L)C_{c2}}$$

where R_C is the collector resistance and R_L is the load resistance.

3. **Emitter Bypass Capacitor (C_E):**
$$f_{L3} = \frac{1}{2\pi R_e C_E}$$
where R_e is the Thevenin equivalent resistance looking into the emitter circuit.

4. **Dominant Lower Cut-off Frequency:** The actual lower cut-off frequency f_L of the entire amplifier stage is determined by the highest of these three frequencies:
$$f_L \approx \max(f_{L1}, f_{L2}, f_{L3})$$

Worked Example:

Calculate the Lower Cut off Frequency Component An amplifier has an input resistance of 4 kΩ and is driven by a voltage source with a source resistance of 1 kΩ. It uses an input coupling capacitor $C_{c1} = 2\,\mu$F. Calculate the lower cut-off frequency due to this input coupling network.

Step 1: Identify the equivalent series resistance for the input loop.

$$R_{eq} = R_s + R_{in} = 1000\ \Omega + 4000\ \Omega = 5000\ \Omega$$

Step 2: Apply the RC cut-off frequency formula.

$$f_{L1} = \frac{1}{2\pi R_{eq} C_{c1}}$$

$$f_{L1} = \frac{1}{2 \times 3.1416 \times 5000 \times 2 \times 10^{-6}}$$

Step 3: Compute the final value.

$$f_{L1} = \frac{1}{6.2832 \times 0.01} = \frac{1}{0.062832} \approx 15.9\ \text{Hz}$$

3.5 Gain of Multi-Stage Amplifier

To achieve high voltage or current gains that a single transistor stage cannot provide, multiple amplifier stages are cascaded (connected in series). The overall gain is derived from the individual gains of each stage.

Methodology:

Calculating Gain of Multi Stage Amplifiers When n amplifier stages are connected in cascade, the overall gain is evaluated as follows:

1. **Linear Overall Gain:** Multiply the individual linear gains of each stage.
$$A_{total} = A_1 \times A_2 \times A_3 \times \cdots \times A_n$$

2. **Overall Gain in Decibels (dB):** Add the individual decibel gains of each stage.
$$A_{total(dB)} = A_{1(dB)} + A_{2(dB)} + A_{3(dB)} + \cdots + A_{n(dB)}$$

Worked Example:

Overall Gain of a Cascaded Amplifier A three-stage amplifier system has individual stage voltage gains of $A_1 = 10$, $A_2 = 50$, and $A_3 = 20$. Calculate the overall linear voltage gain and the overall voltage gain in decibels.

Step 1: Calculate the overall linear voltage gain.

$$A_{total} = A_1 \times A_2 \times A_3$$

$$A_{total} = 10 \times 50 \times 20 = 10,000$$

Step 2: Calculate individual dB gains.

$$A_{1(dB)} = 20 \log_{10}(10) = 20 \times 1 = 20 \text{ dB}$$

$$A_{2(dB)} = 20 \log_{10}(50) = 20 \times 1.699 = 33.98 \text{ dB}$$

$$A_{3(dB)} = 20 \log_{10}(20) = 20 \times 1.301 = 26.02 \text{ dB}$$

Step 3: Sum the dB gains to find the overall dB gain.

$$A_{total(dB)} = 20 + 33.98 + 26.02 = 80 \text{ dB}$$

Verification:

$$20 \log_{10}(A_{total}) = 20 \log_{10}(10,000) = 20 \times 4 = 80 \text{ dB}$$

The results match.

3.6 Coupling Techniques

Various coupling methods are used to transfer signals between cascaded amplifier stages while ensuring proper DC biasing remains undisturbed. The four main types are:

- **RC Coupling:** Uses resistors and capacitors. Excellent frequency response over audio frequencies, but cannot pass DC.
- **LC Coupling:** Uses inductors and capacitors. High efficiency but bulky and suffers from poor low-frequency response.
- **Transformer Coupling:** Uses a transformer. Excellent for impedance matching and isolating DC, widely used in power amplifiers.
- **Direct Coupling:** Connects the output of one stage directly to the input of the next. Able to amplify DC signals (0 Hz) but suffers from thermal drift.

Methodology:

Transformer Coupling and Impedance Matching Transformer coupling is primarily calculated based on the turns ratio for perfect impedance matching, ensuring maximum power transfer.

1. Identify the primary turns (N_p) and secondary turns (N_s).
2. Calculate the turns ratio: $n = \frac{N_p}{N_s}$.
3. The equivalent impedance (R'_L) reflected to the primary side from the load resistance (R_L) on the secondary is:

$$R'_L = \left(\frac{N_p}{N_s}\right)^2 \times R_L = n^2 \times R_L$$

Worked Example:

Calculating Turns Ratio for Impedance Matching An audio output amplifier requires an effective load impedance of 4 kΩ to transfer maximum power to a loudspeaker having a resistance of 8 Ω. Calculate the required turns ratio of the coupling transformer.

Step 1: Set up the impedance matching equation.

$$R'_L = n^2 \times R_L$$

Where $R'_L = 4000\ \Omega$ (primary side) and $R_L = 8\ \Omega$ (secondary side).
Step 2: Solve for n^2.

$$4000 = n^2 \times 8$$

$$n^2 = \frac{4000}{8} = 500$$

Step 3: Solve for the turns ratio n.

$$n = \sqrt{500} \approx 22.36$$

The transformer needs a primary-to-secondary turns ratio of approximately $22.36 : 1$.

3.7 Frequency Response of Two-Stage RC Coupled Amplifier

When multiple identical amplifier stages are cascaded, the overall bandwidth shrinks. The overall lower cut-off frequency increases, and the overall upper cut-off frequency decreases.

Methodology:

Bandwidth Shrinkage in Cascaded Identical Stages For a multi-stage amplifier comprising n identical stages, each with a lower cut-off f_L and upper cut-off f_H, the new overall cut-off frequencies are:

1. **Overall Lower Cut-off Frequency ($f_{L(overall)}$):**

$$f_{L(overall)} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

2. **Overall Upper Cut-off Frequency ($f_{H(overall)}$):**

$$f_{H(overall)} = f_H \times \sqrt{2^{1/n} - 1}$$

3. **Overall Bandwidth:**

$$BW_{overall} = f_{H(overall)} - f_{L(overall)}$$

For a **Two-Stage** amplifier ($n = 2$), the shrinkage factor simplifies:

$$\sqrt{2^{1/2} - 1} = \sqrt{1.414 - 1} = \sqrt{0.414} \approx 0.643$$

Worked Example:

Calculate Frequencies for a Two Stage RC Amplifier A single-stage RC coupled amplifier has a lower cut-off frequency of 40 Hz and an upper cut-off frequency of 2 MHz. Two such identical stages are cascaded. Find the overall lower and upper cut-off frequencies and the new bandwidth of the two-stage amplifier.
Step 1: Identify given parameters. $f_L = 40$ Hz, $f_H = 2$ MHz, and $n = 2$ stages. We know the constant for $n = 2$ is $\sqrt{2^{1/2} - 1} \approx 0.643$.
Step 2: Calculate the overall lower cut-off frequency.

$$f_{L(overall)} = \frac{f_L}{0.643} = \frac{40}{0.643} \approx 62.2 \text{ Hz}$$

(The lower cut-off frequency has increased, meaning poorer low-frequency response).
Step 3: Calculate the overall upper cut-off frequency.

$$f_{H(overall)} = f_H \times 0.643 = 2,000,000 \times 0.643 = 1,286,000 \text{ Hz} = 1.286 \text{ MHz}$$

(The upper cut-off frequency has decreased).
Step 4: Calculate the overall bandwidth.

$$BW_{overall} = 1,286,000 \text{ Hz} - 62.2 \text{ Hz} \approx 1.286 \text{ MHz}$$

The bandwidth of the cascaded system has shrunk significantly compared to the single stage bandwidth of nearly 2 MHz.

CHAPTER 4

Feedback in Amplifiers

4.1 Concept of Feedback

In amplifiers, feedback is the process of returning a fraction of the output signal to the input. Depending on the phase of the feedback signal relative to the input signal, feedback can be either positive or negative.

Methodology:

Calculating Feedback Parameters

1. **Open-Loop Gain (A):** Gain of the amplifier without any feedback connection.
2. **Feedback Factor (β):** The fraction of output voltage (or current) fed back to the input.
3. **Loop Gain:** The product $A\beta$.
4. **Feedback Signal (V_f):** The voltage returned to the input. It is defined as $V_f = \beta V_o$.

Worked Example:

Calculate Feedback Voltage An amplifier has an open-loop voltage gain of 1000 and an output voltage of 10 V. If 5% of the output voltage is fed back to the input, calculate the feedback factor and the feedback voltage.

Solution:

1. **Identify given values:** Open-loop gain $A = 1000$, Output voltage $V_o = 10$ V, Feedback percentage $= 5\%$.
2. **Calculate Feedback Factor (β):**
$$\beta = \frac{5}{100} = 0.05$$
3. **Calculate Feedback Voltage (V_f):**
$$V_f = \beta \times V_o = 0.05 \times 10 = 0.5 \text{ V}$$

4.2 Types of Feedback

Feedback is broadly classified into two types based on the phase relation between the input signal and the feedback signal:

1. **Positive Feedback:** The feedback signal is in phase with the input signal. Used mainly in oscillators.
2. **Negative Feedback:** The feedback signal is out of phase (usually by 180°) with the input signal. Widely used in amplifiers to stabilize gain.

Furthermore, negative feedback is classified based on the sampling and mixing networks:

1. Voltage-Series Feedback
2. Voltage-Shunt Feedback
3. Current-Series Feedback
4. Current-Shunt Feedback

4.3 Voltage Gain with Feedback

Methodology:

Closed-Loop Voltage Gain Computation The gain of an amplifier with feedback (closed-loop gain) is denoted by A_f.

1. **For Negative Feedback:**
$$A_f = \frac{A}{1 + A\beta}$$
2. **For Positive Feedback:**
$$A_f = \frac{A}{1 - A\beta}$$
3. **Desensitivity Factor:** The quantity $(1 + A\beta)$ for negative feedback is called the desensitivity factor.

Worked Example:

Gain with Negative Feedback An amplifier has an open-loop gain of 500. A negative feedback is applied with a feedback fraction of 0.04. Calculate the closed-loop gain.
Solution:

1. **Identify given values:** $A = 500$, $\beta = 0.04$.
2. **Apply Negative Feedback Formula:**
$$A_f = \frac{A}{1 + A\beta}$$
3. **Compute Denominator:**
$$1 + A\beta = 1 + (500 \times 0.04) = 1 + 20 = 21$$
4. **Calculate A_f:**
$$A_f = \frac{500}{21} \approx 23.81$$

The closed-loop gain is 23.81.

Worked Example:

Required Feedback Factor for Desired Gain An amplifier has an open-loop gain of 1000. It is required to have a closed-loop gain of 100 using negative feedback. Calculate the required feedback fraction and the loop gain.
Solution:

1. **Identify given values:** $A = 1000$, $A_f = 100$.

2. **Rearrange Feedback Formula to solve for β:**

$$A_f = \frac{A}{1 + A\beta} \implies 1 + A\beta = \frac{A}{A_f}$$

3. **Compute $1 + A\beta$:**

$$1 + A\beta = \frac{1000}{100} = 10$$

4. **Calculate Loop Gain ($A\beta$):**

$$A\beta = 10 - 1 = 9$$

5. **Calculate Feedback Factor (β):**

$$\beta = \frac{9}{A} = \frac{9}{1000} = 0.009$$

The required feedback fraction is 0.009.

4.4 Effect of Negative Feedback

Negative feedback modifies various parameters of an amplifier significantly.

Methodology:

Effects on Amplifier Parameters For an amplifier with negative feedback (where desensitivity factor $D = 1 + A\beta$):

1. **Gain Stability:** The fractional change in gain is reduced.

$$\frac{dA_f}{A_f} = \frac{1}{1 + A\beta}\frac{dA}{A}$$

2. **Bandwidth (BW_f):** Bandwidth is increased.

$$BW_f = BW_{open} \times (1 + A\beta)$$

3. **Non-linear Distortion (D_f) and Noise (N_f):** Both are reduced.

$$D_f = \frac{D_{open}}{1 + A\beta}, \quad N_f = \frac{N_{open}}{1 + A\beta}$$

4. **Input Impedance (Z_{if}):**
   - Series mixing increases input impedance: $Z_{if} = Z_i(1 + A\beta)$
   - Shunt mixing decreases input impedance: $Z_{if} = \frac{Z_i}{1+A\beta}$
5. **Output Impedance (Z_{of}):**
   - Voltage sampling decreases output impedance: $Z_{of} = \frac{Z_o}{1+A\beta}$
   - Current sampling increases output impedance: $Z_{of} = Z_o(1 + A\beta)$

Worked Example:

Bandwidth and Distortion Calculation An amplifier has an open-loop gain of 200, bandwidth of 50 kHz, and 5% harmonic distortion. A negative feedback with $\beta = 0.02$ is introduced. Calculate the new bandwidth

and new distortion.
Solution:

1. **Identify given values:** $A = 200$, $BW_{open} = 50$ kHz, $D_{open} = 5\% = 0.05$, $\beta = 0.02$.
2. **Compute Desensitivity Factor:**

$$1 + A\beta = 1 + (200 \times 0.02) = 1 + 4 = 5$$

3. **Calculate New Bandwidth (BW_f):**

$$BW_f = BW_{open} \times (1 + A\beta) = 50 \text{ kHz} \times 5 = 250 \text{ kHz}$$

4. **Calculate New Distortion (D_f):**

$$D_f = \frac{D_{open}}{1 + A\beta} = \frac{5\%}{5} = 1\%$$

The new bandwidth is 250 kHz and the new distortion is 1%.

Worked Example:

Input and Output Impedance Evaluation A voltage-series negative feedback amplifier has $A = 100$, $R_i = 2$ kΩ, $R_o = 40$ kΩ, and $\beta = 0.09$. Determine the input and output impedances with feedback.
Solution:

1. **Compute Desensitivity Factor:**

$$1 + A\beta = 1 + (100 \times 0.09) = 1 + 9 = 10$$

2. **Calculate Input Impedance (R_{if}):** For voltage-series feedback, R_i increases.

$$R_{if} = R_i(1 + A\beta) = 2 \text{ k}\Omega \times 10 = 20 \text{ k}\Omega$$

3. **Calculate Output Impedance (R_{of}):** For voltage-series feedback, R_o decreases.

$$R_{of} = \frac{R_o}{1 + A\beta} = \frac{40 \text{ k}\Omega}{10} = 4 \text{ k}\Omega$$

4.5 Advantages and Disadvantages of Negative Feedback

4.5.1 Advantages

1. Stabilizes the voltage gain against variations in temperature and active device parameters.
2. Increases the bandwidth (improves frequency response).
3. Reduces harmonic distortion and noise.
4. Modifies input and output impedances to desired values (e.g. higher input impedance and lower output impedance for voltage amplifiers).

4.5.2 Disadvantages

1. Reduces the overall voltage gain of the amplifier.
2. May lead to instability (oscillations) if the feedback becomes positive at high frequencies due to phase shifts.

4.6 Emitter Follower

The emitter follower is a common-collector amplifier configuration that heavily utilizes negative feedback (specifically voltage-series feedback). The output is taken from the emitter terminal, and it "follows" the input voltage.

Methodology:

Emitter Follower Parameter Computation For an emitter follower using approximate h-parameter model ($h_{re} \approx 0, h_{oe} \approx 0$):

1. **Voltage Gain (A_v):** The voltage gain is always slightly less than unity.

$$A_v \approx \frac{(1 + h_{fe})R_E}{h_{ie} + (1 + h_{fe})R_E} \approx 1$$

2. **Input Impedance (R_i):** Results in a very high input impedance.

$$R_i = h_{ie} + (1 + h_{fe})R_E$$

3. **Output Impedance (R_o):** Results in a very low output impedance. Let R_s be the source resistance.

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}}$$

Worked Example:

Emitter Follower Characteristics An emitter follower circuit has a load resistance $R_E = 2$ kΩ, source resistance $R_s = 1$ kΩ, and transistor parameters $h_{ie} = 1.5$ kΩ, $h_{fe} = 100$. Calculate the voltage gain, input impedance, and output impedance.

Solution:

1. **Identify given values:** $R_E = 2000\ \Omega$, $R_s = 1000\ \Omega$, $h_{ie} = 1500\ \Omega$, $h_{fe} = 100$.

2. **Calculate Input Impedance (R_i):**

$$R_i = h_{ie} + (1 + h_{fe})R_E$$

$$R_i = 1500 + (1 + 100) \times 2000 = 1500 + 101 \times 2000$$

$$R_i = 1500 + 202000 = 203500\ \Omega = 203.5\ \text{k}\Omega$$

3. **Calculate Voltage Gain (A_v):**

$$A_v = \frac{(1 + h_{fe})R_E}{R_i}$$

$$A_v = \frac{101 \times 2000}{203500} = \frac{202000}{203500} \approx 0.9926$$

4. **Calculate Output Impedance (R_o):**

$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}}$$

$$R_o = \frac{1500 + 1000}{101} = \frac{2500}{101} \approx 24.75\ \Omega$$

The voltage gain is ~ 0.99, input impedance is 203.5 kΩ, and output impedance is 24.75 Ω.

CHAPTER 5
Oscillators

5.1 Positive Feedback

In an oscillator, a portion of the output signal is fed back to the input in phase with the original input signal. This is known as positive feedback. The overall gain of the system increases due to positive feedback, eventually leading to sustained oscillations if specific conditions are met.

Methodology:

Calculating Closed-Loop Gain with Positive Feedback To determine the closed-loop gain when positive feedback is applied:

1. Identify the open-loop gain A (gain without feedback).
2. Identify the feedback factor β (fraction of output fed back to the input).
3. Calculate the closed-loop gain A_f using the formula:

$$A_f = \frac{A}{1 - A\beta}$$

Worked Example:

Closed-Loop Gain Calculation An amplifier has an open-loop gain of 100. A positive feedback loop is introduced with a feedback fraction of 0.005. Calculate the closed-loop gain. If the feedback fraction is increased to 0.01, what happens to the gain?
Solution:

1. **Given:** Open-loop gain $A = 100$, initial feedback factor $\beta_1 = 0.005$, new feedback factor $\beta_2 = 0.01$.
2. **Calculate A_{f1}:**
$$A_{f1} = \frac{A}{1 - A\beta_1} = \frac{100}{1 - 100(0.005)} = \frac{100}{1 - 0.5} = \frac{100}{0.5} = 200$$
3. **Calculate A_{f2}:**
$$A_{f2} = \frac{A}{1 - A\beta_2} = \frac{100}{1 - 100(0.01)} = \frac{100}{1 - 1} = \frac{100}{0} = \infty$$
When $A\beta = 1$, the closed-loop gain becomes infinite and the circuit acts as an oscillator.

5.2 Barkhausen's Criteria

Barkhausen's criteria state the fundamental conditions for a circuit to operate as an oscillator, generating a continuous output waveform without any external input signal.

Methodology:

Applying Barkhausen Criteria For a feedback circuit to sustain continuous oscillations at a specific frequency:

1. **Magnitude Condition:** The loop gain magnitude must be equal to or greater than unity:

$$|A\beta| \geq 1$$

(For oscillations to start, $|A\beta| > 1$. For steady sustained oscillations, $|A\beta| = 1$).

2. **Phase Condition:** The total phase shift around the closed loop must be $0°$ or an integer multiple of $360°$:

$$\angle A\beta = 0° \text{ or } 360° \text{ or } n \times 360°$$

Worked Example:

Checking Oscillation Conditions In a feedback network the open-loop gain of the amplifier is $A = -50$. The feedback network has a transfer function $\beta = -0.025$. Determine if the circuit will oscillate.
Solution:

1. **Calculate Loop Gain Magnitude:**

$$|A\beta| = |(-50) \times (-0.025)| = 1.25$$

Since $|A\beta| = 1.25 > 1$, the magnitude condition for starting oscillations is satisfied.

2. **Check Phase Condition:** The amplifier has a negative gain indicating a phase shift of $180°$. The feedback network also has a negative transfer function indicating another phase shift of $180°$. Total loop phase shift $= 180° + 180° = 360°$. The phase condition is satisfied.

3. **Conclusion:** Both conditions of Barkhausen's criteria are satisfied. The circuit will start and sustain oscillations.

5.3 Overall Gain

The overall gain or closed-loop gain of an oscillator becomes theoretically infinite when Barkhausen's criteria are met. This means an output is produced without any external input.

Methodology:

Determining Required Gain for Sustained Oscillation To analyze the gain requirements for an oscillator:

1. Determine the feedback factor β of the circuit.
2. Ensure the phase condition ($360°$ loop shift) is satisfied.
3. Apply the magnitude condition $|A\beta| \geq 1$.
4. Solve for the minimum required amplifier gain $A \geq \frac{1}{|\beta|}$.

Worked Example:

Gain Adjustment for Sustained Oscillation A feedback oscillator has an amplifier with an adjustable gain A. The feedback network provides an attenuation of $\beta = 1/29$ with a phase shift of $180°$. The amplifier also introduces a phase shift of $180°$. Find the minimum gain A required for sustained oscillations.
Solution:

1. **Identify total phase shift:** Total phase shift $= 180°(\text{amplifier}) + 180°(\text{feedback network}) = 360°$. Phase condition is met.

2. **Apply magnitude condition:** For sustained oscillations $|A\beta| \geq 1$.
3. **Calculate required gain A:**

$$A \geq \frac{1}{\beta} = \frac{1}{1/29} = 29$$

The minimum gain A required is 29.

5.4 Tank Circuit

A tank circuit consists of an inductor (L) and a capacitor (C) connected in parallel. It is the frequency-determining component in LC oscillators. The circuit oscillates by exchanging energy between the capacitor's electric field and the inductor's magnetic field.

Methodology:

Analyzing Parallel LC Tank Circuits To find the resonant frequency of a tank circuit:

1. Identify the inductance L (in Henrys) and capacitance C (in Farads).
2. Calculate the resonant frequency f_r where inductive reactance equals capacitive reactance ($X_L = X_C$):

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

Worked Example:

Tank Circuit Resonant Frequency Calculation A tank circuit contains an inductor of 50 μH and a capacitor of 200 pF. Calculate its resonant frequency.
Solution:

1. **Identify values:** $L = 50 \times 10^{-6}$ H, $C = 200 \times 10^{-12}$ F.
2. **Calculate resonant frequency f_r:**

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

$$f_r = \frac{1}{2\pi\sqrt{(50 \times 10^{-6})(200 \times 10^{-12})}}$$

$$f_r = \frac{1}{2\pi\sqrt{10000 \times 10^{-18}}} = \frac{1}{2\pi\sqrt{1 \times 10^{-14}}} = \frac{1}{2\pi \times 10^{-7}}$$

$$f_r = \frac{10^7}{2\pi} \approx 1.59 \times 10^6 \text{ Hz} = 1.59 \text{ MHz}$$

5.5 Types of Oscillators

Oscillators are broadly classified based on the components used in their frequency-determining network and the shape of the generated waveform:

- **LC Oscillators:** Use inductors and capacitors (e.g. Hartley Colpitts). Primarily used for high frequencies (RF).
- **RC Oscillators:** Use resistors and capacitors (e.g. Phase Shift Wien Bridge). Primarily used for low frequencies (Audio).
- **Crystal Oscillators:** Use piezoelectric crystals for highly stable reference frequencies.

- **Relaxation Oscillators:** Use non-linear devices (like UJT) to produce non-sinusoidal waves (e.g. square triangular sawtooth).

5.6 LC Oscillators

LC oscillators use a tuned LC circuit. Two common types are the Hartley and Colpitts oscillators.

Methodology:

Frequency of Hartley and Colpitts Oscillators To find the frequency of LC oscillators:

1. **Hartley Oscillator:** Uses two tapped inductors (L_1 and L_2) and one capacitor (C).
   - Find equivalent inductance: $L_{eq} = L_1 + L_2 + 2M$ (where M is mutual inductance. If not given assume $M = 0$).
   - Frequency: $f = \frac{1}{2\pi\sqrt{L_{eq}C}}$
2. **Colpitts Oscillator:** Uses two tapped capacitors (C_1 and C_2) and one inductor (L).
   - Find equivalent capacitance: $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$
   - Frequency: $f = \frac{1}{2\pi\sqrt{LC_{eq}}}$

Worked Example:

Hartley Oscillator Frequency In a Hartley oscillator the tank circuit has $L_1 = 1$ mH, $L_2 = 100\,\mu$H, and $C = 50$ pF. Calculate the frequency of oscillation assuming zero mutual inductance.
Solution:

1. **Identify values:** $L_1 = 1 \times 10^{-3}$ H, $L_2 = 100 \times 10^{-6}$ H $= 0.1 \times 10^{-3}$ H, $C = 50 \times 10^{-12}$ F.
2. **Calculate L_{eq}:**
$$L_{eq} = L_1 + L_2 = 1 \times 10^{-3} + 0.1 \times 10^{-3} = 1.1 \times 10^{-3} \text{ H}$$
3. **Calculate Frequency:**
$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} = \frac{1}{2\pi\sqrt{(1.1 \times 10^{-3})(50 \times 10^{-12})}}$$
$$f = \frac{1}{2\pi\sqrt{55 \times 10^{-15}}} \approx \frac{1}{2\pi(2.345 \times 10^{-7})} \approx 678.6 \text{ kHz}$$

Worked Example:

Colpitts Oscillator Design A Colpitts oscillator is required to oscillate at 1 MHz. The inductor is $100\,\mu$H. If $C_1 = 1000$ pF, calculate the required value of C_2.
Solution:

1. **Identify values:** $f = 10^6$ Hz, $L = 100 \times 10^{-6}$ H, $C_1 = 1000 \times 10^{-12}$ F.
2. **Calculate required C_{eq}:**
$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \implies f^2 = \frac{1}{4\pi^2 LC_{eq}}$$
$$C_{eq} = \frac{1}{4\pi^2 f^2 L} = \frac{1}{4\pi^2 (10^6)^2 (100 \times 10^{-6})} = \frac{1}{4\pi^2 (10^{12})(10^{-4})}$$
$$C_{eq} = \frac{1}{4\pi^2 \times 10^8} \approx 2.533 \times 10^{-10} \text{ F} = 253.3 \text{ pF}$$

3. **Calculate C_2:** Since $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$, we have:

$$\frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}$$

$$\frac{1}{253.3} = \frac{1}{1000} + \frac{1}{C_2}$$

$$\frac{1}{C_2} = \frac{1}{253.3} - \frac{1}{1000} \approx 0.003948 - 0.001 = 0.002948 \text{ pF}^{-1}$$

$$C_2 = \frac{1}{0.002948} \approx 339 \text{ pF}$$

5.7 RC Oscillators

RC oscillators use resistors and capacitors for the feedback network. Common types are the Phase Shift Oscillator and the Wien Bridge Oscillator.

Methodology:

RC Oscillator Frequency

1. **RC Phase Shift Oscillator:**
   - Consists of three identical RC stages providing a 180° phase shift.
   - Frequency of oscillation: $f = \frac{1}{2\pi RC\sqrt{6}}$
2. **Wien Bridge Oscillator:**
   - Uses a lead-lag network providing a 0° phase shift at resonance.
   - Frequency of oscillation: $f = \frac{1}{2\pi RC}$

Worked Example:

RC Phase Shift Oscillator Frequency In an RC phase shift oscillator $R = 10\ \text{k}\Omega$ and $C = 0.001\,\mu\text{F}$. Calculate the frequency of oscillation.
Solution:

1. **Identify values:** $R = 10 \times 10^3\,\Omega$, $C = 0.001 \times 10^{-6}$ F $= 10^{-9}$ F.
2. **Calculate Frequency:**

$$f = \frac{1}{2\pi RC\sqrt{6}}$$

$$f = \frac{1}{2\pi(10 \times 10^3)(10^{-9})\sqrt{6}}$$

$$f = \frac{1}{2\pi(10^{-5})(2.449)}$$

$$f \approx \frac{1}{1.539 \times 10^{-4}} \approx 6497 \text{ Hz or } 6.497 \text{ kHz}$$

Worked Example:

Wien Bridge Oscillator Component Selection Design the frequency-determining network of a Wien bridge oscillator to generate a frequency of 1 kHz. Choose $C = 0.01\,\mu\text{F}$.
Solution:

1. **Identify values:** $f = 1000$ Hz, $C = 0.01 \times 10^{-6}$ F $= 10^{-8}$ F.
2. **Use Frequency Formula:**
$$f = \frac{1}{2\pi RC}$$
3. **Solve for R:**
$$R = \frac{1}{2\pi fC}$$
$$R = \frac{1}{2\pi(1000)(10^{-8})} = \frac{1}{2\pi \times 10^{-5}}$$
$$R \approx \frac{100000}{6.283} \approx 15915\,\Omega = 15.9\ \text{k}\Omega$$

5.8 Crystal Oscillator

Crystal oscillators use a quartz crystal to provide extremely stable resonant frequencies due to the piezoelectric effect. The crystal behaves like a series RLC circuit (motional parameters) in parallel with a mounting capacitance C_m.

Methodology:

Crystal Oscillator Frequencies A crystal has two closely spaced resonant frequencies:

1. **Series Resonant Frequency (f_s):** Occurs when the motional inductance L and motional capacitance C resonate. The impedance is minimum.
$$f_s = \frac{1}{2\pi\sqrt{LC}}$$
2. **Parallel Resonant Frequency (f_p):** Occurs when L resonates with the equivalent series capacitance of C and the mounting capacitance C_m. The impedance is maximum.
$$C_{eq} = \frac{C \cdot C_m}{C + C_m}$$
$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

Worked Example:

Crystal Oscillator Series and Parallel Frequencies A quartz crystal has the following parameters: $L = 0.4$ H, $C = 0.08$ pF, and mounting capacitance $C_m = 2$ pF. Calculate its series and parallel resonant frequencies.
Solution:

1. **Calculate Series Resonant Frequency (f_s):**
$$f_s = \frac{1}{2\pi\sqrt{LC}}$$
$$f_s = \frac{1}{2\pi\sqrt{0.4 \times 0.08 \times 10^{-12}}} = \frac{1}{2\pi\sqrt{0.032 \times 10^{-12}}} = \frac{1}{2\pi(5.657 \times 10^{-7})}$$
$$f_s \approx 281.3\ \text{kHz}$$
2. **Calculate Equivalent Capacitance (C_{eq}):**
$$C_{eq} = \frac{C \cdot C_m}{C + C_m} = \frac{0.08 \times 2}{0.08 + 2}\ \text{pF} = \frac{0.16}{2.08}\ \text{pF} \approx 0.0769\ \text{pF}$$

3. **Calculate Parallel Resonant Frequency (f_p):**

$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}}$$

$$f_p = \frac{1}{2\pi\sqrt{0.4 \times 0.0769 \times 10^{-12}}} = \frac{1}{2\pi\sqrt{0.03076 \times 10^{-12}}} = \frac{1}{2\pi(5.546 \times 10^{-7})}$$

$$f_p \approx 286.9 \text{ kHz}$$

5.9 UJT

A Unijunction Transistor (UJT) is a three-terminal semiconductor device exhibiting negative resistance, making it ideal for use in relaxation oscillators.

Methodology:

UJT Parameters and Peak Voltage To analyze UJT characteristics:

1. **Interbase Resistance (R_{BB}):** The total resistance between base 1 (B_1) and base 2 (B_2).

$$R_{BB} = R_{B1} + R_{B2}$$

2. **Intrinsic Stand-Off Ratio (η):** The voltage division ratio formed by the internal resistances.

$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}}$$

3. **Peak Voltage (V_P):** The emitter voltage at which the UJT fires (turns on). V_D is the forward voltage drop of the internal diode (typically 0.7 V). V_{BB} is the applied interbase voltage.

$$V_P = \eta V_{BB} + V_D$$

Worked Example:

Calculating UJT Peak Voltage A UJT has an intrinsic stand-off ratio $\eta = 0.6$ and an interbase voltage $V_{BB} = 15$ V. If the diode voltage drop is 0.7 V, calculate the peak point voltage V_P.
Solution:

1. **Identify values:** $\eta = 0.6$, $V_{BB} = 15$ V, $V_D = 0.7$ V.

2. **Calculate Peak Voltage V_P:**

$$V_P = \eta V_{BB} + V_D$$

$$V_P = (0.6)(15) + 0.7 = 9 + 0.7 = 9.7 \text{ V}$$

The UJT will trigger when the emitter voltage reaches 9.7 V.

5.10 UJT as Relaxation Oscillator

A UJT relaxation oscillator generates a non-sinusoidal waveform. It typically produces a sawtooth wave across the capacitor and sharp voltage spikes at the bases.

Methodology:

UJT Relaxation Oscillator Frequency To calculate the frequency of oscillation for a UJT relaxation oscillator:

1. An external RC circuit determines the charging time of the capacitor C through resistor R.

2. The capacitor charges until its voltage reaches V_P, at which point the UJT discharges it rapidly.
3. The period T of the oscillation is given by:

$$T = RC \ln\left(\frac{1}{1-\eta}\right)$$

4. The frequency of oscillation f is the reciprocal of the period:

$$f = \frac{1}{T}$$

Worked Example:

UJT Relaxation Oscillator Frequency Calculation A UJT relaxation oscillator has $R = 50\ \text{k}\Omega$, $C = 0.1\,\mu\text{F}$, and an intrinsic stand-off ratio $\eta = 0.63$. Calculate the frequency of oscillation.

Solution:

1. **Identify values:** $R = 50 \times 10^3\,\Omega$, $C = 0.1 \times 10^{-6}$ F, $\eta = 0.63$.
2. **Calculate Period T:**

$$T = RC \ln\left(\frac{1}{1-\eta}\right)$$

$$T = (50 \times 10^3)(0.1 \times 10^{-6}) \ln\left(\frac{1}{1-0.63}\right)$$

$$T = 5 \times 10^{-3} \ln\left(\frac{1}{0.37}\right)$$

$$T = 0.005 \times \ln(2.7027) \approx 0.005 \times 0.994 \approx 0.00497\ \text{s} \approx 4.97\ \text{ms}$$

3. **Calculate Frequency f:**

$$f = \frac{1}{T} = \frac{1}{0.00497} \approx 201.2\ \text{Hz}$$

Formulae

Appendix: Key Formulae

This appendix provides a quick reference to the key formulae and mathematical relationships discussed in this book.

Unit 1: Field Effect Transistors (FETs)

JFET Parameters

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 \quad \text{(Drain Current in Saturation Region)}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) \quad \text{(Transconductance)}$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \quad \text{(Maximum Transconductance)}$$

$$R_0 = \frac{|V_P|}{2I_{DSS}} \quad \text{(Ohmic Resistance at } V_{GS} = 0\text{)}$$

$$r_d = \frac{R_0}{1 - \frac{V_{GS}}{V_P}} \quad \text{(Drain Resistance)}$$

MOSFET Parameters

$$I_D = k(V_{GS} - V_T)^2 \quad \text{(Drain Current for E-MOSFET)}$$

$$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2} \quad \text{(Conduction Parameter)}$$

General Biasing

$$I_B = \frac{I_C}{\beta} \quad \text{(Base Current in BJT)}$$

$$I_G = \frac{V_{GS}}{R_{in}} \quad \text{(Gate Current in FET)}$$

Unit 2: Transistor Biasing and Thermal Stabilization

BJT Biasing

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} \quad \text{(Fixed Bias Base Current)}$$
$$I_C = \beta I_B \quad \text{(Collector Current)}$$
$$I_E = I_B + I_C \approx I_C \quad \text{(Emitter Current)}$$
$$V_{CE} = V_{CC} - I_C R_C \quad \text{(Collector-Emitter Voltage)}$$
$$V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E) \quad \text{(With Emitter Resistor)}$$
$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} \quad \text{(Saturation Current)}$$
$$V_{CE(cutoff)} = V_{CC} \quad \text{(Cutoff Voltage)}$$

Voltage Divider Bias

$$V_{TH} = V_{CC}\frac{R_2}{R_1 + R_2} \quad \text{(Thevenin Equivalent Voltage)}$$
$$R_{TH} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1 + R_2} \quad \text{(Thevenin Equivalent Resistance)}$$
$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E} \quad \text{(Base Current)}$$

Stability Factors

$$I_C = \beta I_B + (1 + \beta) I_{CBO} \quad \text{(General Collector Current Equation)}$$
$$S = \frac{\partial I_C}{\partial I_{CBO}} = \frac{1 + \beta}{1 - \beta\left(\frac{\partial I_B}{\partial I_C}\right)} \quad \text{(Stability Factor Definition)}$$
$$S_{\text{fixed}} = 1 + \beta \quad \text{(Fixed Bias Stability Factor)}$$
$$S_{\text{divider}} = \frac{(1 + \beta)\left(1 + \frac{R_{TH}}{R_E}\right)}{1 + \beta + \frac{R_{TH}}{R_E}} \quad \text{(Voltage Divider Bias Stability Factor)}$$

Thermal Stabilization

$$P_D \approx V_{CE} I_C \quad \text{(Power Dissipation)}$$
$$T_J = T_A + \theta_{JA} P_D \quad \text{(Junction Temperature)}$$
$$\theta_{JA} = \frac{T_{J(max)} - T_A}{P_D} \quad \text{(Junction-to-Ambient Thermal Resistance)}$$
$$\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} \quad \text{(Total Thermal Resistance)}$$
$$\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}} \quad \text{(Condition for Thermal Stability)}$$

Unit 3: Amplifiers and Frequency Response

Gain Definitions

$$A_v = \frac{V_{out}}{V_{in}} \quad \text{(Voltage Gain)}$$
$$A_i = \frac{I_{out}}{I_{in}} \quad \text{(Current Gain)}$$
$$A_p = \frac{P_{out}}{P_{in}} = A_v \times A_i \quad \text{(Power Gain)}$$
$$A_{v(dB)} = 20\log_{10}(|A_v|) \quad \text{(Voltage Gain in dB)}$$
$$A_{p(dB)} = 10\log_{10}(A_p) \quad \text{(Power Gain in dB)}$$
$$A_v = 10^{\frac{A_{v(dB)}}{20}} \quad \text{(Linear Voltage Gain from dB)}$$

Multistage Amplifiers

$$A_{v(total)} = A_{v1} \times A_{v2} \times \cdots \times A_{vn} \quad \text{(Total Voltage Gain)}$$
$$A_{v(total)dB} = A_{v1(dB)} + A_{v2(dB)} + \cdots + A_{vn(dB)} \quad \text{(Total Voltage Gain in dB)}$$

Small Signal AC Parameters

$$r_e \approx \frac{26\text{ mV}}{I_E} \quad \text{(Dynamic Emitter Resistance)}$$
$$g_m = \frac{1}{r_e} \quad \text{(Transconductance)}$$
$$A_v = -g_m r_L = -\frac{r_L}{r_e} \quad \text{(Voltage Gain for Common Emitter)}$$
$$r_L = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L} \quad \text{(AC Load Resistance)}$$

Frequency Response

$$BW = f_H - f_L \quad \text{(Bandwidth)}$$
$$A_{v(cutoff)} = \frac{A_{v(mid)}}{\sqrt{2}} \quad \text{(Gain at Cutoff Frequencies)}$$
$$X_C = \frac{1}{2\pi f C} \quad \text{(Capacitive Reactance)}$$

Cutoff Frequencies (RC Coupled)

$$f_{L1} = \frac{1}{2\pi(R_s + R_{in})C_{C1}} \quad \text{(Input Coupling Capacitor Lower Cutoff)}$$
$$f_{L2} = \frac{1}{2\pi(R_{out} + R_L)C_{C2}} \quad \text{(Output Coupling Capacitor Lower Cutoff)}$$
$$f_{LE} = \frac{1}{2\pi R_{eqE} C_E} \quad \text{(Emitter Bypass Capacitor Lower Cutoff)}$$

Cascaded Stages Frequency Response

$$f_{L(new)} = \frac{f_L}{\sqrt{2^{1/n} - 1}} \quad \text{(Lower Cutoff for } n \text{ identical stages)}$$
$$f_{H(new)} = f_H \times \sqrt{2^{1/n} - 1} \quad \text{(Upper Cutoff for } n \text{ identical stages)}$$

Transformer Coupling

$$n = \frac{N_p}{N_s} \quad \text{(Turns Ratio)}$$
$$R'_L = n^2 R_L = \left(\frac{N_p}{N_s}\right)^2 R_L \quad \text{(Reflected Load Resistance)}$$
$$n = \sqrt{\frac{R_{out}}{R_L}} \quad \text{(Turns Ratio for Maximum Power Transfer)}$$

Unit 4: Feedback Amplifiers

General Feedback Relationships

$$A_f = \frac{A}{1 + A\beta} \quad \text{(Closed-loop Gain for Negative Feedback)}$$
$$1 + A\beta = \frac{A}{A_f} \quad \text{(Amount of Feedback or Desensitivity Factor)}$$
$$A_f = \frac{A}{1 - A\beta} \quad \text{(Closed-loop Gain for Positive Feedback)}$$

Effects of Negative Feedback

$$BW_f = BW_{open} \times (1 + A\beta) \quad \text{(Bandwidth with Feedback)}$$
$$D_f = \frac{D_{open}}{1 + A\beta} \quad \text{(Distortion with Feedback)}$$
$$N_f = \frac{N_{open}}{1 + A\beta} \quad \text{(Noise with Feedback)}$$
$$\frac{dA_f}{A_f} = \frac{1}{1 + A\beta}\frac{dA}{A} \quad \text{(Gain Stability)}$$

Impedance with Feedback

$$R_{if} = R_i(1 + A\beta) \quad \text{(Input Impedance for Series Feedback)}$$
$$R_{of} = \frac{R_o}{1 + A\beta} \quad \text{(Output Impedance for Voltage Feedback)}$$

Emitter Follower (Common Collector)

$$R_i = h_{ie} + (1 + h_{fe})R_E \quad \text{(Input Resistance)}$$
$$R_o = \frac{h_{ie} + R_s}{1 + h_{fe}} \quad \text{(Output Resistance)}$$
$$A_v = \frac{(1 + h_{fe})R_E}{h_{ie} + (1 + h_{fe})R_E} \approx 1 \quad \text{(Voltage Gain)}$$

Unit 5: Oscillators

Barkhausen Criterion

$$|A\beta| \geq 1 \quad \text{(Loop Gain Condition for Oscillation)}$$
$$\angle A\beta = 0°, 360°, \ldots, n \times 360° \quad \text{(Phase Shift Condition)}$$

RC Oscillators

$$f = \frac{1}{2\pi RC\sqrt{6}} \quad \text{(Frequency of RC Phase Shift Oscillator)}$$
$$f = \frac{1}{2\pi RC} \quad \text{(Frequency of Wien Bridge Oscillator)}$$

LC Oscillators

$$f_r = \frac{1}{2\pi\sqrt{LC}} \quad \text{(Resonant Frequency of LC Tank)}$$
$$f = \frac{1}{2\pi\sqrt{L_{eq}C}} \quad \text{(Frequency of Hartley Oscillator, } L_{eq} = L_1 + L_2\text{)}$$
$$f = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad \text{(Frequency of Colpitts Oscillator, } \frac{1}{C_{eq}} = \frac{1}{C_1} + \frac{1}{C_2}\text{)}$$

Crystal Oscillators

$$f_s = \frac{1}{2\pi\sqrt{LC}} \quad \text{(Series Resonant Frequency)}$$
$$f_p = \frac{1}{2\pi\sqrt{LC_{eq}}} \quad \text{(Parallel Resonant Frequency, } C_{eq} = \frac{C \cdot C_m}{C + C_m}\text{)}$$

UJT Relaxation Oscillator

$$T = RC \ln\left(\frac{1}{1-\eta}\right) \quad \text{(Time Period of Oscillation)}$$
$$f = \frac{1}{T} \quad \text{(Frequency of Oscillation)}$$
$$\eta = \frac{R_{B1}}{R_{B1} + R_{B2}} = \frac{R_{B1}}{R_{BB}} \quad \text{(Intrinsic Stand-off Ratio)}$$
$$V_P = \eta V_{BB} + V_D \quad \text{(Peak Voltage)}$$
$$R_{BB} = R_{B1} + R_{B2} \quad \text{(Interbase Resistance)}$$