# Lecture 44: Uni junction transistor(UJT) Structure, symbol, working, cha...

## Oscillators

DI02011011: Electronics Circuit and Application (ECA)

# Lecture Agenda: Unijunction Transistor Physics

- 1. Physical Structure, Doping Profile & Circuit Symbol of UJT
- 2. Equivalent Circuit Model & Intrinsic Standoff Ratio ($\eta$) Derivation
- 3. Operational Modes: Cut-off Region, Peak Point Voltage ($V_P$), and Triggering
- 4. Hole Injection Mechanism & Conductivity Modulation in Base-1 Region
- 5. Voltage-Current (V-I) Characteristic Curve Analysis (Cut-off, Negative Resistance, Saturation)
- 6. Temperature Compensation Techniques for Peak Voltage $V_P$ using Base-2 Resistor $R_2$
- 7. Programmable Unijunction Transistor (PUT): Construction, Operation & Design Formulas

# Physical Structure & Terminal Geometry of UJT

- Semiconductor Bar Construction: Formed on a lightly doped N-type silicon bar with two ohmic contact terminals at opposite ends designated as Base 1 ($B_1$) and Base 2 ($B_2$).
- Emitter Junction Formation: A heavily doped P-type alloyed region ($P^+$) is diffused into the N-bar closer to $B_2$ than $B_1$, creating a single PN junction.
- Asymmetrical Geometry: Physical distance from Emitter to $B_2$ is shorter than distance from Emitter to $B_1$. Unbiased channel resistance $R_{B1}$ is greater than $R_{B2}$.
- Circuit Symbol Features: Triangle arrow on Emitter terminal points inward toward N-type bar, indicating direction of forward PN junction current ($P \rightarrow N$).
- Terminal Definitions: Emitter ($E$) acts as trigger/control terminal; Base 1 ($B_1$) is output reference; Base 2 ($B_2$) is bias voltage terminal.

# UJT Equivalent Circuit & Standoff Ratio (\{}eta)

- Interbase Resistance ($R_{BB}$): Total resistance of N-bar between $B_1$ and $B_2$ with Emitter open-circuited ($I_E = 0$): $R_{BB} = R_{B1} + R_{B2}$ (typical values 4.7 k$\Omega$ – 10.0 k$\Omega$).
- Internal Potential Divider: Voltage at internal node $N$ (cathode of PN junction) relative to $B_1$: $V_N = V_{BB} \times \frac{R_{B1}}{R_{B1}+R_{B2}} = \eta V_{BB}$.
- Intrinsic Standoff Ratio ($\eta$): Dimensionless structural parameter defined as $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} = \frac{R_{B1}}{R_{BB}}$. Typical range $\eta = 0.51$ to $0.82$.
- Equivalent Circuit Model: Represented electrically as an ideal PN junction diode $D_E$ connected to internal node $N$ between fixed resistor $R_{B2}$ and variable resistor $R_{B1}$.

# Operational Modes: Cut-Off Region & Triggering

- Cut-Off State ($V_E < V_P$): When applied Emitter voltage $V_E$ is less than node voltage $V_N = \eta V_{BB} + V_D$ (where $V_D \approx 0.6\ \text{V} - 0.7\ \text{V}$ is PN junction diode drop), diode $D_E$ is reverse biased.
- Reverse Leakage Current: Emitter current $I_E = -I_{EO}$ (minority carrier reverse leakage, $\mu$A range). UJT presents high input impedance ($M\Omega$) and remains OFF.
- Peak Point Voltage ($V_P$): Threshold firing voltage required to forward-bias diode $D_E$: $V_P = \eta V_{BB} + V_D$.
- Peak Point Current ($I_P$): Minimum emitter current required to trigger UJT from cut-off into negative resistance region (typically $1.0\ \mu\text{A} - 10.0\ \mu\text{A}$).

# Negative Resistance & Conductivity Modulation

- Forward Conduction Triggering: When $V_E \geq V_P$, diode $D_E$ becomes forward biased, injecting holes ($P^+$) into the lightly doped N-type $B_1$ region.
- Conductivity Modulation Mechanism: Injected minority carriers (holes) attract majority carriers (electrons) into the $B_1$ channel to maintain charge neutrality, drastically increasing free carrier concentration.
- Collapse of $R_{B1}$: Increased conductivity causes resistance $R_{B1}$ to drop rapidly from several k$\Omega$ down to $20\ \Omega - 50\ \Omega$.
- Negative Resistance Dynamic: As emitter current $I_E$ increases, voltage drop across $R_{B1}$ decreases ($V_E$ drops while $I_E$ rises), creating a negative differential resistance region where $R_{diff} = \frac{dV_E}{dI_E} < 0$.

# V-I Characteristic Curve Regions

- Region 1: Cut-off Region ($V_E < V_P$): High impedance state, $I_E \approx 0$. Ends abruptly at Peak Point $(V_P, I_P)$.
- Region 2: Negative Resistance Region ($V_P > V_E > V_V$): Dynamic conductivity modulation occurs. Emitter voltage $V_E$ decreases exponentially as emitter current $I_E$ increases. Ends at Valley Point $(V_V, I_V)$.
- Region 3: Saturation Region ($V_E < V_V, I_E > I_V$): Base-1 region becomes fully flooded with charge carriers; $R_{B1}$ reaches minimum limit $R_{B1,sat}$. Further increase in $I_E$ causes $V_E$ to rise slowly ($R_{diff} > 0$), behaving as a low-resistance ohmic conductor.
- Key Parameter Thresholds: Valley Voltage ($V_V \approx 1.5\ \text{V} - 3.0\ \text{V}$), Valley Current ($I_V \approx 1.0\ \text{mA} - 10.0\ \text{mA}$).

# UJT Parameter Calculation Example

- Problem Statement: A UJT has interbase resistance $R_{BB} = 8.0\ \text{k}\Omega$ and intrinsic standoff ratio $\eta = 0.65$. Given supply voltage $V_{BB} = 20.0\ \text{V}$ and PN junction drop $V_D = 0.7\ \text{V}$, calculate: (a) Unbiased base resistances $R_{B1}$ and $R_{B2}$, (b) Peak point voltage $V_P$, (c) Interbase leakage current $I_{BB}$ prior to turn-on.
- Step 1: Calculate $R_{B1}$: $R_{B1} = \eta R_{BB} = 0.65 \times 8.0\ \text{k}\Omega = 5.2\ \text{k}\Omega$.
- Step 2: Calculate $R_{B2}$: $R_{B2} = R_{BB} - R_{B1} = 8.0\ \text{k}\Omega - 5.2\ \text{k}\Omega = 2.8\ \text{k}\Omega$.
- Step 3: Calculate Peak Point Voltage ($V_P$):
  $V_P = \eta V_{BB} + V_D = (0.65 \times 20.0\ \text{V}) + 0.7\ \text{V} = 13.0\ \text{V} + 0.7\ \text{V} = 13.7\ \text{V}$.
- Step 4: Compute Interbase Leakage Current ($I_{BB}$): $I_{BB} = \frac{V_{BB}}{R_{BB}} = \frac{20.0\ \text{V}}{8.0\ \text{k}\Omega} = 2.5\ \text{mA}$.

# Temperature Compensation of Peak Voltage V_P

- Temperature Drift Mechanisms: Peak voltage $V_P = \eta V_{BB} + V_D(T)$. PN junction voltage $V_D$ decreases with temperature by $\approx -2.2$ mV/°C, while interbase resistance $R_{BB}$ increases with temperature (positive temperature coefficient $+0.8\%/°C$).
- Compensation Circuit Topology: Place an external resistor $R_2$ in series with Base 2 terminal ($B_2$).
- Modified Base Voltage ($V'_{BB}$): $V'_{BB} = V_{CC} \times \frac{R_{BB}}{R_{BB}+R_2}$. As temperature rises, $R_{BB}$ increases, raising $V'_{BB}$ and compensating for the drop in $V_D$.
- Optimal Compensation Resistor Equation: $R_2 \approx \frac{0.7R_{BB}}{\eta V_{CC}}$ or empirically $R_2 \approx \frac{10000}{\eta V_{CC}}$ for silicon UJTs.

# Programmable Unijunction Transistor (PUT)

- Limitation of Standard UJT: Intrinsic standoff ratio $\eta$ is fixed permanently during silicon wafer fabrication.
- PUT Structure & Terminals: Four-layer PNPN device (similar to an SCR) featuring three terminals: Anode ($A$), Cathode ($K$), and Gate ($G$) connected to N-region adjacent to Anode.
- Programmable Standoff Ratio ($\eta$): Set externally using two resistors ($R_A, R_B$) forming a voltage divider at Gate terminal: $\eta = \frac{R_B}{R_A+R_B}$.
- PUT Firing Voltage ($V_P$): $V_P = V_G + V_D = \eta V_{GG} + V_D = \left(\frac{R_B}{R_A+R_B}\right) V_{GG} + V_D$.
- Superior Performance Characteristics: Lower peak current ($I_P < 0.1\ \mu$A), faster switching speeds, adjustable peak firing voltage.

# PUT Parameter Design Example

- Problem Statement: Design a PUT gate voltage divider to establish an effective standoff ratio $\eta = 0.70$ with supply voltage $V_{GG} = 15.0$ V and equivalent gate resistance $R_G = 10.0$ kΩ. Calculate peak firing voltage $V_P$ (assume $V_D = 0.6$ V).
- Step 1: Set Up Gate Bias Equations:
  $\eta = \frac{R_B}{R_A+R_B} = 0.70 \Rightarrow R_B = 0.70(R_A + R_B) \Rightarrow R_A = \frac{0.30}{0.70} R_B = 0.4286 R_B$.
- Step 2: Apply Gate Resistance Constraint ($R_G = R_A \parallel R_B$):
  $R_G = \frac{R_A R_B}{R_A+R_B} = 0.70 R_A = 0.70(0.4286 R_B) = 0.30 R_B = 10.0$ kΩ.
- Step 3: Solve for $R_B$ and $R_A$: $R_B = \frac{10.0 \text{ k}\Omega}{0.30} \approx 33.33$ kΩ; $R_A = 0.4286 \times 33.33$ kΩ $\approx 14.28$ kΩ.
- Step 4: Compute Firing Voltage ($V_P$):
  $V_P = \eta V_{GG} + V_D = (0.70 \times 15.0 \text{ V}) + 0.6 \text{ V} = 10.5 \text{ V} + 0.6 \text{ V} = 11.1 \text{ V}$.

# Comparison: UJT vs. BJT vs. FET vs. PUT

- Junction Architecture: UJT (1 PN junction, 3 terminals); BJT (2 PN junctions, 3 terminals); FET (1 channel, 3 terminals); PUT (3 PN junctions, 4 layers).
- Control Mechanism: BJT (current-controlled $I_B$); FET (voltage-controlled $V_{GS}$); UJT/PUT (voltage-triggered negative resistance threshold $V_P$).
- Terminal Designations: UJT ($E, B_1, B_2$); BJT ($B, C, E$); FET ($G, D, S$); PUT ($A, K, G$).
- Primary Circuit Applications: BJT/FET (linear analog amplification, digital switching); UJT/PUT (relaxation oscillators, SCR/TRIAC phase control triggers, timing delays).

# Summary of UJT Structure & Characteristics

- UJT is a 3-terminal, single-junction device ($E, B_1, B_2$) exhibiting negative differential resistance via conductivity modulation.
- Intrinsic Standoff Ratio $\eta = R_{B1}/R_{BB}$ $(0.51 - 0.82)$ determines peak firing voltage $V_P = \eta V_{BB} + V_D$.
- Conductivity modulation collapses $R_{B1}$ from several k$\Omega$ down to $\sim 20\ \Omega$ upon forward biasing diode $D_E$.
- Base-2 resistor $R_2$ provides temperature compensation for $V_P$; PUT allows external programming of $\eta$ using a two-resistor gate divider.

# Formula Reference & Key Equations

- Interbase Resistance: $R_{BB} = R_{B1} + R_{B2} \approx 4.7\ \text{k}\Omega - 10.0\ \text{k}\Omega$.
- Intrinsic Standoff Ratio: $\eta = \frac{R_{B1}}{R_{BB}} = \frac{R_{B1}}{R_{B1}+R_{B2}}$.
- Peak Point Firing Voltage: $V_P = \eta V_{BB} + V_D$.
- Base-2 Temperature Compensation Resistor: $R_2 \approx \frac{10000}{\eta V_{CC}}$.
- PUT Standoff Ratio & Peak Voltage: $\eta = \frac{R_B}{R_A+R_B}$, $V_P = \eta V_{GG} + V_D$.