Lecture 35: Emitter follower circuit

Feedback in amplifiers

DI02011011: Electronics Circuit and Application (ECA)

Lecture Agenda: Emitter Follower Circuit Breakdown

- Circuit Topology & DC Biasing Analysis (V_B, V_E, I_E, r_e)
- Identification of 100% Voltage-Series Feedback Mechanism ($\beta = 1.0$)
- Small-Signal Hybrid-\{}pi$ AC Equivalent Circuit Modeling
- Exact Mathematical Derivation of Voltage Gain ($A_v = \frac{R'_E}{r_e + R'_E}$)
- Exact Mathematical Derivation of Input Impedance ($R_{in} = R_B \parallel [r_\pi + (1 + \beta_0)R'_E]$)
- Exact Mathematical Derivation of Output Impedance ($R_{out} = R_E \parallel [r_e + \frac{R'_S}{1+\beta_0}]$)
- Current Gain ($A_i \approx \beta_0$) and Power Gain ($A_p \approx \beta_0$) Analysis
- High-Frequency Response & Absence of Miller Effect Multiplication
- Solved Numerical Problem: Complete DC & AC Emitter Follower Analysis
- Practical Application: High-Impedance Sensor Buffer Design
- Large-Signal Drive Limitations & Asymmetrical Cutoff Clipping
- Summary & Key Engineering Takeaways

Circuit Topology & DC Operating Point Analysis

- Circuit Configuration: Collector connected directly to V_{CC} (AC ground), input signal V_i applied to Base, output signal V_o taken from Emitter across resistor R_E.
- Base Voltage DC Bias: Voltage divider biasing gives DC Base voltage $V_B = V_{CC}\frac{R_2}{R_1+R_2}$.
- Emitter DC Voltage & Current: Emitter DC voltage $V_E = V_B - V_{BE} = V_B - 0.7$ V. DC Emitter current $I_E = \frac{V_E}{R_E}$.
- Dynamic Emitter Resistance (r_e): $r_e = \frac{V_T}{I_E} = \frac{26\text{ mV}}{I_E}$. Base-emitter dynamic resistance $r_\pi = (1+\beta_0)r_e$.

Feedback Topology: 100% Voltage-Series Feedback

- Feedback Signal Sampling: Output voltage $V_o = V_E$ is sampled directly at the emitter.
- Series Feedback Injection: 100% of output voltage V_o is fed back in series opposition to base input V_i: $v_{be} = v_i - v_o = v_b - v_e$.
- Feedback Ratio: $\beta = 1.0$ (100% voltage-series negative feedback).
- Closed-Loop Gain Formulation: Open-loop gain $A_v = g_m(R_E \parallel r_o) \gg 1$. Closed-loop voltage gain $A_{vf} = \frac{A_v}{1+1 \cdot A_v} = \frac{A_v}{1+A_v} \approx 1.0$ V/V.

Small-Signal Hybrid-\{}pi$ AC Equivalent Circuit Model

- AC Model Representation: Replace BJT with hybrid-\{}pi$model featuring base - emitter resistance r_\{}pi, dependent current source g_m v_\{}pi = \{}beta_0 i_b, and output load R_E' = R_E \{}parallel R_L$.
- Input Voltage Loop Equation: $v_i = v_\pi + v_o = i_b r_\pi + i_e R'_E$.
- Emitter AC Current Relationship: $i_e = i_b + \beta_0 i_b = (1 + \beta_0) i_b$.
- Output Voltage Equation: $v_o = i_e R'_E = (1 + \beta_0) i_b R'_E$.

Exact Derivation of Voltage Gain (A_v)

- Gain Definition: $A_v = \frac{v_o}{v_i} = \frac{(1+\beta_0) i_b R'_E}{i_b r_\pi + (1+\beta_0) i_b R'_E} = \frac{(1+\beta_0) R'_E}{r_\pi + (1+\beta_0) R'_E}$.
- Simplification with r_e: Divide numerator and denominator by $(1+\beta_0)$, substituting $r_e = \frac{r_\pi}{1+\beta_0}$:
- Final Voltage Gain Formula: $A_v = \frac{R'_E}{r_e + R'_E}$, where $R'_E = R_E \parallel R_L$.
- Gain Characteristics: Since $R'_E \gg r_e$ (typically $R'_E \approx 1\ \text{k}\Omega - 10\ \text{k}\Omega$ vs $r_e \approx 5 - 25\ \Omega$), A_v is positive (in-phase output, 0° phase shift) and slightly less than unity ($0.98 - 0.999$).

Exact Derivation of Input Impedance (R_{in})

- Base Input Impedance ($R_{in,base}$): $R_{in,base} = \frac{v_i}{i_b} = \frac{i_b r_\pi + (1+\beta_0) i_b R'_E}{i_b} = r_\pi + (1+\beta_0) R'_E$.
- Resistance Reflection Rule: Emitter resistance R'_E reflected back into the base loop is multiplied by factor $(1+\beta_0)$.
- Total Stage Input Impedance (R_{in}): Including bias resistors $R_B = R_1 \parallel R_2$:
- Final Input Impedance Formula: $R_{in} = R_B \parallel R_{in,base} = R_B \parallel [r_\pi + (1+\beta_0)(R_E \parallel R_L)]$. Reaches hundreds of $k\Omega$ to $M\Omega$.

Exact Derivation of Output Impedance (R_{out})

- Test Source Setup: Deactivate source ($v_s = 0$ V), apply test voltage v_x at emitter port, measure test current i_x.
- Base Loop Equation: $i_b = -\frac{v_x}{r_\pi + (R_S \| R_B)}$, where $R'_S = R_S \parallel R_B$.
- Emitter Test Current: $i_x = -i_b - \beta_0 i_b + \frac{v_x}{R_E} = v_x \left[\frac{1+\beta_0}{r_\pi + R'_S} + \frac{1}{R_E} \right]$.
- Final Output Impedance Formula: $R_{out} = \frac{v_x}{i_x} = R_E \parallel \left[\frac{r_\pi + R'_S}{1+\beta_0} \right] = R_E \parallel \left[r_e + \frac{R_S \| R_B}{1+\beta_0} \right]$. Yields extremely low output impedance ($10\ \Omega - 50\ \Omega$).

Current Gain (A_i) & Power Gain (A_p) Derivation

- Transistor Current Gain: $A_{i,transistor} = \frac{i_e}{i_b} = 1 + \beta_0 \approx \beta_0$ (typically $100 - 300$).
- Stage Current Gain (A_{is}): Accounting for bias divider splitting and load splitting:
- Stage Current Gain Formula: $A_{is} = \frac{i_L}{i_s} = A_{i,transistor} \cdot \frac{R_B}{R_B + R_{in,base}} \cdot \frac{R_E}{R_E + R_L}$.
- Power Gain (A_p): $A_p = A_v \cdot A_{is} \approx 1.0 \cdot A_{is} \approx \beta_0$. Although voltage gain is unity, the Emitter Follower provides high power gain driven entirely by current amplification!

High-Frequency Response & Absence of Miller Effect

- Miller Effect Review: In Common-Emitter stages, base-collector capacitance C_μ is multiplied by $(1 + |A_v|)$, creating large input Miller capacitance $C_{in,M} = C_\mu(1 + A_v)$.
- Common Collector Immunity: In Emitter Follower, Collector is AC grounded. Base-to-Collector voltage equals base voltage v_b, so C_μ is NOT multiplied by voltage gain ($A_{v,BC} = 0$).
- Base-Emitter Capacitance Bootstrapping: Base-to-emitter voltage is $v_{be} = v_i(1 - A_v) \approx 0$. Effective C_π input capacitance is bootstrapped down to $C_{\pi,in} = C_\pi(1 - A_v) \ll C_\pi$.
- Ultra-Wide Bandwidth: Complete absence of Miller multiplication grants the Emitter Follower exceptionally high bandwidth, ideal for high-speed line drivers.

Numerical Problem: Complete AC & DC Emitter Follower Analysis

- Given Parameters: $V_{CC} = 15$ V, $R_1 = 33$ kΩ, $R_2 = 33$ kΩ, $R_E = 3.3$ kΩ, load $R_L = 1$ kΩ, source $R_S = 600$ Ω, transistor $\beta_0 = 150$, $V_{BE} = 0.7$ V.
- Step 1 - DC Analysis: $V_B = 15 \times \frac{33k}{66k} = 7.5$ V. $V_E = 7.5 - 0.7 = 6.8$ V. $I_E = \frac{6.8\text{ V}}{3.3\text{ kΩ}} = 2.06$ mA. Dynamic resistance $r_e = \frac{26\text{ mV}}{2.06\text{ mA}} = 12.62\ \Omega$. $r_\pi = (151) \times 12.62 = 1.905$ kΩ.
- Step 2 - Voltage Gain (A_v): $R'_E = 3.3k \parallel 1k = 767.4\ \Omega$. $A_v = \frac{767.4}{12.62+767.4} = 0.9838$ V/V.
- Step 3 - Input Impedance (R_{in}): $R_{in,base} = 1.905k + (151 \times 767.4) = 117.78$ kΩ. $R_B = 33k \parallel 33k = 16.5$ kΩ. $R_{in} = 16.5k \parallel 117.78k = 14.47$ kΩ.
- Step 4 - Output Impedance (R_{out}): $R'_S = R_S \parallel R_B = 600 \parallel 16.5k = 578.9\ \Omega$. $R_{out} = 3.3k \parallel \left[12.62 + \frac{578.9}{151}\right] = 3.3k \parallel [12.62 + 3.83] = 3.3k \parallel 16.45 = 16.37\ \Omega$!

Practical Application: High-Impedance Sensor Buffer Design

- Problem Scenario: A piezoelectric transducer with high source impedance $R_S = 100$ kΩ drives a low impedance load $R_L = 100$ Ω. Compare direct connection versus inserting an Emitter Follower buffer ($R_{in} = 500$ kΩ, $R_{out} = 10$ Ω, $A_v = 0.99$).
- Direct Connection Signal Voltage: $V_L = V_S \frac{R_L}{R_S + R_L} = V_S \frac{100}{100{,}000+100} = 0.000999 V_S$ (99.9% of signal LOST due to loading!).
- Buffered Connection Signal Voltage:
- Input voltage $V_{in} = V_S \frac{R_{in}}{R_S + R_{in}} = V_S \frac{500k}{600k} = 0.8333 V_S$.
- Output voltage $V_L = A_v V_{in} \frac{R_L}{R_{out} + R_L} = (0.99)(0.8333 V_S) \frac{100}{10+100} = 0.750 V_S$.
- Performance Gain: Signal voltage transfer restored from 0.1% to 75.0% — a 750-fold improvement in voltage delivered to the load!

Limitations of Emitter Follower: Cutoff & Clipping

- Asymmetrical Drive Capability: Emitter follower can source large transient currents (transistor turns ON hard), but sinking current is strictly limited by DC bias current $I_E = \frac{V_E - V_{EE}}{R_E}$.
- Negative Swing Cutoff Clipping: On large negative input voltage swings, if load current demand $\frac{\Delta V}{R_L} > I_E$, transistor cuts off completely ($I_C = 0$), clipping the negative waveform.
- Complementary Push-Pull Solution: Replace single transistor and resistor R_E with NPN-PNP complementary pair (Class-AB Emitter Follower).
- Push-Pull Advantage: NPN transistor sources positive load current; PNP transistor sinks negative load current, achieving symmetrical drive capability.

Summary & Key Takeaways: Emitter Follower Circuit

- Voltage Gain & Phase: Near-unity voltage gain ($A_v = \frac{R'_E}{r_e + R'_E} \approx 0.98 - 0.999$), non-inverting ($0^\circ$ phase shift).
- Impedance Transformation: High input impedance ($R_{in} = R_B \parallel [r_\pi + (1 + \beta_0)R'_E]$) and low output impedance ($R_{out} = R_E \parallel [r_e + \frac{R'_S}{1+\beta_0}]$).
- Feedback & Bandwidth: Operates as 100% voltage-series feedback amplifier ($\beta = 1.0$), immune to Miller multiplication, yielding ultra-wide bandwidth.
- Buffer Application: Ideal impedance matching buffer bridging high-impedance sensors and low-impedance loads.