Lecture 32: Voltage gain of feedback amplifier

Feedback in amplifiers

DI02011011: Electronics Circuit and Application (ECA)

Lecture Agenda: Advanced Feedback Analysis

- Unified Characterization of Primary Gain Types Across Four Topologies
- Rigorous Two-Port h-Parameter Analysis of Voltage-Series Amplifiers
- Voltage Gain Derivation for Two-Stage CE-CC Cascaded Feedback Pair
- FET Common-Drain & Common-Source Voltage Gain Derivations
- Transresistance (Voltage-Shunt) Feedback to Voltage Gain Conversion
- Multistage Op-Amp Closed-Loop Gain Dynamics & Finite Open-Loop Gain Error
- High-Frequency Response & Single-Pole vs Multi-Pole Response
- Gain-Bandwidth Product Invariance ($A_{0f} \cdot \omega_{Hf} = A_0 \cdot \omega_H$)
- Dominant Pole Frequency Compensation to Prevent Closed-Loop Peaking
- Solved Problem: Complete Two-Port Voltage-Series Analysis
- Solved Problem: High-Frequency Voltage Gain & Closed-Loop Bandwidth
- Impact of Source and Load Impedance Loading on Voltage Gain
- Summary & Engineering Synthesis

Unified Gain Characterization Across Topologies

- Voltage-Series (Series-Shunt): Input V_s, Output V_o. Transfer ratio $A_v = V_o/V_i$, feedback $\beta_v = V_f/V_o$. Closed-loop voltage gain $A_{vf} = \frac{A_v}{1+\beta_v A_v}$.
- Voltage-Shunt (Shunt-Shunt): Input I_s, Output V_o. Transfer ratio $R_m = V_o/I_i$ (transresistance in Ω). Feedback $\beta_g = I_f/V_o$ (Siemens). Terminal voltage gain $A_{vf} = \frac{V_o}{V_s} = \frac{R_{mf}}{R_s} = \frac{R_m/(1+\beta_g R_m)}{R_s}$.
- Current-Series (Series-Series): Input V_s, Output I_o. Transfer ratio $G_m = I_o/V_i$ (transconductance in Siemens). Feedback $\beta_z = V_f/I_o$ (Ω). Terminal voltage gain $A_{vf} = \frac{V_o}{V_s} = \frac{-I_o R_L}{V_s} = \frac{-G_{mf} R_L}{1+\beta_z G_{mf}}$.
- Current-Shunt (Shunt-Series): Input I_s, Output I_o. Transfer ratio $A_i = I_o/I_i$, feedback $\beta_i = I_f/I_o$. Terminal voltage gain $A_{vf} = \frac{V_o}{V_s} = \frac{-A_{if} R_L}{R_s}$.

Rigorous Two-Port Analysis of Voltage-Series Amplifiers

- Step 1 - Topology Verification: Output voltage sampled in parallel; feedback voltage injected in series $\rightarrow$ model feedback network as two-port h-parameter block.
- Step 2 - Determine Loaded Open-Loop Circuit: Load input port of basic amplifier with $h_{11} = Z_{in,\beta}\Big|_{V_o=0}$; load output port with $h_{22}^{-1} = Z_{out,\beta}\Big|_{I_i=0}$.
- Step 3 - Compute Loaded Open-Loop Gain (A_v'): Calculate $A_v' = \frac{V_o'}{V_i'}\Big|_{loaded}$ incorporating h_{11}, h_{22}^{-1}, source R_s, and load R_L.
- Step 4 - Evaluate Feedback Factor & Closed-Loop Gain: Determine $\beta = h_{12} = \frac{V_f}{V_o}\Big|_{I_i=0}$.

  Closed-loop gain is $A_{vf} = \frac{A_v'}{1+\beta A_v'}$.

Voltage Gain Derivation for Two-Stage CE-CC Feedback Pair

- Circuit Configuration: Stage 1 Common-Emitter Q_1, Stage 2 Emitter Follower Q_2. Feedback resistor R_f connected from Emitter of Q_2 back to Emitter of Q_1 (R_{E1}).
- First Stage Loaded Gain (A_{v1}): $A_{v1} = \frac{-h_{fe1}(R_{C1} \| R_{in2})}{r_{\pi 1} + (1+h_{fe1})(R_{E1} \| R_f)}$.
- Second Stage Loaded Gain (A_{v2}): Emitter follower gain $A_{v2} \approx 1.0$. Total open-loop gain $A'_v = A_{v1} \cdot A_{v2}$.
- Feedback Factor & Closed-Loop Gain: Feedback ratio $\beta = \frac{R_{E1}}{R_{E1}+R_f}$. Overall closed-loop voltage gain $A_{vf} = \frac{A'_v}{1+\beta A'_v} \approx \frac{1}{\beta} = 1 + \frac{R_f}{R_{E1}}$.

FET Common-Drain & Common-Source Voltage Gain Analysis

- JFET/MOSFET Voltage Amplifier Model: Small-signal model featuring transconductance g_m and drain output resistance r_d.
- Unbypassed Source Resistor R_S: Introduces local voltage-series feedback. Open-loop gain without feedback $A_v = -g_m(R_D \parallel r_d)$. Feedback ratio $\beta = \frac{R_S}{R_D}$.
- Exact Closed-Loop Gain Equation: Deriving from small-signal AC circuit: $A_{vf} = \frac{-g_m R_D}{1+g_m R_S + \frac{R_D+R_S}{r_d}}$.
- FET Gain Simplification ($r_d \to \infty$): $A_{vf} \approx \frac{-g_m R_D}{1+g_m R_S}$. For high transconductance loop gain ($g_m R_S \gg 1$), gain simplifies to $A_{vf} \approx -\frac{R_D}{R_S}$, independent of g_m!

Transresistance Feedback to Voltage Gain Conversion

- Voltage-Shunt Topology Model: Modeled using two-port y-parameters. Feedback factor $\beta_g = y_{12} = -\frac{I_f}{V_o} = -\frac{1}{R_f}$.
- Loaded Open-Loop Transresistance (R'_m): Calculated by loading input with $y_{11}^{-1} = R_f$ in parallel with R_s and output with $y_{22}^{-1} = R_f$ in parallel with R_L: $R'_m = \frac{V_o}{I_i}\Big|_{loaded}$.
- Closed-Loop Transresistance (R_{mf}): $R_{mf} = \frac{R'_m}{1+\beta_g R'_m} = \frac{R'_m}{1+R'_m/R_f}$.
- Terminal Voltage Gain Equation: $A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{mf}}{R_s} = \frac{-R_f}{R_s} \cdot \frac{1}{1+\frac{R_f+R_s}{R'_m}}$.

Multistage Op-Amp Voltage Gain Dynamics & Finite Gain Error

- Internal Op-Amp Architecture: Cascaded differential input stage ($A_1 \approx 40$ dB), high-gain intermediate stage ($A_2 \approx 60$ dB), and output buffer ($A_3 \approx 0$ dB). Total open-loop gain $A_{OL} = A_1 A_2 A_3 \approx 10^5$ V/V (100 dB).
- Finite Open-Loop Gain Equation: Closed-loop gain for non-inverting amplifier with finite A_{OL}: $A_{vf} = \frac{A_{ideal}}{1+\frac{A_{ideal}}{A_{OL}}}$, where $A_{ideal} = 1 + \frac{R_2}{R_1}$.
- Gain Error Percentage (ϵ_g): $\epsilon_g = \frac{A_{ideal} - A_{vf}}{A_{ideal}} = \frac{A_{ideal}}{A_{OL} + A_{ideal}} \approx \frac{A_{ideal}}{A_{OL}}$.
- Numerical Precision Example: If $A_{ideal} = 100$ V/V and $A_{OL} = 100,000$ V/V, fractional gain error $\epsilon_g = \frac{100}{100,000} = 0.001 = 0.1\%$. Actual gain is 99.9 V/V.

High-Frequency Response & Gain-Bandwidth Constancy

- Single-Pole Open-Loop Model: High-frequency gain response $A(s) = \frac{A_0}{1+s/\omega_H}$, where A_0 is midband gain and $\omega_H = 2\pi f_H$ is 3-dB cutoff frequency.
- Closed-Loop Frequency Transfer Function: Substituting $A(s)$ into $A_f(s) = \frac{A(s)}{1+\beta A(s)}$ yields $A_f(s) = \frac{\frac{A_0}{1+A_0\beta}}{1+\frac{s}{\omega_H(1+A_0\beta)}} = \frac{A_{0f}}{1+s/\omega_{Hf}}$.
- Closed-Loop Bandwidth Expansion: Midband gain drops to $A_{0f} = \frac{A_0}{1+A_0\beta}$, while closed-loop bandwidth expands to $\omega_{Hf} = \omega_H(1 + A_0\beta)$.
- Gain-Bandwidth Product (GBW) Invariance: Multiplying midband gain by bandwidth: $A_{0f} \cdot \omega_{Hf} = \left(\frac{A_0}{1+A_0\beta}\right) \cdot [\omega_H(1 + A_0\beta)] = A_0 \cdot \omega_H = \omega_T$. The GBW product is strictly conserved!

Dominant Pole Compensation & Closed-Loop Peaking

- Multi-Pole Transfer Function: Two-pole open-loop gain $A(s) = \frac{A_0}{(1+s/\omega_1)(1+s/\omega_2)}$ exhibits -180° phase shift at high frequencies.
- Closed-Loop Second-Order System: $A_f(s) = \frac{A_{0f}}{1+s\frac{\omega_1+\omega_2}{\omega_1\omega_2(1+A_0\beta)}+s^2\frac{1}{\omega_1\omega_2(1+A_0\beta)}}$.
- Damping Factor (ζ) & Peaking (M_p): Damping factor $\zeta = \frac{\omega_1+\omega_2}{2\sqrt{\omega_1\omega_2(1+A_0\beta)}}$. If $\zeta < 0.707$, frequency response exhibits peaking $M_p > 1$.
- Dominant Pole Compensation: Adding Miller capacitor C_c pushes dominant pole ω_1 down to ω_D, ensuring phase margin $\phi_m \geq 45^\circ$ to prevent gain peaking.

Numerical Problem: Complete Two-Port Voltage-Series Analysis

- Given Circuit: BJT stage with source $R_s = 1$ kΩ, feedback network resistors $R_1 = 9$ kΩ, $R_2 = 1$ kΩ, collector $R_C = 2$ kΩ, $h_{fe} = 100$, $h_{ie} = 1$ kΩ. Feedback taken from collector and connected to emitter via R_1, R_2.
- Step 1 - Feedback h-parameters: $h_{11} = R_1 \parallel R_2 = 9k \parallel 1k = 900\ \Omega$. $\beta = h_{12} = \frac{R_2}{R_1+R_2} = \frac{1k}{10k} = 0.10$. $h_{22}^{-1} = R_1 + R_2 = 10$ kΩ.
- Step 2 - Loaded Open-Loop Gain (A'_v): Total input resistance $R'_{in} = R_s + h_{ie} + h_{11} = 1000 + 1000 + 900 = 2900\ \Omega$. Total load resistance $R'_L = R_C \parallel h_{22}^{-1} = 2k \parallel 10k = 1.667$ kΩ. Loaded gain $A'_v = \frac{-h_{fe}R'_L}{R'_{in}} = \frac{-100\times1667}{2900} = -57.48$ V/V.
- Step 3 - Closed-Loop Gain (A_{vf}): Desensitivity factor $(1 + \beta|A'_v|) = 1 + (0.10 \times 57.48) = 6.75$. Closed-loop voltage gain $A_{vf} = \frac{-57.48}{6.75} = -8.52$ V/V.

Numerical Problem: High-Frequency Gain & Bandwidth Calculation

- Problem Statement: An operational amplifier has DC open-loop gain $A_0 = 200,000$ V/V (106 dB) and dominant pole cutoff frequency $f_H = 5$ Hz. Find closed-loop gain A_{vf} and 3-dB bandwidth f_{Hf} for non-inverting feedback configurations with (a) $\beta = 0.01$ and (b) $\beta = 1.0$.
- Case (a) $\beta = 0.01$: Loop gain $A_0\beta = 200,000 \times 0.01 = 2000$. Desensitivity factor $(1 + A_0\beta) = 2001$. Closed-loop gain $A_{vf} = \frac{200,000}{2001} = 99.95$ V/V (40 dB). Closed-loop bandwidth $f_{Hf} = 5$ Hz $\times$ 2001 $= 10.005$ kHz.
- Case (b) Unity Gain Buffer ($\beta = 1.0$): Desensitivity factor $(1 + A_0\beta) = 200,001$. Closed-loop gain $A_{vf} = \frac{200,000}{200,001} \approx 0.999995$ V/V (0 dB). Closed-loop bandwidth $f_{Hf} = 5$ Hz $\times$ $200,001 = 1.000005$ MHz!
- Verification of GBW Invariance: Case (a) 99.95×10.005 kHz $= 1.0$ MHz. Case (b) 1.0×1.0 MHz $= 1.0$ MHz. Gain-bandwidth product is perfectly conserved at 1 MHz!

Impact of Source and Load Impedances on Overall Gain

- Terminal vs. Overall Voltage Gain: Terminal gain $A_v = V_o/V_i$; overall source-to-load voltage gain $A_{vs} = \frac{V_o}{V_s} = A_v \cdot \frac{R_{in}}{R_s+R_{in}} \cdot \frac{R_L}{R_{out}+R_L}$.
- Voltage-Series Loading Mitigation: Voltage-series feedback increases input resistance $R_{in,f} = R_{in}(1 + A\beta)$ and decreases output resistance $R_{out,f} = \frac{R_{out}}{1+A\beta}$.
- Input Loading Factor: $\frac{R_{in,f}}{R_s+R_{in,f}} \approx 1.0$ because $R_{in,f} \gg R_s$.
- Output Loading Factor: $\frac{R_L}{R_{out,f}+R_L} \approx 1.0$ because $R_{out,f} \ll R_L$. Overall gain $A_{vs,f} \approx A_{vf}$, isolating amplifier performance from source and load fluctuations.

Summary & Key Takeaways: Advanced Voltage Gain Dynamics

- Topological Conversion: All four feedback topologies can be converted to effective terminal voltage gain using source (R_s) and load (R_L) network transformations.
- Two-Port Modeling Precision: Modeling feedback loading via h_{11} and h_{22}^{-1} yields exact closed-loop voltage gain $A_{vf} = \frac{A'_v}{1+\beta A'_v}$.
- Gain-Bandwidth Product Invariance: Closed-loop gain reduction expands upper cutoff frequency ($f_{Hf} = f_H(1 + A_0\beta)$), maintaining $A_{0f} \cdot f_{Hf} = f_T$.
- Stability & Compensation: High loop gain in multi-pole systems can cause gain peaking; Miller dominant pole frequency compensation enforces phase margin $\phi_m \geq 45^\circ$.