Lecture 26: Frequency Response of Two Stage RC Coupled amplifier

Frequency Response of Transistor Amplifier

DI02011011: Electronics Circuit and Application (ECA)

Lecture Agenda & Outline

- 1. Multi-Stage Architecture: Cascaded BJT RC Coupling and DC Biasing Isolation
- 2. Midband Voltage Gain Derivation: Small-Signal AC Equivalent & Stage-to-Stage Interstage Loading
- 3. Low-Frequency Response: Coupling Capacitors (C_C1, C_C2, C_C3) and Emitter Bypass Capacitors (C_E1, C_E2) Pole Calculations
- 4. High-Frequency Response: Hybrid-pi Model, Parasitic Capacitances (C_pi, C_mu), and Miller Effect Transformation
- 5. Multistage Frequency Response Metrics: Dominant Pole Approximations, Bandwidth Shrinkage, and Gain-Bandwidth Product
- 6. Step-by-Step Comprehensive Numerical Design Example and Performance Trade-offs

Two-Stage RC Coupled Amplifier Circuit Architecture & Biasing

- Circuit Configuration: Two cascaded Common-Emitter (CE) BJT stages connected via an interstage coupling capacitor C_C2, with input coupling capacitor C_C1 and output coupling capacitor C_C3.
- DC Biasing Isolation: Coupling capacitors block DC voltage components, allowing independent Q-point biasing (V_CEQ1, I_CQ1 and V_CEQ2, I_CQ2) for each stage via voltage dividers (R_11, R_12 and R_21, R_22).
- AC Signal Coupling: Coupling capacitors present low reactive impedance (X_C = 1 / (2 *pi* f * C) approx 0) in the midband frequency range, allowing AC signal transmission with minimal attenuation between stages.
- Emitter Bypass Networks: Resistors R_E1 and R_E2 provide thermal Q-point stabilization against beta variations, while parallel capacitors C_E1 and C_E2 bypass AC signals to ground to prevent degenerative AC gain reduction.
- Interstage Loading Interaction: The input impedance of the second stage R_in2 = R_21 —— R_22 —— r_pi2 acts as a parallel AC load on the collector resistor R_C1 of the first stage, reducing the effective first-stage gain.

Midband Voltage Gain Derivation & Interstage Loading

- Small-Signal Parameters: Hybrid-pi parameters for stage i: transconductance g_mi = I_CQi / V_T (where V_T approx 26 mV at 300K) and base input resistance r_pi_i = beta_0i / g_mi.
- Stage 2 Voltage Gain (A_v2): The load seen by stage 2 collector is R_L2' = R_C2 —— R_L. Gain A_v2 = V_o / V_i2 = -g_m2 * (R_C2 —— R_L).
- Stage 1 Voltage Gain (A_v1): Stage 1 collector sees AC load R_L1' = R_C1 —— R_B2 —— r_pi2, where R_B2 = R_21 —— R_22. Gain A_v1 = V_i2 / V_i1 = -g_m1 * (R_C1 —— R_B2 —— r_pi2).
- Total Midband System Voltage Gain (A_v0): Calculated as the product of individual voltage gains: A_v0 = A_v1 *A_v2 = g_m1* g_m2 *(R_C1 —— R_B2 —— r_pi2)* (R_C2 —— R_L).
- Overall Voltage Gain from Signal Source (A_vs0): Incorporating source resistance R_s: A_vs0 = (V_o / V_s) = A_v0 * (R_in1 / (R_s + R_in1)), where R_in1 = R_B1 —— r_pi1.
- Decibel Representation: Overall gain in dB is A_v0,dB = 20 * log10(—A_v0—) = A_v1,dB + A_v2,dB.

Low-Frequency Response: Coupling Capacitor Poles Analysis

- Low-Frequency Attenuation Mechanisms: At low frequencies, capacitive reactance X_C = 1 / (2 *pi* f * C) increases, causing potential divider action with circuit resistances and rolling off gain at 20 dB/decade per capacitor.
- Input Coupling Capacitor Pole (f_L,C1): Sees resistance R_eq,C1 = R_s + R_in1 = R_s + (R_11 —— R_12 —— r_pi1). Cutoff frequency f_L,C1 = 1 / (2 *pi* (R_s + R_in1) * C_C1).
- Interstage Coupling Capacitor Pole (f_L,C2): Sees output resistance of stage 1 in series with input resistance of stage 2: R_eq,C2 = (R_C1 —— r_o1) + (R_B2 —— r_pi2). Cutoff frequency f_L,C2 = 1 / (2 *pi* (R_C1 + R_in2) * C_C2).
- Output Coupling Capacitor Pole (f_L,C3): Sees output resistance of stage 2 in series with load resistance: R_eq,C3 = R_C2 + R_L. Cutoff frequency f_L,C3 = 1 / (2 *pi* (R_C2 + R_L) * C_C3).
- High-Pass Transfer Function Formulation: Each coupling capacitor contributes a first-order high-pass transfer factor s / (s + omega_Li), where omega_Li = 2 *pi* f_Li.

Low-Frequency Response: Emitter Bypass Capacitor Poles

- Bypass Capacitor Action: Capacitor C_E in parallel with R_E creates a pole-zero pair in the low-frequency transfer function. At low frequencies, incomplete AC bypassing introduces emitter degeneration.
- Equivalent Resistance Seen by C_E1: Reflected source and base resistance looking into the emitter of Stage 1: R_eq,E1 = R_E1 —— ((r_pi1 + (R_s —— R_B1)) / (1 + beta_0)).
- Stage 1 Emitter Cutoff Frequency (f_L,E1): Derived as f_L,E1 = 1 / (2 *pi* R_eq,E1 * C_E1). Because R_eq,E1 is typically small (tens of ohms), f_L,E1 requires large capacitance (e.g., 10 uF - 100 uF) to keep the pole low.
- Stage 2 Emitter Cutoff Frequency (f_L,E2): Equivalent resistance R_eq,E2 = R_E2 —— ((r_pi2 + (R_C1 —— R_B2)) / (1 + beta_0)), giving cutoff f_L,E2 = 1 / (2 *pi* R_eq,E2 * C_E2).
- Zero Frequency of Emitter Network: The zero occurs at lower frequency f_Z,Ei = 1 / (2 *pi* R_Ei * C_Ei), below which gain flattens out to unbypassed gain A_v,unbypassed approx -R_C / R_E.

Low-Frequency Bode Plot & Dominant Pole Determination

- Overall Low-Frequency System Transfer Function: A_v(s) = A_v0 * product_{i=1}^{5} (s / (s + omega_Li)) (assuming 3 coupling and 2 bypass poles).
- Asymmetrical Low-Frequency Slope: For frequencies omega ¡¡ omega_L,min, the asymptotic slope rolls off at +100 dB/decade (+5 x 20 dB/dec) with a phase lead approaching +450 degrees.
- Dominant Pole Approximation: If one low-frequency pole omega_L,dom is significantly higher than all other low-frequency poles (by a factor of ¿= 4), then lower 3-dB cutoff frequency f_L approx f_L,dom.
- Non-Dominant Pole Interaction Formula: When multiple low-frequency poles are close to each other, the overall lower 3-dB cutoff frequency is approximated by: f_L approx sqrt(f_L1^2 + f_L2^2 + f_L3^2 + f_L,E1^2 + f_L,E2^2).
- Design Rule for Dominant Pole Placement: Design rules typically set f_L,E1 and f_L,E2 as the dominant lower cutoff poles to minimize required physical capacitor sizes.

High-Frequency Response: Hybrid-pi Model Parasitic Capacitances

- BJT Internal Parasitic Capacitances: High-frequency roll-off is dictated by internal junction capacitances: base-emitter junction capacitance C_pi = C_b'e (diffusion + depletion) and base-collector junction capacitance C_mu = C_b'c (depletion capacitance).
- Transistor Gain-Bandwidth Product (f_T): The unity-current-gain frequency f_T = g_m / (2 *pi* (C_pi + C_mu)). Typical values for RF/small-signal BJTs range from 300 MHz to several GHz.
- Diffusion Capacitance Dynamics: C_de = g_m * tau_F, where tau_F is the forward transit time of minority carriers across the base (typically 10 - 500 ps). C_de dominates C_pi at higher collector currents.
- Depletion Capacitance Dependence: C_mu = C_mu0 / (1 + V_CB / V_0)^m, where m approx 0.33 - 0.5 depending on junction grading.
- Stray Wiring Capacitances (C_W): PCB traces, interconnects, and socket capacitances add parasitic shunt capacitance C_W1, C_W2 (typically 2 - 10 pF) to ground at each node.

High-Frequency Response: Miller Effect Transformation

- Miller Theorem Statement: A feedback impedance Z_F connected between input and output nodes with inverted voltage gain A_v = V_o / V_i can be decoupled into equivalent input and output shunt impedances to ground.
- Miller Input Capacitance (C_M,in): C_M,in = C_mu *(1 - A_v). For an inverting stage where A_v = -—A_v—, C_M,in = C_mu* (1 + —A_v—).
- Miller Output Capacitance (C_M,out): C_M,out = C_mu * (1 - 1 / A_v) approx C_mu (since —A_v— ¿¿ 1).
- Stage 1 Total High-Frequency Input Capacitance (C_in1,hi): C_in1,hi = C_pi1 + C_mu1 * (1 + —A_v1—) + C_W1. Because —A_v1— is large, C_M,in1 completely dominates the input node capacitance!
- Stage 2 Total High-Frequency Input Capacitance (C_in2,hi): C_in2,hi = C_pi2 + C_mu2 * (1 + —A_v2—) + C_W2.

High-Frequency Cutoff Frequency f_H & Dominant Pole Analysis

- Stage 1 Input High-Frequency Pole (f_H1): Equivalent Thevenin resistance seen by C_in1,hi: R_th1 = R_s —— R_B1 —— r_pi1. Cutoff frequency f_H1 = 1 / (2 *pi* R_th1 * C_in1,hi).
- Interstage High-Frequency Pole (f_H2): Equivalent Thevenin resistance seen by C_in2,hi: R_th2 = R_C1 —— R_B2 —— r_pi2 —— r_o1. Cutoff frequency f_H2 = 1 / (2 *pi* R_th2 * C_in2,hi).
- Output High-Frequency Pole (f_H3): Total output capacitance C_out2 = C_mu2 + C_W3 seeing resistance R_th3 = R_C2 —— R_L —— r_o2. Cutoff frequency f_H3 = 1 / (2 *pi* R_th3 * C_out2).
- Overall Upper 3-dB Frequency Estimate (f_H): Combining non-dominant high-frequency poles using the reciprocal square-root approximation: 1 / f_H approx 1.1 * sqrt(1/f_H1^2 + 1/f_H2^2 + 1/f_H3^2).
- Open-Circuit Time Constant (OCT) Method: Alternative robust estimation f_H approx 1 / (2 *pi* sum(tau_Hi_0)), where tau_Hi_0 = R_i0 * C_i.

Multistage Bandwidth Shrinkage & Gain-Bandwidth Product

- Identical Cascaded Stage Bandwidth Reduction: For N identical non-interacting amplifier stages each with upper cutoff f_H1 and lower cutoff f_L1:
- System Upper Cutoff Formula: f_H,sys = f_H1 *sqrt(2^(1/N) - 1). For N = 2 stages, sqrt(2^(1/2)-1) = sqrt(sqrt(2)-1) approx 0.643 =¿ f_H,sys = 0.643* f_H1.
- System Lower Cutoff Formula: f_L,sys = f_L1 / sqrt(2^(1/N) - 1). For N = 2 stages, f_L,sys = f_L1 / 0.643 = 1.56 * f_L1.
- System Bandwidth Shrinkage: Overall system bandwidth BW_sys = f_H,sys - f_L,sys approx 0.643 *f_H1 - 1.56* f_L1. Cascading stages narrows overall passband bandwidth!
- Gain-Bandwidth Product (GBP) Trade-Off: While cascading boosts midband voltage gain (A_v0 = A_v1^N), the overall bandwidth reduces, demanding careful pole management in high-frequency communications.

Comprehensive Worked Numerical Design Example

- Circuit Parameters: Two identical BJT stages with g_m = 40 mS, r_pi = 2.5 kOhm, R_C1 = R_C2 = 4 kOhm, R_B1 = R_B2 = 50 kOhm, R_s = 1 kOhm, R_L = 10 kOhm.
- Capacitor Values: C_C1 = C_C2 = C_C3 = 10 uF, C_E1 = C_E2 = 100 uF, C_pi = 30 pF, C_mu = 2 pF.
- Step 1: Calculate Stage Gains: R_L2' = 4k —— 10k = 2.86 kOhm =¿ A_v2 = -40 mS * 2.86 kOhm = -114.4.
- Stage 1 Load: R_L1' = 4k —— 50k —— 2.5k = 1.488 kOhm =¿ A_v1 = -40 mS * 1.488 kOhm = -59.5.
- Total Midband Gain: A_v0 = A_v1 *A_v2 = (-59.5)* (-114.4) = +6807 (76.66 dB).
- Step 2: Miller Capacitance: C_M,in1 = 2 pF * (1 + 59.5) = 121 pF =¿ C_in1,hi = 30 + 121 = 151 pF.
- C_M,in2 = 2 pF * (1 + 114.4) = 230.8 pF =¿ C_in2,hi = 30 + 230.8 = 260.8 pF.
- Step 3: High-Frequency Cutoffs: R_th1 = 1k —— 50k —— 2.5k = 704 Ohm =¿ f_H1 = 1 / (2 *pi* 704 * 151pF) = 1.497 MHz.
- R_th2 = 1.488 kOhm =¿ f_H2 = 1 / (2 *pi* 1488 * 260.8pF) = 410.2 kHz.
- Overall Upper Cutoff: f_H approx 1 / sqrt(1/(1.497M)^2 + 1/(410.2k)^2) = 395.7 kHz.

Frequency Response Comparison: Single-Stage vs Two-Stage RC Coupled

- Midband Voltage Gain Comparison: Single-stage CE provides A_v approx 50-100, whereas two-stage RC coupled provides A_v0 approx 2,000-10,000 (34 dB - 80 dB gain range).
- Bandwidth Comparison: Single-stage features wider bandwidth (BW approx 2 - 5 MHz), whereas two-stage suffers bandwidth compression (BW approx 300 kHz - 800 kHz).
- Phase Response Comparison: Single-stage exhibits 180-degree phase shift in midband (-90 deg at f_L, -270 deg at f_H). Two-stage exhibits 0-degree (360 deg) midband phase shift.
- Noise & Distortion Trade-Offs: Two-stage amplifies first-stage thermal and shot noise; cumulative phase shifts at high frequencies increase susceptibility to parasitic oscillation if stray feedback exists.
- Practical Design Applications: Audio preamplifiers, sensor signal conditioning blocks, intermediate frequency (IF) gain stages in radio receivers.

Summary & Key Engineering Takeaways

- Midband Gain Equation: A_v0 = A_v1 *A_v2 = [-g_m1* (R_C1 —— R_B2 —— r_pi2)] *[-g_m2* (R_C2 —— R_L)].
- Low-Frequency Roll-Off: Dictated by external coupling capacitors (C_C1, C_C2, C_C3) and emitter bypass capacitors (C_E1, C_E2). Dominant pole sets lower cutoff f_L.
- High-Frequency Roll-Off: Dictated by BJT parasitic capacitances (C_pi, C_mu) and Miller multiplication C_M,in = C_mu * (1 + —A_v—), setting upper cutoff f_H.
- Multistage Bandwidth Shrinkage: For 2 identical stages, f_H,sys = 0.643 *f_H1 and f_L,sys = 1.56* f_L1, narrowing net passband.
- Design Guideline: Select large emitter bypass capacitors to prevent dominant low-frequency gain degradation, and use low source/load resistances to maximize high-frequency bandwidth.