Lecture 24: Gain of multi-stage amplifier

Frequency Response of Transistor Amplifier

DI02011011: Electronics Circuit and Application (ECA)

Lecture Agenda & Learning Roadmap

- Necessity and Structural Architecture of Multi-Stage Cascaded Amplifiers
- Total Voltage Gain Derivation in Linear and Decibel Scales
- Inter-Stage Loading Effects on Individual Stage Gain Calculations
- Complete Source-to-Load System Gain (A_{vs}) Derivation
- Detailed Step-by-Step Numerical Example: Two-Stage CE-CE Amplifier
- Cascode Configuration (CE-CB Pair): High Gain & Miller Effect Elimination
- Darlington Pair Configuration for Ultra-High Current Gain ($A_i \approx \beta^2$)
- Effect of Cascading on System Bandwidth (Bandwidth Shrinkage Phenomenon)
- Detailed Step-by-Step Numerical Example: 3-Stage Bandwidth Reduction
- Noise Figure Cascading & Friis Formula for Multi-Stage Signal Chains
- Comprehensive Summary and Key Design Formulas

Necessity and Architecture of Multi-Stage Cascaded Amplifiers

- Limitations of Single-Stage Amplifiers: Single stages cannot provide simultaneously high voltage gain (> 60 dB), high input impedance (> 1 MΩ), and low output impedance (< 50 Ω).
- Cascade Principle: Output signal of Stage 1 (V_{o1}) is fed as input to Stage 2 (V_{i2}), whose output (V_{o2}) drives Stage 3 (V_{i3}), up to Stage N.
- Functional Stage Specialization: (1) Input Stage: High input impedance, low noise. (2) Intermediate Stages: High voltage amplification. (3) Output Stage: Low output impedance, high power drive.
- Overall System Gains: Overall Voltage Gain $A_v = \frac{V_{oN}}{V_{i1}}$, Current Gain $A_i = \frac{I_{oN}}{I_{i1}}$, Power Gain $A_p = A_v A_i$.

Total Voltage Gain Calculation in Linear and Decibel Scales

- Linear Multiplication Rule: For N cascaded stages, overall voltage gain is the product of individual LOADED stage voltage gains: $A_v = \frac{V_{o1}}{V_{i1}} \cdot \frac{V_{o2}}{V_{i2}} \cdot \cdots \cdot \frac{V_{oN}}{V_{iN}} = \prod_{k=1}^{N} A_{vk}$.
- Decibel Addition Rule: Converting to decibels simplifies gain calculations into simple additions: $A_{v(\text{dB})} = 20 \log_{10} \left| \prod_{k=1}^{N} A_{vk} \right| = \sum_{k=1}^{N} 20 \log_{10} |A_{vk}| = \sum_{k=1}^{N} A_{vk(\text{dB})}$.
- Current Gain Product: Total system current gain $A_i = A_{i1} \cdot A_{i2} \ldots A_{iN} = \prod_{k=1}^{N} A_{ik}$.
- Power Gain Product: Total power gain $A_p = A_{p1} \cdot A_{p2} \ldots A_{pN}$. In decibels, $A_{p(\text{dB})} = A_{p1(\text{dB})} + A_{p2(\text{dB})} + \cdots + A_{pN(\text{dB})}$.

Inter-Stage Loading Effects on Individual Stage Gain Calculations

- Inter-Stage Loading Phenomenon: The input impedance $R_{in(k+1)}$ of stage $k+1$ appears in parallel with collector/drain resistor R_{Ck} of stage k.
- Loaded Gain Formula for Stage k: $A_{vk,\text{loaded}} = -g_{mk}\left(R_{Ck} \parallel R_{in(k+1)}\right)$.
- Input Impedance of BJT Stage $k+1$: $R_{in(k+1)} = R_{1(k+1)} \parallel R_{2(k+1)} \parallel r_{\pi(k+1)}$ for a fully bypassed Common-Emitter stage.
- Open-Circuit vs Loaded Gain Warning: Calculating stage k gain as $A_{vk} = -g_{mk}R_{Ck}$ ignoring $R_{in(k+1)}$ leads to severe overestimation of overall system gain!

Complete Source-to-Load System Gain (A_{vs}) Derivation

- System Signal Chain Model: Source V_s with resistance $R_S \rightarrow$ Input Stage 1 $\rightarrow$ Intermediate Stages $\rightarrow$ Output Stage $N \rightarrow$ Load R_L.
- Input Attenuation Factor: $V_{i1} = V_s \left(\frac{R_{in1}}{R_S + R_{in1}} \right)$, where $R_{in1} = R_{11} \parallel R_{21} \parallel r_{\pi 1}$.
- Output Divider Factor: $V_o = V_{oN} \left(\frac{R_L}{R_{outN} + R_L} \right)$, where $R_{outN} \approx R_{CN}$.
- Complete System Voltage Gain Equation:
  $A_{vs} = \frac{V_o}{V_s} = \left(\frac{R_{in1}}{R_S + R_{in1}} \right) \cdot A_{v1,\text{loaded}} \cdot A_{v2,\text{loaded}} \ldots A_{vN,\text{loaded}} \cdot \left(\frac{R_L}{R_{outN} + R_L} \right)$.

Numerical Example 1: Two-Stage RC-Coupled CE-CE Voltage Gain Analysis

- Given Circuit Parameters: $V_{CC} = 12$ V, $R_S = 600\ \Omega$, $R_L = 10$ kΩ. Stage 1: $R_{11} = 40$ kΩ, $R_{21} = 10$ kΩ, $R_{C1} = 4.7$ kΩ, $I_{C1} = 1$ mA, $\beta_1 = 100$. Stage 2: $R_{12} = 33$ kΩ, $R_{22} = 10$ kΩ, $R_{C2} = 2.2$ kΩ, $I_{C2} = 2$ mA, $\beta_2 = 150$. Small-signal params: $g_{m1} = 38.46$ mS, $r_{\pi 1} = 2.6$ kΩ; $g_{m2} = 76.92$ mS, $r_{\pi 2} = 1.95$ kΩ.
- Step 1 - Stage 2 Input Impedance (R_{in2}): $R_{in2} = R_{12} \parallel R_{22} \parallel r_{\pi 2} = 33\ \text{k} \parallel 10\ \text{k} \parallel 1.95\ \text{k} = 1.554$ kΩ.
- Step 2 - Stage 1 Loaded Gain (A_{v1}): Effective collector load $R'_{L1} = R_{C1} \parallel R_{in2} = 4.7\ \text{k} \parallel 1.554\ \text{k} = 1.167$ kΩ. $A_{v1} = -g_{m1} R'_{L1} = -38.46\ \text{mS} \times 1167 = -44.88$ V/V.
- Step 3 - Stage 2 Loaded Gain (A_{v2}): Effective collector load $R'_{L2} = R_{C2} \parallel R_L = 2.2\ \text{k} \parallel 10\ \text{k} = 1.803$ kΩ. $A_{v2} = -g_{m2} R'_{L2} = -76.92\ \text{mS} \times 1803 = -138.69$ V/V.
- Step 4 - Overall System Gain (A_{vs}): $R_{in1} = 40\ \text{k} \parallel 10\ \text{k} \parallel 2.6\ \text{k} = 1.962$ kΩ. $A_{vs} = \left(\frac{1962}{600+1962}\right) \times (-44.88) \times (-138.69) = 0.7658 \times 6224.4 = 4766.6$ V/V (73.56 dB).

Cascode Configuration (CE-CB Pair): High Gain & Miller Effect Elimination

- Cascode Architecture: Common-Emitter stage (Q1) driving a Common-Base stage (Q2) connected in series.
- Stage 1 Load Impedance: Collector load of Q1 is the low input impedance of CB stage Q2: $R_{L1} = R_{in,CB2} = r_{e2} = \frac{V_T}{I_C}$.
- Stage 1 Voltage Gain (A_{v1}): $A_{v1} = -g_{m1} r_{e2} = -\left(\frac{I_C}{V_T}\right)\left(\frac{V_T}{I_C}\right) = -1$ V/V.
- Elimination of Miller Effect: Because $|A_{v1}| = 1$, Miller input capacitance is $C_{M,in} = C_{\mu 1}(1+1) = 2C_{\mu 1}$, completely eliminating Miller multiplication!
- Stage 2 Voltage Gain & Total Gain: Stage 2 (CB) provides high voltage gain $A_{v2} = +g_{m2}(R_C \parallel R_L)$. Overall Cascode gain $A_v = A_{v1}A_{v2} = -g_{m1}(R_C \parallel R_L)$ with wide bandwidth.

Darlington Pair Configuration for Ultra-High Current Gain ($A_i \approx \beta^2$)

- Darlington Structure: Two BJTs connected such that collector terminals are tied together and the emitter of Q1 directly drives the base of Q2.
- Composite Current Gain (β_D): $\beta_D = \beta_1 + \beta_2 + \beta_1\beta_2 \approx \beta_1\beta_2$ (e.g., $100 \times 100 = 10,000$).
- Input Impedance ($r_{\pi,D}$): $r_{\pi,D} = r_{\pi 1} + (1 + \beta_1) r_{\pi 2} \approx 2\beta_1\beta_2 r_{e2}$, providing very high input impedance.
- Base-Emitter Voltage Drop: $V_{BE,D} = V_{BE1} + V_{BE2} \approx 1.4$ V (requires higher turn-on voltage).
- Applications: High-current output drivers, power amplifiers, and high input impedance buffer stages.

Effect of Cascading on System Bandwidth (Bandwidth Shrinkage Phenomenon)

- Bandwidth Shrinkage Phenomenon: Cascading N identical non-interacting amplifier stages increases overall midband gain $(A_M)^N$, but shrinks net system bandwidth.
- System Upper Cutoff Formula ($f_{H,sys}$): $f_{H,sys} = f_H\sqrt{2^{1/N} - 1}$, where f_H is the upper cutoff of an individual stage.
- System Lower Cutoff Formula ($f_{L,sys}$): $f_{L,sys} = \frac{f_L}{\sqrt{2^{1/N}-1}}$, where f_L is the lower cutoff of an individual stage.
- Shrinkage Multiplier Factors: For $N = 1 : 1.00$; $N = 2 : 0.643$; $N = 3 : 0.510$; $N = 4 : 0.435$.
- Net Bandwidth Impact: Lower cutoff $f_{L,sys}$ increases (worsens) while upper cutoff $f_{H,sys}$ decreases (worsens), causing significant bandwidth compression.

Numerical Example 2: 3-Stage Cascaded Amplifier Bandwidth Reduction

- Problem Statement: An amplifier consists of $N = 3$ identical cascaded stages. Each individual stage has a lower cutoff frequency $f_L = 20$ Hz and an upper cutoff frequency $f_H = 500$ kHz. Determine: (1) Single stage bandwidth BW_{single}. (2) Overall 3-stage system lower cutoff $f_{L,sys}$. (3) Overall 3-stage system upper cutoff $f_{H,sys}$. (4) Net system bandwidth BW_{sys}.
- Step 1 - Shrinkage Factor Calculation: Factor $S_N = \sqrt{2^{1/3} - 1} = \sqrt{1.2599 - 1} = \sqrt{0.2599} \approx 0.5098$.
- Step 2 - System Lower Cutoff ($f_{L,sys}$): $f_{L,sys} = \frac{f_L}{S_N} = \frac{20 \text{ Hz}}{0.5098} = 39.23$ Hz.
- Step 3 - System Upper Cutoff ($f_{H,sys}$): $f_{H,sys} = f_H \times S_N = 500 \text{ kHz} \times 0.5098 = 254.91$ kHz.
- Step 4 - Net System Bandwidth (BW_{sys}): Single stage $BW = 500 \text{ kHz} - 20 \text{ Hz} \approx 499.98$ kHz. System $BW_{sys} = 254.91 \text{ kHz} - 39.23 \text{ Hz} = 254.87$ kHz (a 49% bandwidth loss).

Noise Figure Cascading & Friis Formula for Multi-Stage Systems

- Noise Figure Definition (F): Ratio of input SNR to output SNR: $F = \frac{SNR_{in}}{SNR_{out}} \geq 1$. In decibels, $NF(\text{dB}) = 10 \log_{10} F$.
- Friis Formula for Cascaded Noise Figure: $F_{total} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1} A_{p2}} + \cdots + \frac{F_N - 1}{\prod_{k=1}^{N-1} A_{pk}}$, where F_k is stage noise factor and A_{pk} is stage linear power gain.
- Critical Design Insight: The noise factor of the overall multi-stage system is dominated almost entirely by the FIRST stage (F_1).
- Low-Noise Amplifier (LNA) Requirement: The first stage must combine a very low Noise Figure ($F_1 \approx 1$) with high power gain ($A_{p1} \gg 1$) to suppress noise contributions from subsequent stages.

Summary & Engineering Principles for Multi-Stage Amplifier Gain

- Gain Aggregation: Overall gain is product of loaded stage gains $A_v = \prod A_{vk}$. In decibels, stage gains add: $A_{v(\text{dB})} = \sum A_{vk(\text{dB})}$.
- Inter-Stage Loading: Must include input impedance $R_{in(k+1)}$ when calculating collector load $R'_{Ck} = R_{Ck} \parallel R_{in(k+1)}$.
- High-Performance Topologies: Cascode (CE-CB) eliminates Miller effect for wide bandwidth. Darlington pair provides super-beta current gain $\beta_D \approx \beta^2$.
- Bandwidth Shrinkage: Cascading N identical stages narrows system bandwidth ($f_{H,sys} = f_H\sqrt{2^{1/N} - 1}$, $f_{L,sys} = f_L/\sqrt{2^{1/N} - 1}$).
- Noise Cascading: Friis formula dictates that first-stage LNA gain and low noise figure dominate system SNR.