Lecture 18: Thermal Runaway, Thermal Resistance & Thermal Stability

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Blueprint: Thermal Mechanics & Stability

- Physical Mechanism & Positive Feedback Loop of Thermal Runaway.
- Junction Temperature Ratings ($T_{J,\max}$) & Silicon vs Germanium Package Limits.
- Quantitative Definition of Thermal Resistance ($\theta_{JA}, \theta_{JC}, \theta_{CS}, \theta_{SA}$).
- Electrical Circuit Analogy of Thermal Networks (Ohm's Law Analogy).
- Mathematical Derivation of Fundamental Thermal Stability Criterion $\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$.
- Derivation of the $V_{CE} \leq \frac{1}{2} V_{CC}$ Rule for Self-Biased Amplifiers.
- Power Transistor Derating Curves & Numerical Calculation Worked Examples.

Physical Mechanism of Thermal Runaway in BJTs

- Power Dissipation at Collector Junction: $P_D = V_{CE}I_C + V_{BE}I_B \approx V_{CE}I_C$.
- The Self-Reinforcing Positive Feedback Loop: Temperature Rise ($T_J \uparrow$) $\implies$ Leakage Current Increase ($I_{CO} \uparrow$) $\implies$ Collector Current Rise ($I_C \uparrow$) $\implies$ Power Dissipation Increase ($P_D \uparrow$) $\implies$ Further Temperature Rise ($T_J \uparrow\uparrow$).
- Destructive Junction Melting: Unchecked junction temperature exceeding $T_{J,\text{max}}$ ($150^\circ\text{C} - 200^\circ\text{C}$ for Silicon) causes permanent lattice destruction, bond rupturing, and short-circuit failure.
- Dominant Risk Factors: High ambient temperatures, inadequate heat sinking, high collector voltages ($V_{CE} > \frac{1}{2}V_{CC}$), and fixed-bias circuit topologies.

Quantitative Definition of Thermal Resistance (θ)

- Thermal Resistance Definition: $\theta \equiv \frac{\Delta T}{P_D} = \frac{T_1 - T_2}{P_D}$, measured in units of °C/W (degrees Celsius per watt).
- Junction-to-Case Resistance (θ_{JC}): Internal thermal impedance between silicon die junction and package case; fixed by semiconductor manufacturer.
- Case-to-Sink Resistance (θ_{CS}): Contact thermal impedance between transistor case and heat sink surface; dependent on thermal grease / mica washer mounting.
- Sink-to-Ambient Resistance (θ_{SA}): Convective & radiative thermal impedance from heat sink to ambient air; dependent on fin surface area and air flow.
- Total Junction-to-Ambient Resistance: $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$.

Electrical Circuit Analogy of Thermal Networks

- Thermal-Electrical Equivalence Parameters:
- • Heat Dissipation Power P_D (Watts) $\equiv$ Electrical Current I (Amperes).
- • Temperature T ($^\circ$C or K) $\equiv$ Electrical Voltage V (Volts).
- • Thermal Resistance θ ($^\circ$C/W) $\equiv$ Electrical Resistance R (Ohms).
- • Thermal Capacitance C_{th} (Joules/$^\circ$C) $\equiv$ Electrical Capacitance C (Farads).
- Fundamental Node Voltage Equation: $T_J - T_A = P_D \cdot \theta_{JA} = P_D \cdot (\theta_{JC} + \theta_{CS} + \theta_{SA})$.
- Equivalent Circuit Schematic: Current source P_D flowing through series resistors θ_{JC}, θ_{CS}, θ_{SA} anchored to ground potential T_A.

Mathematical Derivation of Fundamental Thermal Stability Condition

- Heat Generation Rate: $P_D = f(T_J)$ (power dissipated by the junction as a function of temperature).
- Heat Dissipation Rate (Removal): $P_R = \frac{T_J - T_A}{\theta_{JA}}$ (power transferred to ambient atmosphere).
- Thermal Equilibrium Condition: At steady state, $P_D = P_R \implies T_J = T_A + P_D\theta_{JA}$.
- Stability Criterion against Thermal Perturbation: To prevent runaway, the rate of increase of heat generation must be LESS than the rate of increase of heat removal.
- Mathematical Inequality: $\frac{\partial P_D}{\partial T_J} < \frac{\partial P_R}{\partial T_J} \implies \frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$.
- Physical Meaning: If $\frac{\partial P_D}{\partial T_J} \geq \frac{1}{\theta_{JA}}$, any infinitesimal temperature spike generates more heat than can be radiated, triggering runaway.

Collector Power Dissipation Derivative & Circuit Parameters

- Collector Power Dissipation: $P_D = V_{CE} I_C$.
- Chain Rule Expansion with respect to Junction Temperature T_J: $\frac{\partial P_D}{\partial T_J} = \frac{\partial (V_{CE} I_C)}{\partial T_J} = V_{CE} \frac{\partial I_C}{\partial T_J} + I_C \frac{\partial V_{CE}}{\partial T_J}$.
- Relating V_{CE} to I_C via KVL Loop: In a common emitter stage, $V_{CE} = V_{CC} - I_C(R_C + R_E) \implies \frac{\partial V_{CE}}{\partial I_C} = -(R_C + R_E)$.
- Substituting $\frac{\partial V_{CE}}{\partial T_J} = \frac{\partial V_{CE}}{\partial I_C} \frac{\partial I_C}{\partial T_J} = -(R_C + R_E) \frac{\partial I_C}{\partial T_J}$:
- Simplified Power Derivative: $\frac{\partial P_D}{\partial T_J} = V_{CE} \frac{\partial I_C}{\partial T_J} - I_C(R_C + R_E) \frac{\partial I_C}{\partial T_J} = \frac{\partial I_C}{\partial T_J} [V_{CE} - I_C(R_C + R_E)]$.

Derivation of the Self-Bias Thermal Stability Condition ($V_{CE} \leq \frac{1}{2}V_{CC}$)

- Expressing $I_C(R_C + R_E)$ from DC KVL: $I_C(R_C + R_E) = V_{CC} - V_{CE}$.
- Substitute into Power Derivative: $\frac{\partial P_D}{\partial T_J} = \frac{\partial I_C}{\partial T_J}[V_{CE} - (V_{CC} - V_{CE})] = \frac{\partial I_C}{\partial T_J}[2V_{CE} - V_{CC}]$.
- Evaluating Condition for Negative or Zero Heat Derivative ($\frac{\partial P_D}{\partial T_J} \leq 0$):
- Since $\frac{\partial I_C}{\partial T_J} > 0$, we require $2V_{CE} - V_{CC} \leq 0 \implies V_{CE} \leq \frac{1}{2}V_{CC}$.
- Engineering Consequence: When $V_{CE} < \frac{1}{2}V_{CC}$, any increase in I_C due to temperature causes V_{CE} to decrease so rapidly that total power $P_D = V_{CE}I_C$ ACTUALLY DECREASES! Thermal runaway becomes physically impossible.

Power Transistor Derating Curves & Maximum Dissipation

- Maximum Power Dissipation Rating ($P_{D,\max}$): Datasheet power rating specified at case temperature $T_C = 25^\circ\text{C}$, given by $P_{D,\max}(25^\circ\text{C}) = \frac{T_{J,\max} - 25^\circ\text{C}}{\theta_{JC}}$.
- Thermal Derating Region ($T_C > 25^\circ\text{C}$): As case/ambient temperature increases, allowable power dissipation decreases linearly to zero at $T_{J,\max}$.
- Power Derating Equation: $P_{D,\max}(T_A) = \frac{T_{J,\max} - T_A}{\theta_{JA}} = \frac{T_{J,\max} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$.
- Derating Slope Factor: Derating Factor $= \frac{1}{\theta_{JA}}$ (in $\text{W}/^\circ\text{C}$).
- Safe Operating Area (SOA): Enforces simultaneous constraints on maximum voltage $V_{CE,\max}$, peak current $I_{C,\max}$, thermal power dissipation limit $P_{D,\max}$, and secondary breakdown boundary.

Transient Thermal Impedance & Pulse Power Handling

- Thermal Mass & Heat Capacity: Semiconductor die and copper headers possess thermal capacitance $C_{th} = m \cdot c_p$ (Joules/°C).
- Transient Thermal Impedance $Z_{\theta JA}(t)$: For short power pulses ($t_p \ll \tau_{th}$), the effective thermal resistance is significantly lower than steady-state θ_{JA}.
- Thermal Time Constant: $\tau_{th} = \theta_{JA} \cdot C_{th}$. Typical die time constants range from 100 μs to 10 ms, while heat sinks range from 10 s to 100 s.
- Pulsed Power Application: Allows power transistors to handle transient peak power pulses (e.g. 500W for 1ms) far exceeding their continuous DC power rating (e.g. 50W).

Role of Emitter Resistor R_E and Stability Factor S in Preventing Thermal Runaway

- Collector Current Temperature Derivative: $\frac{\partial I_C}{\partial T_J} = S \cdot \frac{\partial I_{CO}}{\partial T_J} + S' \cdot \frac{\partial V_{BE}}{\partial T_J} + S'' \cdot \frac{\partial \beta}{\partial T_J}$.
- Impact of Stability Factor S: Minimizing S directly reduces $\frac{\partial I_C}{\partial T_J}$.
- Evaluating Thermal Runaway Criterion: $\left(S \frac{\partial I_{CO}}{\partial T_J} + S' \frac{\partial V_{BE}}{\partial T_J}\right)(2V_{CE} - V_{CC}) < \frac{1}{\theta_{JA}}$.
- Emitter Resistor Degeneration: Adding R_E increases total loop resistance $(R_C + R_E)$ and reduces S, providing dual protection against thermal runaway.
- Design Summary: Achieving thermal stability requires both appropriate electrical bias design $(S \leq 5)$ and proper physical thermal dissipation design (θ_{SA} sizing).

Numerical Example: Junction Temperature & Power Rating Calculation

- Given Parameters: Silicon power transistor with $T_{J,\max} = 175^\circ\text{C}$, $\theta_{JC} = 1.5^\circ\text{C/W}$. Mounted on heat sink with thermal washer $\theta_{CS} = 0.5^\circ\text{C/W}$ and heat sink rating $\theta_{SA} = 2.0^\circ\text{C/W}$. Ambient temperature $T_A = 40^\circ\text{C}$. Transistor dissipates $P_D = 30\,\text{W}$.
- Step 1: Calculate Total Thermal Resistance θ_{JA}:
  $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = 1.5 + 0.5 + 2.0 = 4.0^\circ\text{C/W}$.
- Step 2: Calculate Operating Junction Temperature T_J:
  $T_J = T_A + P_D \cdot \theta_{JA} = 40^\circ\text{C} + (30\,\text{W} \times 4.0^\circ\text{C/W}) = 40^\circ\text{C} + 120^\circ\text{C} = 160^\circ\text{C}$.
- Step 3: Evaluate Safety Margin: $T_J = 160^\circ\text{C} < T_{J,\max} = 175^\circ\text{C}$. The design operates safely with a 15°C thermal headroom.
- Step 4: Calculate Maximum Allowable Power at $T_A = 40^\circ\text{C}$: $P_{D,\max} = \frac{175-40}{4.0} = \frac{135}{4.0} = 33.75\,\text{W}$.

Numerical Example: Thermal Runaway Threshold Determination

- Given Circuit: BJT biased at $V_{CC} = 24\,\text{V}$, $V_{CE} = 16\,\text{V}$, $I_C = 1.5\,\text{A}$. $R_C + R_E = 5.33\,\Omega$. Total thermal resistance $\theta_{JA} = 3.0^\circ\text{C/W}$. Measured collector current drift rate $\frac{\partial I_C}{\partial T_J} = 12\,\text{mA}/^\circ\text{C} = 0.012\,\text{A}/^\circ\text{C}$.
- Step 1: Check V_{CE} relative to $\frac{1}{2}V_{CC}$: $\frac{1}{2}V_{CC} = 12\,\text{V}$. Since $V_{CE} = 16\,\text{V} > 12\,\text{V}$, $\frac{\partial P_D}{\partial T_J} > 0$ and thermal runaway is POSSIBLY RISKY.
- Step 2: Calculate Power Dissipation Derivative $\frac{\partial P_D}{\partial T_J}$: $\frac{\partial P_D}{\partial T_J} = \frac{\partial I_C}{\partial T_J}(2V_{CE} - V_{CC}) = 0.012\,\text{A}/^\circ\text{C} \times (2(16) - 24) = 0.012 \times (32 - 24) = 0.096\,\text{W}/^\circ\text{C}$.
- Step 3: Calculate Heat Dissipation Capability $\frac{1}{\theta_{JA}}$: $\frac{1}{\theta_{JA}} = \frac{1}{3.0^\circ\text{C/W}} = 0.333\,\text{W}/^\circ\text{C}$.
- Step 4: Test Thermal Stability Inequality: $\frac{\partial P_D}{\partial T_J} = 0.096\,\text{W}/^\circ\text{C} < \frac{1}{\theta_{JA}} = 0.333\,\text{W}/^\circ\text{C}$.
- Conclusion: The system is THERMALLY STABLE because heat removal capability ($0.333\,\text{W}/^\circ\text{C}$) exceeds internal heat generation growth ($0.096\,\text{W}/^\circ\text{C}$).

Summary & Core Principles of Thermal Design

- Thermal Runaway Mechanism: Uncontrolled thermal feedback loop driven by exponential I_{CO} and V_{BE} thermal drift.
- Thermal Resistance Network: Junction temperature $T_J = T_A + P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$.
- Universal Stability Criterion: Must enforce $\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$ under all operating conditions.
- Half-Supply Voltage Rule: Biasing at $V_{CE} \leq \frac{1}{2} V_{CC}$ makes $\frac{\partial P_D}{\partial T_J} \leq 0$, rendering thermal runaway physically impossible.
- Integrated Design Strategy: Combine electrical bias stabilization ($S \leq 5$) with properly sized heat sinking (low θ_{SA}) to guarantee lifetime reliability.