Lecture 17: Compensation techniques for bias stability

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Blueprint: Bias Compensation Topologies

- Thermal Drift Mechanisms & Mathematical Dependencies of $V_{BE}(T)$ and $I_{CO}(T)$.
- Diode Compensation Circuitry for V_{BE} Variations: Forward-Biased Diode In-Line Topology.
- Diode Compensation Circuitry for Leakage Current I_{CO}: Reverse-Biased Tracking Diode Topology.
- Thermistor (NTC) Compensation Networks: Circuit Analysis & Resistance Characteristics.
- Sensistor (PTC Silicon Resistor) Compensation Networks in Emitter & Base Circuits.
- Active Current Mirror Compensation in Integrated Analog Circuits & Monolithic Design.
- Comparative Analysis of Passive vs. Active Compensation & Numerical Worked Examples.

Thermal Drift Dynamics of V_{BE}, I_{CO}, and β in Transistors

- Temperature Dependence of V_{BE}: $V_{BE}(T) = V_{BE}(T_0) - k_V(T - T_0)$, where $k_V = \left|\frac{dV_{BE}}{dT}\right| \approx 2.5\,\text{mV}/^\circ\text{C}$.
- Temperature Dependence of Leakage Current: $I_{CO}(T) = I_{CO}(T_0) \cdot 2^{(T-T_0)/10}$, causing exponential growth in leakage power.
- Temperature Dependence of β: $\beta(T) = \beta(T_0)\,[1 + c_T(T - T_0)]$, where $c_T \approx 0.005 - 0.01\,/^\circ\text{C}$.
- Uncompensated Impact: In high-power or wide-temperature applications (-40°C to $+125^\circ$C), passive emitter degeneration alone cannot prevent severe Q-point shifting.

Diode Compensation for V_{BE} Variations: Circuit Operation & Analysis

- Circuit Topology: A forward-biased diode D made of the same semiconductor material (silicon) is connected in series with the base resistor R_B or supply V_{CC}.
- Base Current KVL Equation: $I_B = \frac{V_{CC} - V_D - V_{BE}}{R_B}$, where V_D is the forward voltage drop across the diode.
- Thermal Differential Equation: $\frac{dI_B}{dT} = \frac{1}{R_B}\left(-\frac{dV_D}{dT} - \frac{dV_{BE}}{dT}\right)$.
- Cancellation Condition: If the diode is thermally coupled to the transistor, $\frac{dV_D}{dT} = \frac{dV_{BE}}{dT} = -2.5\,\text{mV}/^\circ\text{C}$.
- Resulting Stability: $\frac{dI_B}{dT} = \frac{1}{R_B}\left(-(-2.5\,\text{mV}/^\circ\text{C}) - (-2.5\,\text{mV}/^\circ\text{C})\right) = 0$, holding I_B and I_C constant despite temperature changes.

Diode Compensation for Reverse Leakage Current I_{CO}

- Circuit Topology: A reverse-biased diode D_1 (fabricated on the same substrate) is connected in parallel with the base-emitter junction or base supply.
- Current Equilibrium Equation: $I_B = I_1 - I_R$, where I_1 is the supply bias current and $I_R = I_0(D_1)$ is the reverse saturation current of diode D_1.
- Collector Current Equation with Compensation: $I_C = \beta I_B + (1+\beta)I_{CO} = \beta(I_1 - I_0) + (1+\beta)I_{CO}$.
- Perfect Diode Matching ($I_0 = I_{CO}$): $I_C = \beta I_1 - \beta I_{CO} + (1+\beta)I_{CO} = \beta I_1 + I_{CO}$.
- Stability Factor Reduction: The multiplier for reverse leakage current is reduced from $(1+\beta)$ down to 1, yielding an effective $S \approx 1$.

Thermistor (NTC) Compensation Networks & Mathematical Formulation

- Negative Temperature Coefficient (NTC) Thermistor Law: $R_T(T) = R_0 \exp\left[B\left(\frac{1}{T} - \frac{1}{T_0}\right)\right]$, where B is the thermistor material constant ($3000\text{K} - 4500\text{K}$).
- Base Divider Topology: NTC thermistor R_T is placed in the lower branch (R_2) of the voltage divider network.
- Circuit Mechanism: As temperature rises, R_T drops exponentially $\implies$ $V_{TH} = V_{CC}\frac{R_T}{R_1+R_T}$ decreases $\implies$ V_B decreases.
- Collector Current Stabilization: The reduction in V_B decreases base current I_B, compensating for the rise in I_C caused by increasing β and I_{CO}.
- Design Formula: Select R_0 and B parameter such that $\frac{dV_{TH}}{dT} = \frac{dV_{BE}}{dT} + I_C\frac{dR_E}{dT}$.

Sensistor (PTC Silicon Resistor) Bias Compensation Networks

- Positive Temperature Coefficient (PTC) Sensistor Law: $R_S(T) = R_0\,[1 + \alpha(T - T_0)]$, where $lpha \approx +0.7\%$ to $+0.8\%\,/^{\circ}\mathrm{C}$ for heavily doped silicon.
- Emitter Degeneration Topology: Sensistor R_S is connected in series with or replaces the emitter resistor R_E.
- Circuit Mechanism: As temperature rises, R_S increases linearly $\implies$ Emitter degeneration voltage $V_E = I_E R_S$ increases dramatically.
- Negative Feedback Action: Higher V_E reduces base-emitter drive voltage $V_{BE,act} = V_B - V_E$, forcing base current I_B down and stabilizing I_C.
- Base Network Variant: Sensistor placed in series with upper divider resistor R_1 increases R_1 with temperature, lowering V_{TH}.

Active Current Mirror Compensation in Integrated Analog Circuits

- Integrated Circuit Limitation: Monolithic ICs cannot easily integrate large electrolytic bypass capacitors or precise thermistors.
- Current Mirror Topology: Two identical transistors (Q_1 reference, Q_2 output) fabricated on the same silicon die in close physical proximity.
- Reference Current Equation: $I_{REF} = \frac{V_{CC} - V_{BE1}}{R_{REF}}$.
- Output Current Scaling: $I_{OUT} = I_{C2} = I_{REF} \cdot \left(\frac{I_{S2}}{I_{S1}}\right) \frac{1}{1+\frac{2}{\beta}}$.
- Thermal Self-Compensation: Since Q_1 and Q_2 share identical temperature T, $V_{BE1}(T) = V_{BE2}(T)$ and $\beta_1(T) = \beta_2(T)$, making output bias current I_{OUT} virtually immune to temperature and β variations.

Comparative Performance Matrix: Passive vs. Active Compensation

- Emitter Resonator (R_E): Passive negative feedback; moderate stability ($S \approx 3 - 10$); causes AC gain reduction (unless bypassed).
- Diode Compensation (V_{BE}): Active element matching; high thermal tracking accuracy; excellent for class B/AB power stages.
- Diode Compensation (I_{CO}): Active leakage diversion; suppresses S to near 1; ideal for high-temperature germanium/silicon legacy systems.
- NTC Thermistor Network: Passive non-linear network; highly customizable temperature slope; slightly higher component tolerance spread.
- Sensistor Network: Passive linear PTC compensation; excellent linearity over $-55°C$ to $+150°C$; higher cost.
- Current Mirror: Active integrated compensation; near-zero temperature drift; ubiquitous in monolithic IC design.

Thermal Tracking and Component Matching Requirements

- Thermal Coupling Necessity: Compensation diodes or sensing elements MUST be mounted on the same heat sink or semiconductor substrate as the power transistor.
- Thermal Resistance Delay: Spatial separation introduces a thermal time constant $\tau_{th} = R_{th}C_{th}$, causing transient Q-point drift during rapid thermal cycling.
- Semiconductor Junction Matching: Diode forward voltage V_D and V_{BE} must match within $\pm 5\,\text{mV}$ across the entire temperature spectrum.
- Isothermal Layout in ICs: Symmetric placement and common-centroid layout techniques are enforced to eliminate thermal gradients across mirror pairs.

Mathematical Sensitivity Analysis of Compensated Bias Networks

- Compensated Sensitivity Equation: $dI_C = S \cdot dI_{CO} + S' \cdot (dV_{BE} - dV_{comp}) + S'' \cdot d\beta$.
- Ideal Cancellation Condition for V_{BE}: Set $dV_{comp} = dV_{BE} \implies S' \cdot (0) = 0$.
- Sensitivity Reduction Factor: $\eta_{comp} = 1 - \frac{\Delta I_{C,\text{compensated}}}{\Delta I_{C,\text{uncompensated}}}$.
- Typical Performance: High-grade diode compensation achieves $\eta_{comp} > 90\%$, restricting Q-point shift to within $\pm 3\%$ over a 100°C temperature span.

Numerical Example: Diode-Compensated Class AB Power Stage

- Given Parameters: Power BJT with $V_{BE} = 0.7\,\text{V}$ at 25°C, $\frac{dV_{BE}}{dT} = -2.2\,\text{mV}/^\circ\text{C}$. Supply $V_{CC} = 20\,\text{V}$, $R_B = 1.8\,\text{k}\Omega$, $\beta = 80$. Temperature rises to 75°C ($\Delta T = 50^\circ\text{C}$).
- Uncompensated Case: $\Delta V_{BE} = -2.2\,\text{mV}/^\circ\text{C} \times 50^\circ\text{C} = -110\,\text{mV} = -0.11\,\text{V}$.
  $\Delta I_B = \frac{0.11\,\text{V}}{1.8\,\text{k}\Omega} = 61.1\,\mu\text{A} \implies \Delta I_C = 80 \times 61.1\,\mu\text{A} = 4.89\,\text{mA}$.
- Compensated Case (Diode in Series): Diode drop changes by
  $\Delta V_D = -2.2\,\text{mV}/^\circ\text{C} \times 50^\circ\text{C} = -0.11\,\text{V}$.
- Net Voltage across R_B:
  $V_{RB} = V_{CC} - V_D - V_{BE} = 20 - (0.7 - 0.11) - (0.7 - 0.11) = 20 - 0.59 - 0.59 = 18.82\,\text{V}$
  (unchanged from 25°C!).
- Result: $\Delta I_B = 0 \implies \Delta I_C = 0\,\text{mA}$ due to V_{BE} drift, completely preventing thermal bias creep.

Design Problem: NTC Thermistor Selection for Temperature Stabilization

- Problem Statement: Select an NTC thermistor for a base divider network ($R_1 = 10\,\text{k}\Omega$) to maintain $V_B = 2.0\,\text{V}$ at 25°C and drop V_B to 1.85 V at 75°C. Supply $V_{CC} = 12\,\text{V}$.
- Step 1: Calculate Thermistor Resistance at 25°C (298.15 K):
  $V_B = 2.0 = 12 \times \frac{R_T(25)}{10\,\text{k}\Omega + R_T(25)} \implies R_T(25) = 2.0\,\text{k}\Omega.$
- Step 2: Calculate Required Thermistor Resistance at 75°C (348.15 K):
  $V_B = 1.85 = 12 \times \frac{R_T(75)}{10\,\text{k}\Omega + R_T(75)} \implies R_T(75) = 1.822\,\text{k}\Omega.$
- Step 3: Calculate Required B Constant:
  $\ln\left(\frac{R_T(75)}{R_T(25)}\right) = B\left(\frac{1}{348.15} - \frac{1}{298.15}\right) \implies \ln(0.911) = B(-0.0004818) \implies B = 193\,\text{K}.$
- Engineering Selection: Pair standard 2.2 kΩ NTC ($B = 3950\,\text{K}$) with parallel fixed resistor to match target slope.

Summary & Selection Criteria for Compensation Networks

- Diode Compensation (V_{BE}): Best for Class A/AB audio & RF power amplifiers; matches linear junction drop $-2.5\,\text{mV}/^{\circ}\text{C}$.
- Diode Compensation (I_{CO}): Best for high-leakage legacy or high-temperature power transistors; suppresses S multiplier to 1.
- NTC/PTC Networks: Highly flexible passive compensation for custom temperature profiling over extended environmental ranges.
- Current Mirrors: Universal standard for monolithic integrated analog circuits (Op-Amps, OTAs, RFICs).
- Golden Design Rule: Always ensure intimate thermal coupling between compensation sensors and power devices to prevent thermal lag.