Lecture 16: Stability Factor: Definition and features

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Blueprint: Stability Factor Analysis

- Physical Mechanisms of Q-Point Instability & Thermal Sensitivity Parameters.
- Total Differential Formulation of Collector Current $I_C = f(I_{CO}, V_{BE}, \beta)$.
- Mathematical Derivation of Primary Stability Factor $S \equiv \frac{\partial I_C}{\partial I_{CO}}$.
- Mathematical Formulations of Secondary Stability Factors $S'(V_{BE})$ and $S''(\beta)$.
- Derivation & Evaluation of S for Fixed Bias, Collector-to-Base Bias, and Voltage Divider Bias Topologies.
- Design Rules for Minimizing Stability Factors ($R_{TH}/R_E \ll \beta$) & Numerical Worked Examples.

Physical Origin of Q-Point Shift & Thermal Sensitivity

- Reverse Leakage Current Drift: I_{CO} doubles approximately every 10°C rise in silicon junction temperature, governed by $I_{CO}(T) = I_{CO}(T_0) \cdot 2^{(T-T_0)/10}$.
- Base-Emitter Voltage Thermal Coefficient: V_{BE} decreases linearly with temperature at approximately $-2.5\,\text{mV}/^\circ\text{C}$, expressed mathematically as $\frac{dV_{BE}}{dT} \approx -2.5\,\text{mV}/^\circ\text{C}$.
- Common-Emitter Current Gain Sensitivity: $\beta = h_{FE}$ increases with temperature at approximately $+0.5\%$ to $+1\%$ per °C due to enhanced minority carrier mobility and lifetime.
- Cumulative Shift in Operating Point: Unchecked shifts in I_C push the Q-point toward saturation ($V_{CE} \to 0$) or cutoff ($I_C \to 0$), severely clipping the AC signal.

Fundamental Collector Current Equation & Total Differential

- General BJT Collector Current Equation: $I_C = \beta I_B + (1+\beta) I_{CO}$, accounting for both base injection current and reverse saturation leakage.
- Total Differential Formulation: $dI_C = \left(\frac{\partial I_C}{\partial I_{CO}}\right) dI_{CO} + \left(\frac{\partial I_C}{\partial V_{BE}}\right) dV_{BE} + \left(\frac{\partial I_C}{\partial \beta}\right) d\beta$.
- Definition of Partial Sensitivity Factors: $dI_C = S \cdot dI_{CO} + S' \cdot dV_{BE} + S'' \cdot d\beta$.
- Superposition Assumption: For small temperature excursions, total quiescent current drift ΔI_C is the linear sum of independent contributions from ΔI_{CO}, ΔV_{BE}, and $\Delta \beta$.

Primary Stability Factor $S(I_{CO})$: General Derivation

- Definition of Primary Stability Factor: $S \equiv \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\beta=\text{const}}$.
- Differentiating $I_C = \beta I_B + (1+\beta) I_{CO}$ with respect to I_C: $1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$.
- Rearranging for $\frac{\partial I_C}{\partial I_{CO}}$ yields the Universal Stability Equation: $S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$.
- Physical Interpretation: $\frac{\partial I_B}{\partial I_C}$ represents the circuit feedback ratio. A negative feedback ratio $\frac{\partial I_B}{\partial I_C} < 0$ increases the denominator, suppressing S toward its ideal minimum value of 1.

Secondary Stability Factors: $S'(V_{BE})$ and $S''(\beta)$

- Definition of $S'(V_{BE})$: $S' \equiv \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta=\text{const}} = \frac{-\beta/R_{TH}}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{-\beta}{R_{TH}+(1+\beta)R_E}$ (for self-bias).
- Definition of $S''(\beta)$: $S'' \equiv \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},V_{BE}=\text{const}} = \frac{\partial}{\partial \beta}\left[\frac{\beta(V_{TH}-V_{BE})}{R_{TH}+(1+\beta)R_E}\right] = \frac{I_{C1}}{\beta_1(1+\beta_2)} \cdot S_2$.
- Interdependence of Stability Factors: High-stability networks (low S) automatically reduce S' and S'' due to shared denominator terms containing R_E feedback.
- Units and Dimensions: S is dimensionless ($1 \leq S \leq 1+\beta$), S' has units of mA/V (Ω^{-1}), and S'' has units of mA per unit change in β.

Stability Factor S Evaluation: Fixed Bias Circuit

- Fixed Bias KVL Equation: $V_{CC} - I_B R_B - V_{BE} = 0 \implies I_B = \frac{V_{CC} - V_{BE}}{R_B}$.
- Feedback Partial Derivative: Since I_B is completely independent of I_C, $\frac{\partial I_B}{\partial I_C} = 0$.
- Substitution into Universal Formula: $S = \frac{1+\beta}{1-\beta(0)} = 1 + \beta$.
- Numerical Impact: For a transistor with $\beta = 100$, $S = 101$. Any increase in leakage current ΔI_{CO} is multiplied by 101 into ΔI_C, making Fixed Bias extremely thermally unstable.

Stability Factor S Evaluation: Collector-to-Base Feedback Bias

- Collector-to-Base Bias KVL Equation: $V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$.
- Base Current Expression: $I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$.
- Feedback Partial Derivative: $\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B + R_C}$.
- Stability Factor Derivation: $S = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_B+R_C}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}$.
- Performance Bounds: As $R_B \to 0$, $S \to 1$. However, small R_B heavily loads the input AC signal, creating a fundamental trade-off between stability and AC voltage gain.

Stability Factor S Evaluation: Self Bias (Voltage Divider with R_E)

- Thévenin Equivalent Network: $V_{TH} = V_{CC}\frac{R_2}{R_1+R_2}$, $R_{TH} = R_1 \parallel R_2 = \frac{R_1R_2}{R_1+R_2}$.
- Thévenin Loop KVL Equation: $V_{TH} - I_B R_{TH} - V_{BE} - (I_C + I_B)R_E = 0$.
- Differentiating KVL with respect to I_C: $0 - \frac{\partial I_B}{\partial I_C}R_{TH} - 0 - R_E - \frac{\partial I_B}{\partial I_C}R_E = 0 \implies \frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_{TH}+R_E}$.
- Exact Stability Factor Formula: $S = \frac{(1+\beta)\left(1+\frac{R_{TH}}{R_E}\right)}{1+\beta+\frac{R_{TH}}{R_E}}$.
- Asymptotic Analysis: If $R_{TH}/R_E \ll 1$, then $S \to \frac{(1+\beta)(1)}{1+\beta} = 1$ (ideal thermal stability).

Optimization Strategy: Minimizing S via R_{TH}/R_E Trade-offs

- Design Rule of Thumb: To achieve $S \ll 1 + \beta$, enforce $R_{TH} \leq 0.1 \cdot \beta R_E$ or $R_{TH}/R_E \approx 10$.
- Constraint 1 — DC Bias Stability: Lowering R_{TH} reduces S toward 1, maximizing immunity against thermal runaway.
- Constraint 2 — AC Input Impedance: R_{TH} appears in parallel with transistor input impedance $R_{in} = r_p + (1 + \beta)r_e$. Excessively small R_{TH} shunts the AC signal current to ground.
- Constraint 3 — Power Dissipation: Low R_1, R_2 resistor values increase static standing current drawn directly from the V_{CC} power supply.
- Optimal Balance: Choose R_E to drop 1 V to 2 V ($V_E \approx 0.1 V_{CC}$) and set $R_{TH} = 0.1\beta R_E$ to achieve $S \approx 5 - 10$.

Comparative Matrix of Biasing Topologies & Stability Margins

- Fixed Bias: $S = 1 + \beta$. Extremely poor stability; highly sensitive to temperature and β; simplest component count (1 resistor).
- Collector Feedback Bias: $S = \frac{1+\beta}{1+\beta\frac{R_C}{R_B+R_C}}$. Moderate stability; sensitive to AC voltage gain degradation unless bypassed; 2 resistors.
- Voltage Divider Bias (Self Bias): $S = \frac{(1+\beta)(1+R_{TH}/R_E)}{1+\beta+R_{TH}/R_E}$. Superior thermal stability ($S \approx 2-10$); independent of β variations if $R_{TH}/R_E \ll \beta$; standard industrial choice.
- Emitter Bias (Dual Supply $\pm V$): $S = \frac{(1+\beta)(1+R_B/R_E)}{1+\beta+R_B/R_E}$. Excellent stability; allows direct coupling; requires dual power supply rails.

Numerical Example: Calculating S, S', and S'' for Voltage Divider Bias

- Given Parameters: $V_{CC} = 12\,\text{V}$, $R_1 = 33\,\text{k}\Omega$, $R_2 = 4.7\,\text{k}\Omega$, $R_C = 2.2\,\text{k}\Omega$, $R_E = 1\,\text{k}\Omega$, $\beta = 100$, $V_{BE} = 0.7\,\text{V}$.
- Step 1: Calculate Thévenin Equivalent: $V_{TH} = 12 \times \frac{4.7}{33+4.7} = 1.496\,\text{V}$; $R_{TH} = \frac{33\times4.7}{33+4.7} = 4.11\,\text{k}\Omega$.
- Step 2: Calculate Ratio R_{TH}/R_E: $\frac{R_{TH}}{R_E} = \frac{4.11\,\text{k}\Omega}{1\,\text{k}\Omega} = 4.11$.
- Step 3: Calculate Primary Stability Factor S: $S = \frac{(1+100)(1+4.11)}{1+100+4.11} = \frac{101\times5.11}{105.11} = 4.91$.
- Step 4: Calculate $S'(V_{BE})$: $S' = \frac{-\beta}{R_{TH}+(1+\beta)R_E} = \frac{-100}{4.11\,\text{k}\Omega+101\,\text{k}\Omega} = -0.951\,\text{mA/V}$.
- Conclusion: $S = 4.91 \ll 101$, demonstrating robust thermal stabilization where leakage current multiplication is reduced by over 95%.

Design Problem: Sizing R_E and R_{TH} for Target Stability $S \leq 5$

- Design Problem Statement: Design a Voltage Divider Bias network for $V_{CC} = 15\,\text{V}$, $I_{CQ} = 2\,\text{mA}$, $V_{CEQ} = 7.5\,\text{V}$, $\beta = 120$, requiring $S \leq 5.0$.
- Step 1: Emitter Voltage Selection: Allocate $V_E = 0.1 V_{CC} = 1.5\,\text{V}$. Therefore, $R_E = \frac{V_E}{I_{CQ}} = \frac{1.5\,\text{V}}{2\,\text{mA}} = 750\,\Omega$.
- Step 2: Solve Stability Equation for R_{TH}: $S = 5 = \frac{(1+120)(1+R_{TH}/750)}{1+120+R_{TH}/750} \implies 5(121 + R_{TH}/750) = 121(1 + R_{TH}/750)$.
- Step 3: Algebraic Solution: $605 + 5(R_{TH}/750) = 121 + 121(R_{TH}/750) \implies 484 = 116(R_{TH}/750) \implies R_{TH} = 3129\,\Omega = 3.13\,\text{k}\Omega$.
- Step 4: Calculate Divider Resistors R_1, R_2: $V_{TH} = V_{BE} + V_E = 0.7 + 1.5 = 2.2\,\text{V}$. $R_1 = R_{TH}\frac{V_{CC}}{V_{TH}} = 3.13\,\text{k}\Omega \times \frac{15}{2.2} = 21.34\,\text{k}\Omega$; $R_2 = \frac{R_1 R_{TH}}{R_1 - R_{TH}} = 3.54\,\text{k}\Omega$.

Summary & Engineering Best Practices for Bias Stability

- Stability Factor Definitions: $S = \partial I_C / \partial I_{CO}$, $S' = \partial I_C / \partial V_{BE}$, $S'' = \partial I_C / \partial \beta$.
- Universal Stability Formula: $S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)}$. Stability depends directly on negative feedback factor $\partial I_B / \partial I_C$.
- Topology Hierarchy: Voltage Divider Bias ($S \approx 3-5$) ¿ Collector Feedback ($S \approx 10-20$) ¿¿¿ Fixed Bias ($S = 1+\beta \approx 100+$).
- Golden Rule of Stable Design: Select $R_E \geq 0.1 V_{CC}/I_C$ and enforce $R_{TH} \leq 0.1\beta R_E$ to guarantee small S and prevent thermal runaway.