Lecture 15: Biasing Methods

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Plan: Biasing Methods Breakdown

- Overview and Selection Criteria for BJT Biasing Networks
- Method 1: Fixed Bias (Base Bias) — Derivation, Drawbacks, and Instability
- Method 2: Collector-to-Base Feedback Bias — Negative Feedback Mechanism
- Method 3: Emitter-Feedback Bias (Fixed Bias with R_E) — DC Degeneration
- Method 4: Voltage Divider Bias (Self Bias) — Detailed Thevenin Analysis
- Design Protocol for Voltage Divider Bias (R_E, R_{Th}, R_1, R_2 Selection)
- Quantitative Comparison of Stability Factors (S) across Topologies
- Worked Numerical Problem 1: Fixed Bias vs Voltage Divider Bias Drift
- Worked Numerical Problem 2: Designing a Voltage Divider Bias Circuit
- Comparative Matrix & Final Selection Guidelines

Method 1: Fixed Bias Circuit Analysis

- Circuit Configuration: Base resistor R_B connected directly between DC supply V_{CC} and base terminal. Collector resistor R_C connected between V_{CC} and collector. Emitter tied to ground.
- Base Current Equation: Applying KVL around base-emitter loop: $V_{CC} - I_{BQ}R_B - V_{BE} = 0 \implies I_{BQ} = \frac{V_{CC}-V_{BE}}{R_B}$.
- Collector Current & Voltage: $I_{CQ} = \beta_{DC} I_{BQ} = \beta \left(\frac{V_{CC}-V_{BE}}{R_B} \right)$. Collector-emitter voltage: $V_{CEQ} = V_{CC} - I_{CQ}R_C$.
- Stability Factor Derivation: Since I_{BQ} is independent of I_{CQ}, $\frac{\partial I_B}{\partial I_C} = 0$. Substituting into general formula: $S = \frac{1+\beta}{1-\beta(0)} = 1 + \beta$.
- Critical Failure Mode: Maximum possible thermal instability ($S = 1 + \beta$). Any rise in temperature or change in transistor β causes severe Q-point shift directly into saturation.

Method 2: Collector-to-Base Feedback Bias

- Circuit Configuration: Base resistor R_B is connected to the collector terminal instead of V_{CC}, introducing negative feedback.
- Base Loop KVL Equation: $V_{CC} - (I_{CQ} + I_{BQ})R_C - I_{BQ}R_B - V_{BE} = 0$.
- Base Current Formula: Assuming $I_{CQ} \gg I_{BQ}$: $I_{BQ} = \frac{V_{CC}-V_{BE}}{R_B+\beta R_C}$.
- Collector Current Formula: $I_{CQ} = \frac{\beta(V_{CC}-V_{BE})}{R_B+\beta R_C} = \frac{V_{CC}-V_{BE}}{\frac{R_B}{\beta}+R_C}$.
- Stabilization Mechanism: If $T \uparrow \implies I_C \uparrow \implies V_C = (V_{CC} - I_C R_C) \downarrow \implies I_B \downarrow \implies I_C \downarrow$ (restores equilibrium).
- Stability Factor S: Derivative $\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B+R_C} \implies S = \frac{1+\beta}{1+\beta\frac{R_C}{R_B+R_C}}$. Achieves moderate stability ($S < 1 + \beta$).

Method 3: Emitter Bias (Fixed Bias with R_E)

- Circuit Topology: Single base resistor R_B to V_{CC}, collector resistor R_C to V_{CC}, and an emitter resistor R_E connected between emitter and ground.
- Input Loop KVL Equation: $V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$.
- Base Current Equation: Since $I_E = (1+\beta) I_B$: $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$.
- Collector Current Equation: $I_{CQ} = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1+\beta) R_E} \approx \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_E}$.
- Stability Factor S: Derivative $\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E} \implies S = \frac{1+\beta}{1+\beta \frac{R_E}{R_B + R_E}}$.
- Condition for β-Independence: If $(1+\beta) R_E \gg R_B$, $I_{CQ} \approx \frac{V_{CC} - V_{BE}}{R_E}$, making collector current nearly independent of transistor β.

Method 4: Voltage Divider Bias (Self-Bias)

- Circuit Topology: Two resistors R_1 and R_2 form a potential divider across V_{CC} to establish a fixed base voltage V_B. Resistors R_C and R_E set collector and emitter currents.
- Thevenin Network Reduction (Base Input): - Thevenin Voltage: $V_{Th} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right)$. - Thevenin Resistance: $R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1+R_2}$.
- Thevenin Base Loop KVL Equation: $V_{Th} - I_{BQ}R_{Th} - V_{BE} - I_{EQ}R_E = 0$.
- Exact Collector Current Equation: $I_{CQ} = \frac{\beta(V_{Th}-V_{BE})}{R_{Th}+(1+\beta)R_E} = \frac{V_{Th}-V_{BE}}{\frac{R_{Th}}{\beta}+\left(\frac{1+\beta}{\beta}\right)R_E}$.
- Approximate Formula (Practical Design Condition): When $(1+\beta)R_E \gg R_{Th}$ (or $R_{Th} \leq 0.1\beta R_E$), $I_B R_{Th} \approx 0$, yielding: $V_B \approx V_{Th} \implies I_{CQ} \approx I_{EQ} = \frac{V_{Th}-V_{BE}}{R_E}$.

Detailed Design Procedure for Voltage Divider Bias

- Step 1 (Select Supply and Q-Point): Choose supply voltage V_{CC} and target quiescent values I_{CQ} and V_{CEQ} (typically $V_{CEQ} \approx 0.5V_{CC}$).
- Step 2 (Select Emitter Resistor R_E): Allocate 10% to 20% of supply voltage across emitter resistor for robust thermal stability: $V_E = I_{EQ}R_E \approx 0.1V_{CC} \implies R_E = \frac{0.1V_{CC}}{I_{CQ}}$.
- Step 3 (Calculate Collector Resistor R_C): Apply output loop KVL: $R_C = \frac{V_{CC}-V_{CEQ}-V_E}{I_{CQ}}$.
- Step 4 (Calculate Base Voltage V_B): $V_B = V_E + V_{BE} = 0.1V_{CC} + 0.7$ V.
- Step 5 (Select Base Divider Resistors R_1, R_2): - Apply stability rule: $R_{Th} \leq 0.1\beta R_E \implies R_1 \parallel R_2 = 0.1\beta R_E$. - Divider current rule: Set divider current $I_{\text{div}} = \frac{V_{CC}}{R_1+R_2} \geq 10I_B$. - Calculate $R_2 = \frac{V_B}{10I_B}$ and $R_1 = \frac{V_{CC}-V_B}{10I_B}$.

Comparative Stability Factor (S) Equations

- Fixed Bias: $S = 1 + \beta$. Maximum instability ($S \approx 100$ to 300). Zero feedback.
- Collector Feedback Bias: $S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}$. Moderate stability ($S \approx 15$ to 40). Voltage feedback.
- Emitter Bias: $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$. Good stability if $R_E \gg R_B/\beta$ ($S \approx 10$ to 25). Current feedback.
- Voltage Divider Bias: $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_{Th}+R_E}\right)}$. Excellent stability ($S < 10$). Best performance when $R_{Th} \ll \beta R_E$.
- Asymptotic Limit of Voltage Divider Bias: As $R_{Th}/R_E \to 0$, $S \to 1 + \frac{R_{Th}}{R_E} \approx 1$ (the theoretical minimum ideal stability factor).

Worked Example: Q-Point Drift Comparison

- Problem Statement: Compare the change in I_{CQ} when β increases from 100 to 200 (100% increase) for: 1. Fixed Bias circuit with $V_{CC} = 12$ V, $R_B = 220$ kΩ, $R_C = 2.2$ kΩ. 2. Voltage Divider Bias circuit with $V_{CC} = 12$ V, $R_1 = 39$ kΩ, $R_2 = 10$ kΩ, $R_C = 2.2$ kΩ, $R_E = 1.0$ kΩ.
- Fixed Bias Analysis: - At $\beta = 100$: $I_{BQ} = \frac{12-0.7}{220\ \text{k}\Omega} = 51.36\ \mu\text{A} \implies I_{CQ1} = 100 \times 51.36\ \mu\text{A} = 5.136$ mA. - At $\beta = 200$: $I_{CQ2} = 200 \times 51.36\ \mu\text{A} = 10.272$ mA (100% INCREASE in I_C, driving circuit into saturation!).
- Voltage Divider Bias Analysis: - $V_{Th} = 12 \times \frac{10}{49} = 2.449$ V; $R_{Th} = \frac{39 \times 10}{49}\ \text{k}\Omega = 7.959$ kΩ. - At $\beta = 100$: $I_{CQ1} = \frac{100(2.449-0.7)}{7.959\ \text{k}\Omega + 101(1\ \text{k}\Omega)} = \frac{174.9\ \text{V}}{108.96\ \text{k}\Omega} = 1.605$ mA. - At $\beta = 200$: $I_{CQ2} = \frac{200(2.449-0.7)}{7.959\ \text{k}\Omega + 201(1\ \text{k}\Omega)} = \frac{349.8\ \text{V}}{208.96\ \text{k}\Omega} = 1.674$ mA.
- Comparison Conclusion: - Fixed Bias I_C drift: +100% (5.14 mA → 10.27 mA). - Voltage Divider Bias I_C drift: ONLY +4.3% (1.605 mA → 1.674 mA). Proves total stability!

Worked Example: Designing a Voltage Divider Bias Network

- Design Specification: Design a Voltage Divider Bias circuit for a silicon NPN BJT ($\beta = 120$, $V_{BE} = 0.7$ V) operating from $V_{CC} = 15$ V to set Q-point at $I_{CQ} = 2.0$ mA and $V_{CEQ} = 7.5$ V.
- Step 1 (Select V_E & Calculate R_E): Set $V_E = 0.1 V_{CC} = 0.1 \times 15$ V $= 1.5$ V. $R_E = \frac{V_E}{I_{CQ}} = \frac{1.5 \text{ V}}{2.0 \text{ mA}} = 750\ \Omega$ (Standard value: 750 Ω).
- Step 2 (Calculate R_C): Output loop KVL: $V_{CC} - I_{CQ} R_C - V_{CEQ} - V_E = 0$. $R_C = \frac{V_{CC} - V_{CEQ} - V_E}{I_{CQ}} = \frac{15 \text{ V} - 7.5 \text{ V} - 1.5 \text{ V}}{2.0 \text{ mA}} = \frac{6.0 \text{ V}}{2.0 \text{ mA}} = 3.0$ kΩ (Standard value: 3.0 kΩ).
- Step 3 (Calculate Base Voltage V_B): $V_B = V_E + V_{BE} = 1.5 \text{ V} + 0.7 \text{ V} = 2.2$ V.
- Step 4 (Determine R_1 and R_2): - Base current $I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{2.0 \text{ mA}}{120} = 16.67\ \mu$A. - Set divider current $I_{\text{div}} = 10 I_{BQ} = 166.7\ \mu$A. - $R_2 = \frac{V_B}{I_{\text{div}}} = \frac{2.2 \text{ V}}{166.7\ \mu\text{A}} = 13.2$ kΩ (Standard value: 13 kΩ). - $R_1 = \frac{V_{CC} - V_B}{I_{\text{div}}} = \frac{15 \text{ V} - 2.2 \text{ V}}{166.7\ \mu\text{A}} = \frac{12.8 \text{ V}}{166.7\ \mu\text{A}} = 76.8$ kΩ (Standard value: 75 kΩ).

Input Impedance Trade-Offs Across Biasing Topologies

- Fixed Bias Input Resistance (R_{in}): Base resistor R_B is connected in parallel with transistor input AC resistance $r_\pi = \beta r_e$: $R_{in} = R_B \parallel r_\pi \approx r_\pi$. Offers highest input impedance because R_B is very large (100 kΩ to 1 MΩ).
- Collector Feedback Input Resistance (R_{in}): Miller effect reduces effective base resistance: $R_{in} = \left(\frac{R_B}{1+A_v}\right) \parallel r_\pi$, significantly reducing input impedance.
- Voltage Divider Bias Input Resistance (R_{in}): Parallel combination of base divider resistors and transistor input impedance: $R_{in} = R_1 \parallel R_2 \parallel [r_\pi + (1+\beta)R'_E]$. For unbypassed emitter, R_{in} is high; for bypassed emitter (C_E shorts R_E), $R_{in} = R_1 \parallel R_2 \parallel r_\pi = R_{Th} \parallel r_\pi$.
- Design Trade-Off: High stability requires small R_{Th} ($R_{Th} \leq 0.1\beta R_E$), which lowers input impedance R_{in}. Engineers balance stability against loading effects.

Comprehensive Biasing Topology Comparison Matrix

- Comparison Parameters Across All 4 Methods: 1. Component Count: Fixed (2 resistors), Collector Feedback (2), Emitter Bias (3), Voltage Divider (4 resistors). 2. Stability Factor S: Fixed $(1+\beta)$, Collector Feedback $(\frac{1+\beta}{1+\beta R_C/(R_B+R_C)})$, Emitter Bias $(\frac{1+\beta}{1+\beta R_E/(R_B+R_E)})$, Voltage Divider $(\approx 1+R_{Th}/R_E)$. 3. β-Dependency: Fixed (Extreme), Collector Feedback (Moderate), Emitter Bias (Low if $\beta R_E \gg R_B$), Voltage Divider (Negligible if $R_{Th} \leq 0.1\beta R_E$). 4. Negative Feedback Type: Fixed (None), Collector Feedback (Voltage Feedback), Emitter Bias (Current Feedback), Voltage Divider (Current Feedback via R_E). 5. Industrial Usage: Fixed (Switching only), Collector Feedback (Simple amplifiers), Emitter Bias (Rare), Voltage Divider (Universal standard).

Summary of Lecture 15 & Unit 2 Conclusion

- Biasing Topologies Evaluated: Fixed Bias, Collector Feedback, Emitter Bias, and Voltage Divider Bias.
- Stability Superiority: Voltage Divider Bias achieves minimum stability factor $S \approx 1 + R_{Th}/R_E$, rendering the Q-point immune to thermal drift and transistor β variations.
- Thevenin Analysis: Simplifies voltage divider bias into $V_{Th} = V_{CC}R_2/(R_1 + R_2)$ and $R_{Th} = R_1 \parallel R_2$, yielding $I_{CQ} \approx (V_{Th} - V_{BE})/R_E$.
- Design Rules Mastered: $V_E = 0.1V_{CC}$, $R_{Th} \leq 0.1\beta R_E$, $V_{CEQ} \approx 0.5V_{CC}$.
- Unit 2 Mastery Complete: Established comprehensive understanding of DC biasing, thermal stability, load line mechanics, and circuit design principles.