Lecture 14: The Load Lines: D

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Plan: Dynamic Design & Power Efficiency

- Dynamic Load Line Mechanics across Transistor Configurations (CE, CC, CB)
- AC Collector Power Output Calculation (P_{ac})
- DC Supply Power (P_{dc}) and Transistor Collector Dissipation (P_C)
- Derivation of Series-Fed Class-A Amplifier Efficiency ($\eta = P_{ac}/P_{dc}$)
- Transformer-Coupled Class-A Load Lines and Efficiency Limit (50%)
- Dynamic Q-Point Shift under Large-Signal Overdrive
- Thermal Hyperbola and Transistor Power Dissipation Ratings ($P_{D(\max)}$)
- Design Problem 1: Designing Biasing for Target AC Power Output
- Design Problem 2: Symmetrical Swing Optimization with Real-World Tolerances
- Summary & Practical Engineering Principles

Dynamic Load Lines Across BJT Configurations

- Common-Emitter (CE) Configuration: Highest combined voltage and current gain. DC load resistance $R_{DC} = R_C + R_E$, AC load resistance $r_c = R_C \parallel R_L$. High input impedance, inverted output AC phase (180°).
- Common-Collector (CC / Emitter Follower): Unity voltage gain ($A_v \approx 1$), high current gain ($\beta + 1$). Collector tied to DC supply ($R_C = 0$). Load resistor R_L is placed in emitter circuit. $R_{DC} = R_E$, $r_e = R_E \parallel R_L$. AC load line equation: $i_e - I_{EQ} = -\frac{1}{r_e}(v_{ce} - V_{CEQ})$.
- Common-Base (CB) Configuration: High voltage gain, unity current gain ($\alpha \approx 1$). Low input impedance, high output impedance. Used in high-frequency RF amplification. $R_{DC} = R_C + R_E$, $r_c = R_C \parallel R_L$.

AC Power Output Derivation (P_{ac})

- RMS Signal Quantities: For a sinusoidal AC signal, RMS voltage across load r_c is $V_{ce(rms)} = \frac{V_{ce(peak)}}{\sqrt{2}}$ and RMS current is $I_{c(rms)} = \frac{I_{c(peak)}}{\sqrt{2}}$.
- AC Power Delivered to Load Resistance (P_{ac}): $P_{ac} = V_{ce(rms)} \cdot I_{c(rms)} = \frac{V_{ce(peak)}}{\sqrt{2}} \cdot \frac{I_{c(peak)}}{\sqrt{2}} = \frac{V_{ce(peak)} \cdot I_{c(peak)}}{2}$.
- Peak-to-Peak Expression: Expressing in terms of peak-to-peak voltage $V_{o(p-p)}$ and current $I_{o(p-p)}$: $P_{ac} = \frac{V_{o(p-p)} \cdot I_{o(p-p)}}{8} = \frac{V_{o(p-p)}^2}{8 r_c}$.
- Maximum Unclipped AC Power Output: Under maximum unclipped symmetrical swing condition ($V_{ce(peak)} = V_{CEQ}, I_{c(peak)} = I_{CQ}$): $P_{ac(\max)} = \frac{V_{CEQ} \cdot I_{CQ}}{2}$.

DC Power Supply & Collector Dissipation

- Total DC Power Input (P_{dc}): Supplied by the DC voltage source V_{CC} to the entire amplifier circuit: $P_{dc} = V_{CC} \cdot I_{CC} \approx V_{CC} \cdot I_{CQ}$ (neglecting minor base bias current).
- DC Power Dissipated in Resistors (P_R): Power consumed as heat in collector and emitter resistors: $P_R = I_{CQ}^2(R_C + R_E) = I_{CQ}^2 R_{DC}$.
- Collector Junction Power Dissipation (P_C): Under zero AC signal conditions, transistor collector junction absorbs all remaining DC power: $P_{C(\text{quiescent})} = V_{CEQ} \cdot I_{CQ}$.
- Signal-Dependent Collector Power ($P_C(ac)$): When AC signal is present, AC power P_{ac} is delivered to load, REDUCING transistor heating: $P_C = P_{C(\text{quiescent})} - P_{ac}$.
- Worst-Case Thermal Condition: Maximum transistor heating occurs at ZERO AC INPUT SIGNAL ($v_{in} = 0$), where $P_C = V_{CEQ} \cdot I_{CQ}$.

Derivation of Max Efficiency for Series-Fed Class-A

- Power Conversion Efficiency Definition: Efficiency η measures the capability of an amplifier to convert DC supply power into useful AC signal power: $\eta = \frac{P_{ac}}{P_{dc}} \times 100\%$.
- Series-Fed Configuration: Load resistor is directly connected as the collector resistor ($R_C = R_L$, $R_{DC} = r_c = R_C$).
- DC Load Line Endpoints: Saturation $I_{C(\text{sat})} = \frac{V_{CC}}{R_C}$, Cutoff $V_{CE(\text{off})} = V_{CC}$.
- Optimum Q-Point for Max Swing: $V_{CEQ} = \frac{V_{CC}}{2}$ and $I_{CQ} = \frac{V_{CC}}{2R_C}$.
- Max AC Power Output: $P_{ac(\text{max})} = \frac{V_{CEQ} \cdot I_{CQ}}{2} = \frac{(V_{CC}/2)(V_{CC}/2R_C)}{2} = \frac{V_{CC}^2}{8R_C}$.
- Total DC Power Input: $P_{dc} = V_{CC} \cdot I_{CQ} = V_{CC} \cdot \frac{V_{CC}}{2R_C} = \frac{V_{CC}^2}{2R_C}$.
- Efficiency Derivation: $\eta_{\text{max}} = \frac{P_{ac(\text{max})}}{P_{dc}} = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} = \frac{2}{8} = 0.25 = 25\%$.

Transformer-Coupled Class-A Amplifier Load Line

- Topology Advantage: Replacing collector resistor R_C with a step-down transformer primary winding reduces DC collector resistance to near zero ($R_{DC} \approx 0\ \Omega$).
- DC Load Line Behavior: Since $R_{DC} \approx 0$, the DC load line is nearly VERTICAL at $V_{CEQ} \approx V_{CC}$.
- Reflected AC Load Resistance (r'_c): Impedance transformation by transformer turns ratio $n = N_1/N_2$: $r'_c = n^2 R_L = \left(\frac{N_1}{N_2}\right)^2 R_L$.
- AC Load Line Voltage Induction: Primary winding inductance allows collector voltage to swing UP TO TWICE V_{CC} ($v_{ce(\text{off})} \approx 2V_{CC}$) during negative current swings due to inductive kickback.
- Efficiency Derivation: Max AC swing $V_{ce(peak)} = V_{CC}$ and $I_{c(peak)} = I_{CQ}$. $P_{ac(\max)} = \frac{V_{CC} I_{CQ}}{2}$, $P_{dc} = V_{CC} I_{CQ}$. Efficiency $\eta_{\max} = \frac{V_{CC} I_{CQ}/2}{V_{CC} I_{CQ}} = 50\%$.

The Maximum Thermal Power Dissipation Hyperbola

- Transistor Rating Limits: Manufacturers specify maximum junction power rating $P_{D(\text{max})}$ at ambient temperature 25°C (e.g., 500 mW for 2N2222, 10 W for TIP31).
- Thermal Hyperbola Equation: Plotting $V_{CE} \cdot I_C = P_{D(\text{max})}$ on output characteristics yields a rectangular hyperbola curve.
- Safe Operating Area (SOA): The region under the hyperbola bounded by $V_{CE(\text{max})}$ breakdown voltage and $I_{C(\text{max})}$ saturation current.
- Q-Point Boundary Constraint: To prevent transistor destruction from overheating, the quiescent Q-point MUST lie strictly BELOW the $P_{D(\text{max})}$ hyperbola curve.
- Derating Factor: At higher operating temperatures ($T_A > 25°\text{C}$), $P_{D(\text{max})}$ must be derated linearly using thermal resistance θ_{JA}: $P_{D(\text{derated})} = \frac{T_{j(\text{max})} - T_A}{\theta_{JA}}$.

Dynamic Q-Point Shift Under Large Signal Overdrive

- Small-Signal Assumption: Linear AC analysis assumes small input amplitudes where operating point variations remain strictly linear along the static AC load line.
- Large-Signal Non-Linearity: BJT exponential transconductance $I_C = I_S e^{V_{BE}/V_T}$ causes positive half-cycles of collector current to expand more than negative half-cycles contract.
- DC Average Shift: Non-symmetrical current peaks create a net DC rectified current component ΔI_{DC}. Total average collector current becomes $I_{C(\text{avg})} = I_{CQ} + \Delta I_{DC}$.
- Dynamic Q-Point Migration: As input signal amplitude increases, the effective average Q-point shifts upward and rightward along the DC load line, altering bias conditions and increasing heat dissipation.

Worked Example: Power Dissipation & Efficiency Calculation

- Problem Statement: A Common-Emitter series-fed Class-A amplifier operates with $V_{CC} = 18$ V, collector resistor $R_C = 1.2$ kΩ, and Q-point set at $V_{CEQ} = 9$ V, $I_{CQ} = 7.5$ mA. 1. Calculate DC supply power P_{dc}. 2. Calculate maximum unclipped AC power output $P_{ac(\max)}$. 3. Calculate amplifier conversion efficiency η. 4. Calculate transistor collector dissipation under zero signal $P_{C(0)}$ and max signal $P_{C(\text{max signal})}$.
- Step 1 (DC Power Input): $P_{dc} = V_{CC} \cdot I_{CQ} = 18 \text{ V} \times 7.5 \text{ mA} = 135 \text{ mW}$.
- Step 2 (Max AC Power Output): $P_{ac(\max)} = \frac{V_{CEQ} \cdot I_{CQ}}{2} = \frac{9 \text{ V} \times 7.5 \text{ mA}}{2} = \frac{67.5}{2} = 33.75 \text{ mW}$.
- Step 3 (Conversion Efficiency): $\eta = \frac{P_{ac(\max)}}{P_{dc}} \times 100\% = \frac{33.75 \text{ mW}}{135 \text{ mW}} \times 100\% = 25.0\%$.
- Step 4 (Transistor Heat Dissipation): - Zero Signal:
  $P_{C(0)} = V_{CEQ} \cdot I_{CQ} = 9 \text{ V} \times 7.5 \text{ mA} = 67.5 \text{ mW}$. - Max Signal:
  $P_{C(\text{max signal})} = P_{C(0)} - P_{ac(\max)} = 67.5 \text{ mW} - 33.75 \text{ mW} = 33.75 \text{ mW}$.

Worked Example: Dynamic AC Load Line with External Load R_L

- Circuit Specification: $V_{CC} = 12$ V, $R_C = 2.2$ kΩ, $R_E = 680$ Ω, $R_L = 1.0$ kΩ, Q-point set at $I_{CQ} = 2.5$ mA, $V_{CEQ} = 4.8$ V.
- Step 1 (DC Resistance & DC Load Line Endpoints): $R_{DC} = R_C + R_E = 2.2\ \text{k}\Omega + 0.68\ \text{k}\Omega = 2.88\ \text{k}\Omega$. DC Cutoff: $V_{CE(\text{off})} = 12$ V; DC Saturation: $I_{C(\text{sat})} = \frac{12\ \text{V}}{2.88\ \text{k}\Omega} = 4.167$ mA.
- Step 2 (AC Load Resistance r_c): $r_c = R_C \parallel R_L = \frac{2.2 \times 1.0}{2.2 + 1.0}\ \text{k}\Omega = \frac{2.2}{3.2}\ \text{k}\Omega = 687.5\ \Omega$.
- Step 3 (AC Load Line Endpoints): AC Saturation Current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c} = 2.5\ \text{mA} + \frac{4.8\ \text{V}}{687.5\ \Omega} = 2.5\ \text{mA} + 6.982\ \text{mA} = 9.482$ mA. AC Cutoff Voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} r_c = 4.8\ \text{V} + (2.5\ \text{mA} \times 687.5\ \Omega) = 4.8\ \text{V} + 1.719\ \text{V} = 6.519$ V.
- Step 4 (Max AC Power Delivered to Load R_L): Max peak voltage across load: $V_p = \min(V_{CEQ} - V_{CE(\text{sat})}, I_{CQ} r_c) = \min(4.6\ \text{V}, 1.719\ \text{V}) = 1.719$ V. AC Power to R_L: $P_{L(\text{max})} = \frac{V_p^2}{2R_L} = \frac{(1.719)^2}{2 \times 1000} = \frac{2.955}{2000} = 1.478$ mW.

Symmetrical Swing Design Optimization Procedure

- Objective: Given supply voltage V_{CC} and AC load R_L, design R_C and R_E to achieve maximum symmetrical undistorted output voltage swing.
- Design Step 1: Choose emitter resistor drop $V_E \approx 0.1V_{CC}$ for DC thermal stability. Set $R_E = \frac{0.1V_{CC}}{I_{CQ}}$.
- Design Step 2: Set optimum V_{CEQ} condition: $V_{CEQ(\text{opt})} = \frac{V_{CC} \cdot r_c}{r_c + R_{DC}}$.
- Design Step 3: Solve for required collector resistor R_C such that $r_c = R_C \parallel R_L$ satisfies symmetrical swing $I_{CQ} r_c = V_{CEQ} - V_{CE(\text{sat})}$.
- Design Step 4: Verify that peak transistor dissipation $P_{C(0)} = V_{CEQ} I_{CQ}$ stays safely below $P_{D(\text{max})}$ thermal hyperbola with a 50% safety margin.

Summary Table: Power & Load Line Formulas

- Core Formula Summary: 1. DC Load Line: $I_C = -\frac{1}{R_C+R_E}V_{CE} + \frac{V_{CC}}{R_C+R_E}$ 2. AC Load Line: $i_C - I_{CQ} = -\frac{1}{r_c}(v_{CE} - V_{CEQ})$, where $r_c = R_C \parallel R_L$ 3. AC Saturation Current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c}$ 4. AC Cutoff Voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ}r_c$ 5. Max Sinusoidal AC Power: $P_{ac(\text{max})} = \frac{V_{ce(peak)}I_{c(peak)}}{2} = \frac{V_{o(p-p)}^2}{8r_c}$ 6. DC Input Power: $P_{dc} = V_{CC}I_{CQ}$ 7. Max Series-Fed Efficiency: $\eta_{\text{max}} = 25\%$ 8. Max Transformer-Coupled Efficiency: $\eta_{\text{max}} = 50\%$

Summary of Lecture 14 & Engineering Principles

- AC Power & Headroom: $P_{ac} = \frac{V_{ce(peak)} I_{c(peak)}}{2}$. AC swing is strictly bounded by load line intercepts $i_{C(\text{sat})}$ and $v_{ce(\text{off})}$.
- Class-A Efficiency Limits: Series-fed topology reaches a maximum of 25% efficiency; transformer coupling elevates efficiency to 50%.
- Worst-Case Thermal Loading: Transistors dissipate maximum heat at ZERO AC input signal ($P_C = V_{CEQ} I_{CQ}$).
- Safe Operating Area: Q-point must remain below the thermal hyperbola $V_{CE} I_C = P_{D(\text{max})}$ under all operating temperatures.
- Next Lecture Preview: Transition to detailed analysis of BJT Biasing Methods (Fixed Bias, Collector Feedback, Emitter Bias, Voltage Divider Bias).