Lecture 13: The Load Lines: D

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Plan: Load Line Fundamentals

- Concept and Purpose of Load Lines in Electronic Circuit Analysis
- DC Load Line: Mathematical Derivation, Slopes, and Boundary Coordinates
- AC Load Line: Concept of AC Load Resistance ($r_c = R_C \parallel R_L$)
- Mathematical Derivation of the AC Load Line Equation
- AC Load Line Endpoints: AC Saturation Current and AC Cutoff Voltage
- Comparative Analysis of DC vs AC Load Line Parameters
- Effect of Coupling/Bypass Capacitors on AC Load Line Slope
- Optimum Q-Point Placement for Maximum Symmetrical AC Swing
- Comprehensive Worked Numerical Example with Graph Plotting
- Summary & Key Takeaways

Overview and Fundamental Concept of Load Lines

- Graphical Interface: A load line is a straight line drawn on the transistor's output characteristic curves (I_C vs V_{CE}) that represents all possible combined operating states allowed by external circuit resistors and power supplies.
- Dual Nature of Amplifiers: An amplifier operates simultaneously under two operational modes: DC steady-state bias (zero input signal) and AC dynamic response (time-varying input signal).
- DC Load Line Function: Determines the static quiescent operating point (Q-point) under zero-signal conditions based solely on DC resistance paths.
- AC Load Line Function: Determines the trajectory along which instantaneous voltage $v_{CE}(t)$ and current $i_C(t)$ move when an AC input signal $v_{in}(t)$ is applied, based on AC load impedance.

D.C. Load Line: Derivation & Characteristics

- Circuit Model: Consider a Common-Emitter amplifier powered by V_{CC} with collector resistor R_C and emitter resistor R_E.
- Output KVL Equation: $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$.
- DC Resistance Definition: Defining total DC resistance $R_{DC} = R_C + R_E$ (since $I_E \approx I_C$), the KVL equation simplifies to: $V_{CE} = V_{CC} - I_C R_{DC}$.
- Linear Equation Form: $I_C = -\frac{1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}$.
- DC Slope & Intercepts: - Slope $m_{DC} = -\frac{1}{R_{DC}} = -\frac{1}{R_C + R_E}$. - Voltage Intercept (Cutoff): $V_{CE(\text{off})} = V_{CC}$ (when $I_C = 0$). - Current Intercept (Saturation): $I_{C(\text{sat})} = \frac{V_{CC}}{R_{DC}} = \frac{V_{CC}}{R_C + R_E}$ (when $V_{CE} = 0$).

A.C. Equivalent Resistance (r_c) Derivation

- Capacitors at Signal Frequencies: At operational AC frequencies ($f > 20$ Hz), coupling capacitors (C_1, C_2) and emitter bypass capacitors (C_E) have negligible reactance ($X_C \to 0\ \Omega$) and act as short circuits.
- DC Supply Behavior at AC: The DC voltage source V_{CC} has zero internal AC impedance and acts as an AC ground reference.
- Collector AC Path: Under AC conditions, collector resistor R_C is connected between collector and AC ground. External load resistor R_L is connected through coupling capacitor C_2 between collector and AC ground.
- Effective AC Load Resistance (r_c): R_C and R_L appear in parallel to AC signals: $r_c = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L}$.
- Emitter AC Path: Bypass capacitor C_E short-circuits R_E to ground ($r_e = 0\ \Omega$ for AC path in bypassed CE amplifier). Therefore, total AC load resistance seen by collector is r_c.

Derivation of the A.C. Load Line Equation

- AC Ohm's Law Relationship: Small-signal collector voltage variation $v_{ce}(t)$ and current variation $i_c(t)$ are related by the AC load resistance: $i_c = -\frac{v_{ce}}{r_c}$.
- Superposition of AC and DC Values: Instantaneous collector current $i_C(t) = I_{CQ} + i_c(t)$ and instantaneous collector-emitter voltage $v_{CE}(t) = V_{CEQ} + v_{ce}(t)$.
- Substituting Instantaneous Variations: $i_c(t) = i_C(t) - I_{CQ}$ and $v_{ce}(t) = v_{CE}(t) - V_{CEQ}$.
- AC Load Line Formula: Substituting variations into AC Ohm's law: $(i_C - I_{CQ}) = -\frac{1}{r_c}(v_{CE} - V_{CEQ})$.
- Standard Point-Slope Form: $i_C = -\frac{1}{r_c} v_{CE} + \left(I_{CQ} + \frac{V_{CEQ}}{r_c}\right)$.
- Constraint: The AC load line MUST pass directly through the quiescent Q-point coordinate (V_{CEQ}, I_{CQ}).

A.C. Load Line Intercepts & Boundary Coordinates

- AC Saturation Current Point ($v_{CE} = 0$ V): Setting instantaneous voltage $v_{CE} = 0$ in the AC load line equation yields the maximum peak AC collector saturation current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c}$.
- AC Cutoff Voltage Point ($i_C = 0$ mA): Setting instantaneous current $i_C = 0$ yields the maximum peak AC collector-emitter cutoff voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} \cdot r_c$.
- Graphical Construction: Connect Point A $(v_{ce(\text{off})}, 0) = (V_{CEQ} + I_{CQ} r_c,\ 0)$ on the voltage axis to Point B $(0, i_{C(\text{sat})}) = (0,\ I_{CQ} + \frac{V_{CEQ}}{r_c})$ on the current axis.
- Pivotal Property: The AC load line intersects the DC load line precisely at the Q-point (V_{CEQ}, I_{CQ}).
- Slope Steepness Comparison: Because $r_c = R_C \parallel R_L < R_{DC} = R_C + R_E$, the magnitude of the AC slope $|-1/r_c|$ is STEEPER than the DC slope $|-1/R_{DC}|$.

Comparative Table: D.C. Load Line vs. A.C. Load Line

- Parameter Comparison: 1. Governing Resistance: DC resistance $R_{DC} = R_C + R_E$ vs AC load resistance $r_c = R_C \parallel R_L$. 2. Slope: DC slope $m_{DC} = -\frac{1}{R_C+R_E}$ vs AC slope $m_{AC} = -\frac{1}{R_C \parallel R_L}$. 3. Line Equation: $I_C = -\frac{1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}$ vs $i_C - I_{CQ} = -\frac{1}{r_c}(v_{CE} - V_{CEQ})$. 4. Voltage Axis Intercept: $V_{CE(\text{off})} = V_{CC}$ vs $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} r_c$. 5. Current Axis Intercept: $I_{C(\text{sat})} = \frac{V_{CC}}{R_C+R_E}$ vs $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c}$. 6. Role in Circuit Design: Sets static DC Q-point vs determines max AC signal swing & output power.

Effect of Load Resistance R_L on AC Load Line Slope

- Unloaded Amplifier ($R_L = \infty$): If no external load is connected, $r_c = R_C \parallel \infty = R_C$. If emitter is bypassed (R_E shorted at AC), AC slope is -\{}frac{1}{R_C}, which is steeper than DC slope -\{}frac{1}{R_C + R_E}.
- Heavy AC Loading ($R_L \ll R_C$): Connecting a small load resistance R_L sharply reduces $r_c = \frac{R_C R_L}{R_C + R_L} \approx R_L$.
- Graphical Rotation: As R_L decreases, r_c decreases, causing the AC load line to rotate CLOCKWISE around the fixed Q-point (steeper slope).
- Impact on Signal Swing: Heavy loading (smaller r_c) dramatically reduces the cutoff voltage swing limit $v_{ce(\text{peak})} = I_{CQ} r_c$, causing early cutoff clipping at lower AC input signal levels.

Optimum Q-Point Location for Maximum AC Voltage Swing

- Equal Swing Headroom Condition: To achieve maximum symmetrical undistorted AC output swing, the AC saturation current headroom must equal the AC cutoff voltage headroom expressed in equivalent current.
- Mathematical Condition: \{}Delta V_{ce(\{}text{sat})} = \{}Delta V_{ce(\{}text{cutoff})} \{}implies V_{CEQ} - V_{CE(\{}text{sat})} = I_{CQ} \{}cdot r_c.
- Assuming $V_{CE(\text{sat})} \approx 0$ V: $V_{CEQ} = I_{CQ} \cdot r_c$.
- Derivation of Optimum V_{CEQ}: Substitute $I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_{DC}}$ into optimum condition:
  $V_{CEQ} = \left(\frac{V_{CC} - V_{CEQ}}{R_{DC}}\right) r_c \implies V_{CEQ}\left(1 + \frac{r_c}{R_{DC}}\right) = V_{CC}\frac{r_c}{R_{DC}}$.
- Optimum Q-Point Equation: $V_{CEQ(\text{opt})} = \frac{V_{CC}}{1 + \frac{R_{DC}}{r_c}} = \frac{V_{CC} \cdot r_c}{r_c + R_{DC}}$.
- Optimum Current Equation: $I_{CQ(\text{opt})} = \frac{V_{CC}}{r_c + R_{DC}}$.

Worked Example: DC and AC Load Line Calculation

- Circuit Specification: A CE amplifier has $V_{CC} = 15$ V, $R_C = 3.3$ kΩ, $R_E = 1.2$ kΩ, $R_L = 4.7$ kΩ, and Q-point coordinates $I_{CQ} = 2.0$ mA, $V_{CEQ} = 6.0$ V.
- Step 1 (DC Resistance & DC Load Line): $R_{DC} = R_C + R_E = 3.3\ \text{k}\Omega + 1.2\ \text{k}\Omega = 4.5\ \text{k}\Omega$. DC Cutoff Voltage: $V_{CE(\text{off})} = V_{CC} = 15$ V. DC Saturation Current: $I_{C(\text{sat})} = \frac{V_{CC}}{R_{DC}} = \frac{15\ \text{V}}{4.5\ \text{k}\Omega} = 3.33$ mA.
- Step 2 (AC Load Resistance r_c): $r_c = R_C \parallel R_L = \frac{3.3 \times 4.7}{3.3+4.7}\ \text{k}\Omega = \frac{15.51}{8.0}\ \text{k}\Omega = 1.939\ \text{k}\Omega$.
- Step 3 (AC Load Line Intercepts): AC Saturation Current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c} = 2.0\ \text{mA} + \frac{6.0\ \text{V}}{1.939\ \text{k}\Omega} = 2.0 + 3.094 = 5.094$ mA. AC Cutoff Voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} r_c = 6.0\ \text{V} + (2.0\ \text{mA} \times 1.939\ \text{k}\Omega) = 6.0 + 3.878 = 9.878$ V.

Worked Example: Max Swing & Clipping Determination

- Continuing from Slide 11: Q-point (6.0 V, 2.0 mA), $r_c = 1.939$ kΩ.
- Step 1 (Calculate Saturation-Limited Peak Voltage):
  $V_{ce(peak1)} = V_{CEQ} - V_{CE(\text{sat})} = 6.0\text{ V} - 0.2\text{ V} = 5.80\text{ V}$.
- Step 2 (Calculate Cutoff-Limited Peak Voltage):
  $V_{ce(peak2)} = I_{CQ} \cdot r_c = 2.0\text{ mA} \times 1.939\text{ k}\Omega = 3.878\text{ V}$.
- Step 3 (Determine Maximum Unclipped Output Swing):
  $V_{ce(peak)} = \min(5.80\text{ V}, 3.878\text{ V}) = 3.878\text{ V}$. $V_{o(p-p)\,\max} = 2 \times 3.878\text{ V} = 7.756\text{ V}$.
- Step 4 (Clipping Analysis): Since $V_{ce(peak2)}(3.878\text{ V}) < V_{ce(peak1)}(5.80\text{ V})$, the amplifier will experience CUTOFF CLIPPING first if overdriven beyond 7.76 V_{p-p}.

Graphical Plotting Guidelines for Load Lines

- Step 1: Plot transistor output characteristic curves (I_C vs V_{CE}) for various base currents I_B.
- Step 2: Plot the DC Load Line using endpoints $(V_{CC}, 0)$ and $(0, \frac{V_{CC}}{R_{DC}})$. Draw a straight line between them.
- Step 3: Mark the Q-point at the intersection of the DC Load Line and the operating base current curve $I_B = I_{BQ}$.
- Step 4: Compute AC load resistance $r_c = R_C \parallel R_L$ and find AC endpoints $(V_{CEQ} + I_{CQ} r_c,\ 0)$ and $(0,\ I_{CQ} + \frac{V_{CEQ}}{r_c})$.
- Step 5: Draw the AC Load Line passing through both AC endpoints and verify that it pivots directly through the Q-point.
- Step 6: Draw input AC signal waveform $i_b(t)$ on base axis and project output AC signals $i_c(t)$ and $v_{ce}(t)$ along the AC Load Line.

Summary of Lecture 13 & Load Line Principles

- Dual Load Line Concept: DC load line determines static Q-point; AC load line dictates dynamic AC signal variations.
- Slope Differences: DC slope $m_{DC} = -1/(R_C + R_E)$ vs AC slope $m_{AC} = -1/(R_C \parallel R_L)$. AC slope is always steeper due to $r_c < R_{DC}$.
- AC Intercepts: Saturation $i_{C(\text{sat})} = I_{CQ} + V_{CEQ}/r_c$; Cutoff $v_{ce(\text{off})} = V_{CEQ} + I_{CQ}r_c$.
- Optimum Q-Point: Maximum symmetrical AC swing occurs when $V_{CEQ(\text{opt})} = \frac{V_{CC}r_c}{r_c + R_{DC}}$.
- Engineering Application: Crucial tool for designing high-efficiency power amplifiers and preventing waveform clipping.