Lecture 12: Biasing of Amplifier and Definition of Operating Point

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Agenda: Q-Point Dynamics & Stability Analysis

- Maximum Undistorted Peak-to-Peak Signal Swing ($V_{o(p-p)}$)
- Graphical Analysis of Saturation Clipping vs. Cutoff Clipping
- Non-linear Signal Distortion and Harmonic Generation
- Derivation of Stability Factor $S = \frac{\partial I_C}{\partial I_{CBO}}$
- Stability Factors S' ($\partial I_C / \partial V_{BE}$) and S'' ($\partial I_C / \partial \beta$)
- Emitter Degeneration Resistor R_E and Negative Bias Feedback
- Comparative Evaluation of Biasing Networks against Thermal Drift
- Comprehensive Step-by-Step Numerical Stability Analysis
- Summary & Practical Circuit Design Rules

Maximum Undistorted Signal Swing Mechanics

- Dynamic AC Swing Concept: When an AC signal $v_{in}(t)$ is applied, collector current $i_C(t) = I_{CQ} + i_c(t)$ and collector-emitter voltage $v_{CE}(t) = V_{CEQ} + v_{ce}(t)$ oscillate along the load line around the quiescent Q-point.
- Saturation Limit (Positive Collector Current Peak): As i_c increases, v_{CE} decreases toward saturation $V_{CE(\text{sat})}$. The maximum positive swing in collector current before saturation clipping is: \{}Delta I_{C(\{}text{sat})} = I_{C(\{}text{sat})} - I_{CQ} = \{}frac{V_{CEQ} - V_{CE(\{}text{sat})}}{r_c}.
- Cutoff Limit (Negative Collector Current Peak): As i_c decreases toward zero ($i_C = 0$), v_{CE} increases toward cutoff $v_{ce(\text{off})}$. The maximum negative swing in collector current before cutoff clipping is: \{}Delta I_{C(\{}text{off})} = I_{CQ}.
- Symmetrical Swing Condition: To prevent asymmetric clipping, the maximum unclipped peak AC collector current is: $I_{c(\text{peak})} = \min\left(I_{CQ}, \frac{V_{CEQ} - V_{CE(\text{sat})}}{r_c}\right)$.

Mathematical Derivation of Maximum Peak-to-Peak Voltage Swing

- AC Output Voltage Swing Definition: The AC output voltage swing across collector AC load resistance $r_c = R_C \parallel R_L$ is given by $v_{ce(p-p)} = 2 \cdot V_{ce(peak)}$.
- Voltage Swing Bound 1 (Saturation Limited): $V_{ce(peak1)} = V_{CEQ} - V_{CE(\text{sat})} \approx V_{CEQ}$ (assuming $V_{CE(\text{sat})} \approx 0$ V).
- Voltage Swing Bound 2 (Cutoff Limited): $V_{ce(peak2)} = I_{CQ} \cdot r_c$.
- Unclipped Voltage Swing Equation: $V_{o(p-p)\,\max} = 2 \cdot \min\left(V_{CEQ} - V_{CE(\text{sat})},\ I_{CQ} \cdot r_c\right)$.
- Optimum Q-Point for Maximum Swing: Setting $V_{CEQ} - V_{CE(\text{sat})} = I_{CQ} r_c$ yields identical clipping boundaries on both positive and negative peaks, achieving maximum possible output power efficiency.

Waveform Distortion: Saturation vs. Cutoff Clipping

- Saturation Clipping Characteristics: Occurs when input signal amplitude pushes V_{CE} below $V_{CE(\text{sat})} \approx 0.2$ V. The output voltage waveform flattens out at the bottom peak (or top peak depending on phase inversion), introducing heavy odd-harmonic frequency components.
- Cutoff Clipping Characteristics: Occurs when base-emitter junction becomes reverse-biased during input troughs ($i_B \leq 0$). Collector current drops to zero, flattening the opposite peak of the AC output voltage waveform.
- Non-Linear Transfer Characteristic: BJT exponential collector current equation $I_C = I_S e^{V_{BE}/V_T}$ causes harmonic generation even prior to sharp clipping when signal amplitude exceeds thermal voltage $V_T \approx 26$ mV.
- Total Harmonic Distortion (THD): Defined as $\text{THD} = \frac{\sqrt{V_2^2+V_3^2+V_4^2+\cdots}}{V_1} \times 100\%$. Severe clipping elevates THD beyond 10%, rendering the amplifier unusable for high-fidelity audio.

Introduction to Thermal Stability Factor S

- Definition of Stability Factor S: The stability factor S measures the rate of change of collector current I_C with respect to reverse saturation leakage current I_{CBO}, holding V_{BE} and β constant: $S = \frac{\partial I_C}{\partial I_{CBO}}$.
- Ideal vs. Worst-Case Values: Lower S signifies superior thermal stability. Ideal stability factor is $S = 1$ (where change in I_C equals change in I_{CBO}). Poor stability circuits exhibit $S = 1 + \beta \approx 100$ to 300.
- General Derivative Formula Derivation: Starting with collector current relation $I_C = \beta I_B + (1 + \beta) I_{CBO}$. Differentiating both sides with respect to I_C: $1 = \beta \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial I_{CBO}}{\partial I_C}$.
- General Stability Equation: Rearranging terms yields: $S = \frac{\partial I_C}{\partial I_{CBO}} = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$.

Secondary Stability Factors S' and S''

- Stability Factor S' (V_{BE} Sensitivity): Measures change in I_C relative to base-emitter voltage drop V_{BE}, holding I_{CBO} and β constant: $S' = \frac{\partial I_C}{\partial V_{BE}}$.
- Mathematical Formulation for S': For circuit with feedback resistance, $S' = \frac{-\beta}{R_{Th}+(1+\beta)R_E}$. Since V_{BE} decreases by -2.5 mV/$^\circ$C, collector current shift is $\Delta I_C = S' \cdot \Delta V_{BE}$.
- Stability Factor S'' (β Sensitivity): Measures change in I_C relative to transistor current gain β, holding I_{CBO} and V_{BE} constant: $S'' = \frac{\partial I_C}{\partial \beta}$.
- Mathematical Formulation for S'': Differentiating I_C with respect to β yields $S'' = \frac{I_{C1}}{\beta_1(1+\beta_2)} \cdot S_2$, where S_2 is the stability factor of the target state.
- Total Collector Current Drift: Total drift combining all three thermal effects is: $\Delta I_C = S \cdot \Delta I_{CBO} + S' \cdot \Delta V_{BE} + S'' \cdot \Delta\beta$.

Emitter Degeneration Resistor R_E & Negative Bias Feedback

- Role of Emitter Resistor R_E: Introducing an emitter resistor R_E between transistor emitter and ground creates automatic negative voltage feedback that stabilizes the Q-point against thermal changes.
- Self-Stabilization Feedback Mechanism: 1. Temperature increases $\rightarrow I_C$ attempts to increase. 2. Emitter voltage $V_E = I_E R_E \approx I_C R_E$ increases. 3. Base-emitter junction voltage $V_{BE} = V_B - V_E$ decreases. 4. Decreased V_{BE} reduces base current I_B, opposing the initial rise in I_C.
- Quantitative Stabilization Requirement: Effective stabilization occurs when the voltage drop across emitter resistor $V_E = I_E R_E$ is much larger than thermal variations in V_{BE} ($V_E \approx 1$ V to 2 V, or $0.1V_{CC}$ to $0.2V_{CC}$).
- AC Bypass Capacitor C_E: To prevent R_E from reducing AC voltage gain (A_v), a large bypass capacitor C_E is connected in parallel with R_E, shorting AC signals to ground while retaining DC feedback.

Evaluation of Stability Factor S in Fixed Bias

- Circuit Base Current Equation: $I_B = \frac{V_{CC} - V_{BE}}{R_B}$.
- Derivative $\frac{\partial I_B}{\partial I_C}$: Since I_B depends only on constant parameters V_{CC}, V_{BE}, R_B, base current is completely independent of I_C: $\frac{\partial I_B}{\partial I_C} = 0$.
- Substitution into General Stability Formula: $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}} = \frac{1+\beta}{1-0} = 1 + \beta$.
- Numerical Impact: For a typical transistor with $\beta = 100$, $S = 101$. Any increase in leakage current ΔI_{CBO} is amplified by 101 times in collector current!
- Conclusion: Fixed bias offers zero feedback stabilization ($\frac{\partial I_B}{\partial I_C} = 0$), resulting in the worst possible stability factor $S = 1 + \beta$.

Evaluation of Stability Factor S in Collector-to-Base Bias

- Circuit Configuration: Base resistor R_B is tied between collector terminal and base terminal.
- Input Loop Equation: $V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0 \implies I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$.
- Derivative Calculation: Differentiating I_B with respect to I_C: $\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B + R_C}$.
- Substitution into Stability Equation: $S = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_B+R_C}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}$.
- Stability Improvement Analysis: Because the denominator is $(1 + \text{positive term}) > 1$, S is significantly smaller than $1 + \beta$. If $\beta R_C \gg (R_B + R_C)$, $S \approx 1 + \frac{R_B}{R_C}$.

Worked Example: Calculating S and S' for Voltage Divider Bias

- Circuit Parameters: Silicon transistor with $\beta = 100$, $V_{CC} = 15$ V, $R_1 = 33$ kΩ, $R_2 = 10$ kΩ, $R_C = 2.7$ kΩ, $R_E = 1$ kΩ.
- Step 1 (Thevenin Equivalent): $V_{Th} = V_{CC}\frac{R_2}{R_1+R_2} = 15\text{ V} \times \frac{10\text{ k}\Omega}{43\text{ k}\Omega} = 3.488$ V.
  $R_{Th} = R_1 \parallel R_2 = \frac{33\times 10}{43}\ \text{k}\Omega = 7.674\ \text{k}\Omega$.
- Step 2 (Derivative $\frac{\partial I_B}{\partial I_C}$): Base loop KVL: $V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$. Since $I_E = I_B + I_C$, $I_B = \frac{V_{Th}-V_{BE}-I_C R_E}{R_{Th}+R_E}$. Differentiating wrt I_C: $\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_{Th}+R_E}$.
- Step 3 (Calculate Stability Factor S):
  $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_{Th}+R_E}\right)} = \frac{101}{1+100\left(\frac{1\text{ k}\Omega}{7.674\text{ k}\Omega+1\text{ k}\Omega}\right)} = \frac{101}{1+100\left(\frac{1}{8.674}\right)} = \frac{101}{1+11.529} = \frac{101}{12.529} = 8.06.$
- Step 4 (Calculate Stability Factor S'):
  $S' = \frac{-\beta}{R_{Th}+(1+\beta)R_E} = \frac{-100}{7.674\text{ k}\Omega+101\times 1\text{ k}\Omega} = \frac{-100}{108.674\text{ k}\Omega} = -0.920$ mA/V.

Worked Example: Collector Current Shift under Temperature Rise

- Problem Statement: Using the Voltage Divider Bias circuit from Slide 11 ($S = 8.06, S' = -0.92$ mA/V), calculate the change in collector current ΔI_C when ambient temperature rises from 25°C to 75°C ($\Delta T = 50°C$). Given at 25°C: $I_{CBO} = 0.2\ \mu$A, $V_{BE} = 0.7$ V. At 75°C: I_{CBO} doubles every 10°C, $\frac{dV_{BE}}{dT} = -2.5$ mV/°C.
- Step 1 (ΔI_{CBO} Calculation): $\Delta T = 50°C \implies$ 5 doublings ($2^{50/10} = 32$). $I_{CBO}(75°C) = 0.2\ \mu\text{A} \times 2^5 = 0.2 \times 32 = 6.4\ \mu$A. $\Delta I_{CBO} = 6.4\ \mu\text{A} - 0.2\ \mu\text{A} = 6.2\ \mu$A.
- Step 2 (ΔV_{BE} Calculation): $\Delta V_{BE} = (-2.5\ \text{mV}/°\text{C}) \times 50°\text{C} = -125$ mV $= -0.125$ V.
- Step 3 (Drift due to I_{CBO}): $\Delta I_{C1} = S \cdot \Delta I_{CBO} = 8.06 \times 6.2\ \mu\text{A} = 49.97\ \mu\text{A} \approx 0.050$ mA.
- Step 4 (Drift due to V_{BE}): $\Delta I_{C2} = S' \cdot \Delta V_{BE} = (-0.920\ \text{mA/V}) \times (-0.125\ \text{V}) = +0.115$ mA.
- Step 5 (Total Shift ΔI_C): $\Delta I_C = \Delta I_{C1} + \Delta I_{C2} = 0.050\ \text{mA} + 0.115\ \text{mA} = +0.165$ mA.

Comparative Analysis of Biasing Stability Factors

- Fixed Bias: Stability Factor $S = 1 + \beta$. No feedback loop ($\partial I_B / \partial I_C = 0$). Poor stability; unusable in precision circuits.
- Collector-to-Base Feedback Bias: Stability Factor $S = \frac{1+\beta}{1+\beta \frac{R_C}{R_B + R_C}}$. Negative voltage feedback improves S moderately ($S \approx 10$ to 30).
- Voltage Divider Bias (Self-Bias): Stability Factor $S = \frac{1+\beta}{1+\beta \frac{R_E}{R_{Th} + R_E}} \approx 1 + \frac{R_{Th}}{R_E}$ (when $\beta R_E \gg R_{Th}$). Best overall stability ($S < 10$ easily achievable).
- Design Criterion for Minimal Drift: Select $R_{Th} \leq 0.1 \beta R_E$. Under this condition, $S \approx 1 + \frac{0.1 \beta R_E}{R_E} \approx 1 + 0.1\beta$, ensuring complete independence from transistor β variations.

Summary of Lecture 12 & Advanced Q-Point Rules

- Max Undistorted Swing: Bounded by $V_{o(p-p)\,\max} = 2 \cdot \min(V_{CEQ} - V_{CE(\text{sat})}, I_{CQ} r_c)$. Symmetrical headroom requires $V_{CEQ} = I_{CQ} r_c$.
- Harmonic Clipping: Saturation clips positive collector current peaks; cutoff clips negative peaks, producing high Total Harmonic Distortion (THD).
- Stability Factor S: Quantifies sensitivity to leakage current: $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$. Target low values ($S \to 1$).
- Role of Negative Feedback: Emitter resistor R_E introduces negative current feedback to oppose thermal drift in I_C.
- Optimal Topology: Voltage Divider Bias provides the most predictable Q-point stability when designed with $R_{Th} \ll \beta R_E$.