Lecture 11: Biasing of Amplifier and Definition of Operating Point

Transistor Biasing circuits And Thermal stability

DI02011011: Electronics Circuit and Application (ECA)

Lecture Plan & Topics Outline

- Need for DC Biasing in Transistor Amplifiers & Concept of Quiescent State
- Definition and Graphical Representation of Operating Point (Q-Point)
- Regions of BJT Operation: Cutoff, Active, and Saturation Limits
- DC Load Line Equation and Determination of Boundary Conditions
- DC Equivalent Circuit Derivation: Capacitive Open-Circuit Analysis
- Basic Fixed-Bias Circuit: Mathematical Analysis and Limitations
- Thermal Stability Factors & Parameters Affecting Q-Point Drift (β, V_{BE}, I_{CBO})
- Worked Numerical Problem: Calculating I_{CQ}, V_{CEQ}, and Power Dissipation
- Summary of Core Biasing Concepts and Q-Point Criteria

Need for DC Biasing in Transistor Amplifiers

- Superposition of AC Signal on DC Bias: BJT is a non-linear active device; to achieve linear operation for small-signal amplification, an external DC bias voltage V_{CC} must set a steady DC operating voltage and current before applying the AC input signal $v_{in}(t)$.
- Conduction Control in Base-Emitter Junction: The base-emitter PN junction requires a forward-bias voltage ($V_{BE} \approx 0.7$ V for Silicon, 0.3 V for Germanium) to maintain forward current conduction $I_B > 0$ throughout the entire 360-degree cycle of the AC input.
- Prevention of Distortion and Cutoff: Without proper DC bias, negative half-cycles of an AC input signal would drive $V_{BE} < 0.7$ V, turning the transistor OFF and causing extreme output distortion (cutoff clipping).
- Energy Conversion Function: Amplifiers do not create energy; they convert DC electrical power supplied by the bias source V_{CC} into AC signal power delivered to the load resistor R_L under the control of the input signal.

Definition of the Operating Point (Q-Point)

- Quiescent State Definition: The Operating Point, commonly called the Quiescent Point or Q-point, is the set of DC current and voltage values (V_{CEQ}, I_{CQ}) that exist in the transistor circuit in the complete absence of any AC input signal ($v_{in} = 0$ V).
- DC Coordinate Pair: For a Common-Emitter (CE) BJT amplifier, the Q-point is uniquely specified by two parameters: the DC collector current I_{CQ} (in mA) and the DC collector-emitter voltage V_{CEQ} (in Volts).
- Input Characteristic Dependency: Base current at the Q-point is governed by $I_{BQ} = \frac{V_{CC} - V_{BEQ}}{R_B}$, establishing the specific output characteristic curve $I_C = f(V_{CE})|_{I_B = I_{BQ}}$.
- Graphical Location: Geometrically, the Q-point is the exact point of intersection between the DC Load Line equation and the transistor's static collector characteristic curve corresponding to $I_B = I_{BQ}$.

BJT Regions of Operation & Q-Point Boundaries

- Active Region (Linear Amplifier Mode): Base-Emitter junction is forward biased ($V_{BE} \approx 0.7$ V), Collector-Base junction is reverse biased ($V_{CB} > 0$ V). Collector current is proportional to base current: $I_{CQ} = \beta_{DC} I_{BQ}$. This is the required region for low-distortion linear amplification.
- Saturation Region (Switch ON Mode): Base-Emitter and Collector-Base junctions are both forward biased ($V_{BE} \approx 0.8$ V, $V_{BC} > 0$ V). Collector-emitter voltage collapses to saturation level $V_{CE(\text{sat})} \approx 0.2$ V, and $I_C < \beta I_B$ (current limited by external collector resistor R_C).
- Cutoff Region (Switch OFF Mode): Base-Emitter junction is zero or reverse biased ($V_{BE} \leq 0$ V). Base current $I_B = 0$, collector current falls to leakage current $I_{CQ} = I_{CEO} \approx 0$ A, and $V_{CEQ} = V_{CC}$.
- Boundary Criteria for Undistorted Swing: To maximize symmetric AC voltage swing without hitting Saturation ($V_{CE(\text{sat})}$) or Cutoff (V_{CC}), the Q-point must be located precisely at the midpoint of the active region: $V_{CEQ} \approx \frac{V_{CC}}{2}$.

Derivation of the DC Load Line Equation

- DC Circuit Reduction: Apply Kirchhoff's Voltage Law (KVL) to the output collector-emitter loop of a common-emitter amplifier operating under pure DC bias.
- Loop Equation: Starting from V_{CC} through collector resistor R_C, transistor collector-emitter junction V_{CE}, and emitter resistor R_E to ground: $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$.
- Current Approximation: Since $I_E = I_C + I_B \approx I_C$ (for $\beta \gg 1$), simplify the KVL loop to: $V_{CC} - I_C(R_C + R_E) - V_{CE} = 0$.
- Standard Line Form ($y = mx + c$): Expressing I_C as a function of V_{CE}: $I_C = -\frac{1}{R_C+R_E} V_{CE} + \frac{V_{CC}}{R_C+R_E}$.
- Physical Slope Interpretation: The slope of the DC Load Line is given by $m = -\frac{1}{R_{DC}} = -\frac{1}{R_C+R_E}$, determined entirely by external circuit resistors and independent of transistor parameters.

DC Load Line Endpoints & Graphical Construction

- Cutoff Endpoint ($I_C = 0$ mA): Set collector current to zero in the DC load line equation. The collector-emitter voltage reaches its maximum value equal to the supply voltage: $V_{CE(\text{off})} = V_{CC}$. Point A on graph: $(V_{CC}, 0)$.
- Saturation Endpoint ($V_{CE} = 0$ V): Assuming ideal zero saturation voltage $V_{CE} = 0$ V, the collector current reaches its theoretical maximum saturation limit: $I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E}$. Point B on graph: $(0, \frac{V_{CC}}{R_C + R_E})$.
- Constructing the Line: Connecting Point A $(V_{CC}, 0)$ on the horizontal voltage axis to Point B $(0, I_{C(\text{sat})})$ on the vertical current axis yields the DC Load Line.
- Q-Point Intersection: Substituting base bias current $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$ yields $I_{CQ} = \beta I_{BQ}$. The Q-point is the intersection of the line with the static curve $I_B = I_{BQ}$, giving coordinates (V_{CEQ}, I_{CQ}) where $V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$.

DC Equivalent Circuit Analysis Procedure

- Capacitor Behavior at DC ($f = 0$ Hz): The capacitive reactance is $X_C = \frac{1}{2\pi fC} \to \infty\ \Omega$. All input coupling ($C_{in}$), output coupling ($C_{out}$), and emitter bypass ($C_E$) capacitors act as complete OPEN CIRCUITS.
- Isolation of DC Biasing Network: Removing open-circuited capacitors isolates the DC bias circuit from AC input signal sources and external load resistance R_L.
- AC Source Deactivation: All independent AC voltage sources $v_{in}(t)$ are set to zero (replaced by short circuits to ground).
- DC Circuit Analysis Steps: 1. Calculate base current I_{BQ} from input loop KVL. 2. Calculate collector current $I_{CQ} = \beta_{DC} I_{BQ}$. 3. Calculate collector voltage $V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E$. 4. Verify that $V_{CEQ} > V_{CE(\text{sat})} \approx 0.2$ V to confirm active region operation.

Basic Fixed-Bias Circuit & Mathematical Formulations

- Circuit Configuration: A single base resistor R_B is connected directly between the supply voltage V_{CC} and the transistor base terminal. Collector resistor R_C is connected from V_{CC} to collector. Emitter is tied directly to ground ($R_E = 0$).
- Input Loop Analysis (Base-Emitter Loop): Applying KVL:
  $V_{CC} - I_B R_B - V_{BE} = 0 \implies I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$.
- Output Loop Analysis (Collector-Emitter Loop): Applying KVL:
  $V_{CC} - I_C R_C - V_{CE} = 0 \implies V_{CEQ} = V_{CC} - I_{CQ} R_C$, where $I_{CQ} = \beta_{DC} I_{BQ}$.
- Major Drawback & Instability: Base current I_{BQ} is constant for a given R_B, but collector current $I_{CQ} = \beta \cdot I_{BQ}$ depends heavily on β_{DC}. Since β_{DC} varies widely (e.g., 50 to 300 due to manufacturing spread and temperature), the Q-point is extremely unstable.

Factors Influencing Q-Point Instability & Thermal Drift

- Transistor Parameter Sensitivity: The operating point (V_{CEQ}, I_{CQ}) drifts significantly due to temperature variations and component replacement.
- Temperature Variation of Reverse Saturation Current (I_{CBO}): Reverse leakage current doubles approximately every 10°C rise in temperature: $I_{CBO}(T_2) = I_{CBO}(T_1) \cdot 2^{\frac{T_2 - T_1}{10}}$. Rise in I_{CBO} directly increases total $I_C = \beta I_B + (1 + \beta) I_{CBO}$.
- Temperature Variation of Base-Emitter Voltage (V_{BE}): V_{BE} decreases linearly with temperature at a rate of $\frac{dV_{BE}}{dT} \approx -2.5$ mV/°C (or -2.3 mV/°C). As T increases, V_{BE} drops, causing base current I_B and collector current I_C to increase.
- Temperature Sensitivity of Current Gain (β_{DC}): Beta increases with temperature at approximately $+0.5\%$ to $+1\%$ per °C, further amplifying the drift of I_{CQ}.

Thermal Runaway Mechanism in BJT Circuits

- Definition: Thermal Runaway is a destructive self-reinforcing positive feedback loop where increased junction temperature causes collector current to rise, which increases power dissipation, leading to further temperature rise until transistor destruction.
- Positive Feedback Chain: $\uparrow T_j \longrightarrow \uparrow I_{CBO}$ & $\uparrow \beta$ & $\downarrow V_{BE} \longrightarrow \uparrow I_C \longrightarrow \uparrow P_D(V_{CE}I_C) \longrightarrow \uparrow T_j$.
- Power Dissipation Formula: Collector junction power dissipation is $P_D = V_{CE}I_C + V_{BE}I_B \approx V_{CE}I_C$. Heat generated elevates junction temperature $T_j = T_A + \theta_{JA}P_D$, where θ_{JA} is thermal resistance (°C/W).
- Thermal Stability Condition: To prevent thermal runaway, the rate of increase of heat dissipation capability must exceed the rate of increase of heat generation: $\frac{\partial P_D}{\partial T_j} < \frac{1}{\theta_{JA}}$.
- Mitigation Strategy: Incorporating an emitter resistor R_E provides negative feedback to stabilize I_C against thermal drift.

Worked Example: Q-Point Calculation for Fixed-Bias Circuit

- Problem Statement: For a fixed-bias common-emitter amplifier circuit with $V_{CC} = 12$ V, base resistor $R_B = 240$ kΩ, collector resistor $R_C = 2.2$ kΩ, and silicon transistor with $\beta = 100$ ($V_{BE} = 0.7$ V): 1. Calculate quiescent base current I_{BQ} and collector current I_{CQ}. 2. Calculate quiescent collector-emitter voltage V_{CEQ}. 3. Determine saturation collector current $I_{C(\text{sat})}$. 4. Calculate total DC power dissipated by the transistor.
- Step 1 (Base Current): $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240 \times 10^3\ \Omega} = \frac{11.3\text{ V}}{240\text{ k}\Omega} = 47.08\ \mu\text{A}$.
- Step 2 (Collector Current): $I_{CQ} = \beta \cdot I_{BQ} = 100 \times 47.08\ \mu\text{A} = 4.708$ mA.
- Step 3 (Collector-Emitter Voltage): $V_{CEQ} = V_{CC} - I_{CQ}R_C = 12\text{ V} - (4.708\text{ mA} \times 2.2\text{ k}\Omega) = 12\text{ V} - 10.358\text{ V} = 1.642$ V.
- Step 4 (Saturation & Power): $I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = 5.455$ mA. Transistor power $P_D = V_{CEQ} \cdot I_{CQ} = 1.642\text{ V} \times 4.708\text{ mA} = 7.73$ mW.

Worked Example: Evaluating β Sensitivity in Fixed Bias

- Problem Statement: Using the same circuit parameters ($V_{CC} = 12$ V, $R_B = 240$ kΩ, $R_C = 2.2$ kΩ), evaluate the shift in Q-point if the transistor is replaced with one having $\beta = 150$ (50% increase).
- Base Current Calculation: $I_{BQ} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = 47.08\ \mu$A (remains completely unchanged by transistor replacement).
- New Collector Current: $I_{CQ(\text{new})} = \beta_{\text{new}} \cdot I_{BQ} = 150 \times 47.08\ \mu\text{A} = 7.062$ mA.
- Attempted V_{CEQ} Calculation: $V_{CEQ} = V_{CC} - I_{CQ(\text{new})} R_C = 12\text{ V} - (7.062\text{ mA} \times 2.2\text{ k}\Omega) = 12\text{ V} - 15.536\text{ V} = -3.536$ V.
- Physical Analysis & Saturation Verification: Since calculated $V_{CEQ} < 0$ V (impossible in passive circuits), the transistor has been driven completely into SATURATION! Actual $V_{CE(\text{sat})} \approx 0.2$ V, and actual $I_{C(\text{sat})} = \frac{12 - 0.2}{2.2\text{ k}\Omega} = 5.36$ mA.
- Engineering Conclusion: Fixed bias fails to maintain active region operation under normal β parameter variations, proving the imperative need for stabilized biasing schemes like Voltage Divider Bias.

Summary of Lecture 11 & Key Engineering Insights

- Purpose of Biasing: DC biasing establishes quiescent conditions (V_{CEQ}, I_{CQ}) to ensure linear, unclipped small-signal amplification.
- DC Load Line Mechanics: Defined by $I_C = -\frac{1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}$, connecting $(V_{CC}, 0)$ to $(0, \frac{V_{CC}}{R_{DC}})$. It depends exclusively on passive supply and resistor values.
- Optimal Q-Point Selection: Center of the active region ($V_{CEQ} \approx V_{CC}/2$) offers maximum symmetrical peak-to-peak signal swing.
- Thermal Sensitivity Factors: Junction temperature rise elevates I_{CBO} and β while reducing V_{BE}, threatening thermal runaway.
- Fixed Bias Limitation: Unacceptable Q-point instability due to direct β-dependence, necessitating emitter degeneration feedback circuits.