Lecture 10: List application of FETs

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: Industrial & Circuit Applications of FETs

- Application 1: Voltage Variable Resistors (VVR) in the Ohmic Region.
- Application 2: Analog Switches, Multiplexers, and CMOS Transmission Gates.
- Application 3: High Input Impedance Buffers & Source Followers.
- Application 4: Active Loads & Constant Current Sources in Integrated Circuits.
- Application 5: CMOS Digital Logic Gate Design & Power Dissipation.
- Application 6: Power MOSFETs in SMPS, Buck Converters, and H-Bridges.
- Application 7: RF / Microwave Low-Noise Amplifiers & AGC Systems.
- Quantitative Application Examples, Selection Guidelines, and Future Trends.

FET as a Voltage Variable Resistor (VVR)

- Operating Region Requirement: Operated strictly in the Deep Triode / Linear region where drain-source voltage is kept very small ($V_{DS} \ll V_{GS} - V_{Th}$).
- Resistance Formula (JFET / D-MOSFET): Channel resistance varies inversely with gate voltage: $r_{DS} = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)} = \frac{|V_P|}{2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)}$.
- Resistance Formula (E-MOSFET): $r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Th})} = \frac{1}{K_n(V_{GS} - V_{Th})}$.
- AC Distortion Reduction: Small AC signals ($\Delta v_{ds} < 100$ mV) prevent non-linear harmonic distortion; feedback resistors from drain to gate cancel second-harmonic distortion.
- Practical Uses: Automatic Gain Control (AGC) attenuators, voltage-controlled filters (VCF), volume control stages, and electronic equalizers.

FET as an Analog Switch & CMOS Transmission Gate

- Single-FET Analog Switch: An E-MOSFET acts as an ON/OFF switch for analog signals. When $V_{GS} > V_{Th}$, switch is ON ($R_{ON} \approx 10 - 100\,\Omega$); when $V_{GS} < V_{Th}$, switch is OFF ($R_{OFF} > 10^9\,\Omega$).
- Signal Amplitude Limitation: A single NMOS switch suffers from signal distortion when analog input voltage v_{in} approaches $V_{DD} - V_{Th}$, increasing R_{ON} drastically.
- CMOS Transmission Gate (TG): Connects an NMOS and a PMOS transistor in parallel, driven by complementary control signals (C and $\bar{C}$).
- Complementary Resistance Compensation: As v_{in} rises, NMOS R_{ON} increases while PMOS R_{ON} decreases, maintaining a nearly constant total switch resistance ($R_{TG} \approx$ const) across full signal rail 0V to V_{DD}.
- Applications: Sample-and-Hold (S/H) circuits for ADCs, switched-capacitor filters, analog multiplexers (MUX), and crossbar matrix switches.

Source Follower (Common Drain) Buffer Amplifier

- Circuit Topology: Input signal applied to Gate; output taken from Source across resistor R_S; Drain connected to DC supply V_{DD}.
- Near-Unity Voltage Gain: $A_v = \frac{v_o}{v_i} = \frac{g_m R_S}{1+g_m R_S} \approx 1$ (typically 0.95 to 0.99).
- Ultra-High Input Resistance: $R_{in} = R_G \approx 10^7\,\Omega$ to $10^{12}\,\Omega$ (can be bootstrapped to $> 10^{14}\,\Omega$).
- Low Output Resistance: $R_{out} = R_S \parallel \frac{1}{g_m} \approx \frac{1}{g_m}$ (typically $50\,\Omega$ to $500\,\Omega$).
- Primary Function: Impedance matching buffer; steps down high source impedance to drive low-impedance coaxial cables or heavy capacitive loads without signal attenuation.

FET Constant Current Sources and Active Loads in ICs

- Two-Terminal JFET Current Regulator: Tying Gate to Source ($V_{GS} = 0\text{V}$) forces a JFET to operate at constant saturation current $I_D = I_{DSS}$.
- MOSFET Current Mirror: Uses a diode-connected MOSFET ($V_{DS} = V_{GS}$) to bias a secondary MOSFET in saturation, replicating reference current: $I_{out} = I_{ref} \left(\frac{W_2/L_2}{W_1/L_1} \right)$.
- Active Load Superiority: Replacing passive collector/drain resistors with MOSFET current mirrors in integrated amplifiers yields extremely high incremental load resistance ($R_L \approx r_o \sim 100$ kΩ to 1 MΩ).
- Ultra-High Voltage Gain: Enables single-stage IC amplifier gain $A_v = -g_m(r_{o1} \parallel r_{o2}) \approx 100 - 1000$ without requiring large DC supply voltages or silicon area.
- Cascode Current Mirrors: Stacked FET current sources increase output resistance to $R_{out} \approx g_m r_o^2$, providing near-ideal current regulation.

CMOS Digital Logic Architecture and Power Efficiency

- Complementary Topology: Integrates Pull-Up PMOS network connected to V_{DD} and Pull-Down NMOS network connected to Ground (GND).
- CMOS Inverter Operation: When $V_{in} = 0$V (Logic 0), NMOS is OFF, PMOS is ON $\implies V_{out} = V_{DD}$ (Logic 1). When $V_{in} = V_{DD}$ (Logic 1), NMOS is ON, PMOS is OFF $\implies V_{out} = 0$V (Logic 0).
- Zero Static DC Power Dissipation: In both logic states, one network is completely OFF ($I_{DC} \approx 0$ A), yielding near-zero static power dissipation: $P_{static} = V_{DD} I_{leak}$.
- Dynamic Power Dissipation: Power is consumed ONLY during switching transitions to charge load capacitance: $P_{dynamic} = C_L V_{DD}^2 f_{clock}$.
- CMOS NAND & NOR Gates: NAND uses series NMOS / parallel PMOS; NOR uses parallel NMOS / series PMOS, forming the foundation of all microprocessors and microcontrollers.

Power MOSFETs in Switching Power Electronics

- Vertical Double-Diffused MOSFET (VDMOS / HEXFET): Vertical current flow through substrate allows high breakdown voltages (> 1000V) and low ON-resistance ($R_{DS(on)} < 10$ mΩ).
- Switch-Mode Power Supplies (SMPS): High switching speeds (100 kHz to 5 MHz) drastically reduce size of inductors and capacitors in DC-DC Buck/Boost converters.
- H-Bridge Motor Drive Circuits: Four Power MOSFETs arranged in an H-bridge configuration enable bidirectional speed and direction control of DC and BLDC motors via Pulse-Width Modulation (PWM).
- Freewheeling Body Diode: Intrinsic parasitic PN body diode in Power MOSFETs provides automatic freewheeling conduction paths for inductive motor currents.
- Thermal Management: Power MOSFETs parallel easily due to negative temperature coefficient of carrier mobility, preventing thermal hot-spots.

RF / Microwave Amplifiers and Dual-Gate MOSFETs

- Low-Noise Amplifiers (LNAs): High input impedance and low high-frequency noise figure make GaAs MESFETs and SiGe MOSFETs preferred for wireless receiver front-ends (GPS, Wi-Fi, 5G).
- Dual-Gate MOSFET Architecture: Features two gates in series over a single channel, creating an integrated Cascode structure inside a single physical package.
- Reduction of Miller Effect: Gate 2 (ac grounded) shields Gate 1 from Drain, reducing feedback capacitance C_{gd} to near zero and boosting bandwidth above 1 GHz.
- Automatic Gain Control (AGC) Function: Varying DC voltage on Gate 2 modulates channel transconductance g_m continuously, adjusting RF amplifier gain over a 50 dB range without changing input tuning.
- RF Power Amplifiers: Lateral Diffused MOS (LDMOS) provides tens of watts of linear RF power for cellular basestation transmitters.

FETs in Sample-and-Hold (S/H) Circuits for ADCs

- Sample-and-Hold Function: Captures fast-changing analog voltage levels and holds them constant during Analog-to-Digital Converter (ADC) conversion cycles.
- Circuit Components: An input FET switch (or CMOS Transmission Gate), a hold capacitor (C_H), and a high-input-impedance Source Follower or Op-Amp buffer.
- Sample Phase: Gate control signal turns FET switch ON ($R_{ON} \sim 20\,\Omega$), rapidly charging hold capacitor C_H to input signal voltage v_{in}.
- Hold Phase: Control signal turns FET switch OFF ($R_{OFF} > 10^{10}\,\Omega$); capacitor holds charge with minimal leakage current ($I_{leak} < 1$ pA).
- Key Performance Metrics: Low aperture jitter, fast settling time, minimal charge injection from gate clock, and low droop rate ($dV/dt = I_{leak}/C_H$).

FET Sensor Interfacing and Ion-Sensitive FETs (ISFET)

- High-Impedance Sensor Interface: FET buffers interface directly with high-impedance sensors such as piezoelectric accelerometers, pH electrodes, and pyroelectric infrared (PIR) detectors.
- Ion-Sensitive FET (ISFET): Replaces metal gate electrode with an chemically sensitive ion-selective membrane exposed to an aqueous electrolyte solution.
- ISFET Operation: Hydronium ion concentration (pH) in solution generates an electrostatic surface potential at membrane boundary, shifting V_{Th} linearly according to Nernst Equation.
- Bio-FETs & DNA Chips: Functionalized gate surfaces bind specific biomolecules or DNA strands, modulating channel current for real-time label-free biosensing.
- CMOS Sensor Integration: Enables smart single-chip sensors combining bio-transducers, amplification, and digital signal processing on one silicon die.

Quantitative Problem: Voltage Variable Resistor Design

- Design Goal: Design an N-channel JFET Voltage Variable Resistor (VVR) operating between $R_{min} = 200\,\Omega$ and $R_{max} = 5$ kΩ.
- Given JFET Parameters: $I_{DSS} = 10$ mA, $V_P = -4.0$V.
- Step 1: Calculate Minimum Resistance at $V_{GS} = 0$V: $r_{DS(min)} = \frac{|V_P|}{2I_{DSS}} = \frac{4.0\text{V}}{2(10\text{ mA})} = \frac{4.0}{0.020} = 200\,\Omega$ (Matches R_{min} specification!).
- Step 2: Calculate Required Gate Bias for $R_{max} = 5$ kΩ: $r_{DS} = \frac{r_{DS(min)}}{1 - V_{GS}/V_P} \implies 5000 = \frac{200}{1 - V_{GS}/(-4.0)}$.
- Step 3: Solve for V_{GS}: $1 - \frac{V_{GS}}{-4.0} = \frac{200}{5000} = 0.04 \implies \frac{V_{GS}}{4.0} = 0.04 - 1 = -0.96 \implies V_{GS} = -3.84$V.
- Conclusion: Adjusting gate voltage V_{GS} from 0V to -3.84V controls channel resistance continuously from $200\,\Omega$ up to $5000\,\Omega$.

Emerging Trends: Gallium Nitride (GaN) & Silicon Carbide (SiC) FETs

- Silicon Physical Limits: Silicon MOSFETs approach material limits in breakdown voltage ($E_{crit} \approx 0.3$ MV/cm) and thermal conductivity.
- Wide-Bandgap Advantages: GaN (3.4 eV) and SiC (3.2 eV) feature $10\times$ higher critical breakdown electric field ($E_{crit} \approx 3.0$ MV/cm) than Silicon (1.1 eV).
- High-Electron-Mobility Transistor (GaN HEMT): Utilizes 2D Electron Gas (2DEG) at AlGaN/GaN heterojunction, achieving ultra-low $R_{DS(on)}$ and switching speeds > 10 MHz.
- Electric Vehicle (EV) Power Inverters: SiC MOSFETs operate at junction temperatures $> 200°C$ and voltages > 1200V, improving EV drive range by $5 - 10\%$.
- Compact Fast Chargers: GaN power switches enable ultra-compact USB-C laptop/smartphone chargers operating at megahertz frequencies.

Summary: Comprehensive Application Taxonomy of FETs

- Analog Signal Modulation: Voltage Variable Resistors (VVR), AGC attenuators, and CMOS Transmission Gates.
- High-Impedance Amplification: Source Followers, buffer stages, and electrometer interfaces.
- Integrated Circuit Design: Active current sources, MOSFET current mirrors, and cascode amplifiers.
- Digital VLSI Systems: CMOS logic gates (Inverter, NAND, NOR) with near-zero static power dissipation.
- Power & RF Electronics: VDMOS/HEXFET in SMPS and H-Bridges; GaN/SiC FETs in EV power electronics; Dual-Gate MOSFETs in RF LNAs.