Lecture 9: Comparison of BJT, JFET, MOSFET

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: Three-Way Transistor Comparison

- Fundamental Device Physics & Carrier Types (Bipolar vs Unipolar).
- Control Mechanism Comparison: $I_C = \beta I_B$ vs Shockley & Square-Law models.
- Input Impedance Analysis ($r_\pi \sim 1$ kΩ vs $R_{in} \sim 10^8\,\Omega$ vs $R_{in} \sim 10^{12}\,\Omega$).
- Transconductance (g_m) & Voltage Gain Comparison.
- Noise Performance, Thermal Stability, and Thermal Runaway.
- Switching Speed, Power Dissipation, and High-Frequency Limits.
- Comprehensive Summary Comparison Matrix & Application Selection Guide.

Device Physics: Bipolar vs. Unipolar Carrier Transport

- BJT (Bipolar Junction Transistor): Bipolar transport; current conduction involves BOTH majority and minority charge carriers (electrons and holes).
- JFET (Junction Field-Effect Transistor): Unipolar transport; current conducted strictly by majority carriers (electrons in N-channel, holes in P-channel) flowing through a physical channel.
- MOSFET (Metal-Oxide-Semiconductor FET): Unipolar transport; current conducted exclusively by majority carriers flowing through a physically built-in or field-induced inversion channel.
- Minority Carrier Storage Effect: BJTs suffer from minority carrier storage delay in the base during turn-off; FETs exhibit zero minority carrier storage delay.
- Radiation Hardness: Unipolar FETs demonstrate significantly higher resistance to nuclear radiation damage than BJTs, as radiation creates recombination centers affecting minority carrier lifetime.

Control Mechanism: Current-Controlled vs. Voltage-Controlled

- BJT Control Equation: Current-controlled device; small input base current I_B controls large output collector current: $I_C = \beta I_B = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$.
- JFET Control Equation: Voltage-controlled device; gate-to-source reverse voltage V_{GS} modulates depletion channel width: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ (for $V_P \leq V_{GS} \leq 0$).
- D-MOSFET Control Equation: Voltage-controlled device; insulated gate potential operates across depletion and enhancement: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
- E-MOSFET Control Equation: Voltage-controlled device; gate bias induces channel above threshold: $I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{Th})^2$.
- Static Drive Power: BJTs demand continuous DC base drive power ($P_{drive} = V_{BE} I_B$); FETs require ZERO static DC gate current ($I_G \approx 0$ A).

Input Impedance Analysis (R_{in} / Z_{in} Comparison)

- BJT Input Impedance: Low to moderate ($R_{in} = r_\pi = \frac{\beta V_T}{I_{CQ}} \approx 1$ kΩ to 10 kΩ); forward-biased base-emitter PN junction draws continuous base current.
- JFET Input Impedance: High ($R_{in} = R_{gate} \parallel R_{reverse\_PN} \approx 10^8\Omega$ to $10^{10}\Omega$); reverse-biased gate-channel PN junction limits gate leakage to nanoamperes ($I_{GSS} \sim 1$ nA).
- MOSFET Input Impedance: Extremely High ($R_{in} \approx 10^{12}\Omega$ to $10^{15}\Omega$); dielectric SiO_2 oxide layer provides true physical DC isolation with picoampere leakage ($I_{GSS} \sim 1$ pA).
- Loading Effects: High input impedance of FETs eliminates loading errors when buffering high-impedance sensors (e.g., pH probes, piezoelectric crystals, capacitive transducers).
- ESD Susceptibility: Extreme insulation makes MOSFET gates vulnerable to Electrostatic Discharge (ESD) damage, whereas BJTs are robust against static charge accumulation.

Transconductance (g_m) and Voltage Gain Capabilities

- BJT Transconductance: Extremely High; proportional to DC bias current: $g_{m(BJT)} = \frac{I_C}{V_T} \approx \frac{I_C}{26\ \text{mV}} \approx 38.5 \times I_C$ mS (at 1 mA, $g_m = 38.5$ mS).
- JFET Transconductance: Moderate; $g_{m(JFET)} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) \approx 1$ mS to 5 mS.
- MOSFET Transconductance: Moderate to High; $g_{m(MOS)} = \sqrt{2\mu C_{ox}(W/L)I_D} \approx 1$ mS to 20 mS (scalable by increasing channel width W).
- Voltage Gain Comparison: Single-stage BJT amplifier achieves higher voltage gain ($A_v = -g_m R_C \approx 100 - 500$) than standard FET stages ($A_v = -g_m R_D \approx 10 - 50$) due to superior g_m per unit bias current.
- Gain-Bandwidth Product: BJT provides high transconductance-to-current ratio (g_m/I_D), making it ideal for ultra-high-frequency analog RF amplifiers.

Noise Characteristics: Shot Noise vs. Thermal & Surface Noise

- BJT Noise Profile: Exhibits Shot Noise due to charge carriers crossing potential barriers ($i_{n,shot}^2 = 2qI_B\Delta f$) and Thermal Noise from base resistance $r_{bb'}$.
- JFET Noise Profile: Lowest noise at low-to-medium frequencies; zero shot noise (no carrier junction crossing in channel), low $1/f$ flicker noise because channel is buried inside bulk silicon away from surface traps.
- MOSFET Noise Profile: Higher $1/f$ flicker noise at low frequencies due to carrier trapping at the SiO_2-silicon surface interface traps; thermal channel noise $i_{n,ch}^2 = 4kT(\frac{2}{3}g_m)\Delta f$ dominates at high frequencies.
- Low-Noise Audio Applications: JFETs are the premier choice for ultra-low-noise preamplifiers (condenser microphones, audio pickup cartridges).
- RF Noise Performance: Dual-gate MOSFETs and GaAs MESFETs excel in RF Low-Noise Amplifiers (LNAs) above 1 GHz.

Thermal Behavior and Thermal Runaway Resistance

- BJT Temperature Coefficient: Positive temperature coefficient of collector current (I_C increases with temperature T as V_{BE} decreases by -2 mV/$^\circ$C).
- Thermal Runaway Hazard in BJTs: Higher $T \implies$ Higher $I_C \implies$ Higher power dissipation $P_D \implies$ Higher T, leading to destructive thermal runaway unless stabilized by emitter resistor R_E.
- FET Temperature Coefficient: Negative temperature coefficient of drain current at high bias levels; carrier mobility decreases with temperature ($\mu_n \propto T^{-1.5}$) due to increased lattice scattering.
- Self-Limiting Safety in FETs: Higher $T \implies$ Lower carrier mobility $\mu_n \implies$ Lower drain current $I_D \implies$ Lower power dissipation, inherently preventing thermal runaway.
- Parallel Operation: MOSFETs can be connected in parallel without current-hogging resistors; BJTs in parallel require ballasting resistors to prevent one device from hogging all current.

Frequency Response and Switching Speed Comparison

- BJT Switching Delays: Limited by minority carrier storage time (t_s) during saturation turn-off; transition frequency $f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$ reaches tens of GHz in advanced SiGe heterojunction BJTs (HBTs).
- JFET Frequency Response: Limited by large gate-to-channel PN junction capacitance ($C_{iss} \sim 10 - 50$ pF); generally restricted to frequencies below 500 MHz.
- MOSFET Switching Speed: Extremely fast switching (nanoseconds); zero minority carrier storage delay allows multi-megahertz operation in switching power supplies (SMPS).
- MOSFET Parasitic Gate Drive Delay: High input capacitance requires substantial transient current to charge/discharge C_{gs} and C_{gd} (Miller capacitance) rapidly during switching transitions.
- RF Power Supremacy: LDMOS (Lateral Diffused MOS) and GaN HEMT devices dominate modern cellular basestation RF power amplifiers.

Fabrication Scalability and VLSI Integration Density

- BJT Fabrication Complexity: Requires complex multi-step isolation diffusion wells, deep collector sinks, and larger silicon area per transistor; limited integration density.
- JFET Fabrication Density: Difficult to integrate in high-density VLSI; primarily manufactured as discrete devices or specialized bi-FET op-amp front-ends.
- MOSFET VLSI Dominance: Extremely simple planar self-aligned structure; occupies minimal silicon real estate; enables billions of transistors per chip in modern CMOS microprocessors.
- CMOS Power Advantage: Complementary MOS (NMOS + PMOS) logic consumes ZERO static DC power, drawing power only during switching transients ($P = CfV_{DD}^2$).
- BiCMOS Technology: Combines high-input-impedance MOSFETs and high-drive BJT output stages on a single IC substrate for premium analog/digital performance.

Quantitative Problem: Transconductance & Drive Power Comparison

- Scenario: Compare a BJT ($I_{CQ} = 2$ mA, $\beta = 100$) and an NMOS ($K_n = 4$ mA/V^2, $I_{DQ} = 2$ mA) operating at room temperature ($V_T = 26$ mV).
- BJT Transconductance ($g_{m,BJT}$): $g_{m,BJT} = \frac{I_{CQ}}{V_T} = \frac{2\text{ mA}}{26\text{ mV}} = 76.92$ mS.
- MOSFET Transconductance ($g_{m,MOS}$):
  $g_{m,MOS} = \sqrt{2K_n I_{DQ}} = \sqrt{2 \times 4\text{ mA/V}^2 \times 2\text{ mA}} = \sqrt{16} = 4.0$ mS.
- BJT DC Input Drive Current (I_B): $I_B = \frac{I_{CQ}}{\beta} = \frac{2\text{ mA}}{100} = 20\ \mu$A.
- MOSFET DC Input Drive Current (I_G): $I_G = 0.00\ \mu$A (ideal dielectric oxide isolation).
- Conclusion: BJT achieves $\approx 19.2\times$ higher transconductance, but demands 20 μA continuous DC drive current compared to 0 μA for MOSFET.

Master Technical Comparison Matrix: BJT vs. JFET vs. MOSFET

- Primary Carrier: BJT = Bipolar (n & p); JFET = Unipolar (majority); MOSFET = Unipolar (majority).
- Control Mechanism: BJT = Current (I_B); JFET = Voltage (V_{GS}); MOSFET = Voltage (V_{GS}).
- Input Resistance (R_{in}): BJT = $1 - 10$ kΩ; JFET = $10^8 - 10^{10}\,\Omega$; MOSFET = $10^{12} - 10^{15}\,\Omega$.
- Transconductance (g_m): BJT = Extremely High (I_C/V_T); JFET = Low-Moderate; MOSFET = Moderate-High (scalable).
- Thermal Coefficient: BJT = Positive (runaway risk); JFET = Negative (self-limiting); MOSFET = Negative (self-limiting).
- Low-Frequency Noise: BJT = Moderate (shot noise); JFET = Lowest (buried channel); MOSFET = High ($1/f$ surface noise).
- Static Power Dissipation: BJT = High ($V_{BE}I_B$); JFET = Very Low; MOSFET = Zero ($I_G = 0$).

Engineering Selection Guide: Choosing the Optimal Transistor

- Select BJT when: Requiring maximum voltage gain per stage, ultra-high transconductance, low output resistance drive, or discrete high-frequency RF amplification.
- Select JFET when: Designing ultra-low-noise front-end audio preamplifiers, high-input-impedance electrometers, or low-distortion analog switches.
- Select MOSFET when: Designing high-density digital VLSI microprocessors (CMOS), high-efficiency switch-mode power supplies (SMPS), or high-voltage EV inverters.
- Select IGBT (Insulated-Gate Bipolar Transistor) when: Combining MOSFET insulated gate drive with BJT low saturation voltage in mega-watt grid power electronics.

Summary: Comparative Transistor Performance Synthesis

- BJT Strength: Highest transconductance (g_m), superior voltage gain, but low input resistance and thermal runaway risk.
- JFET Strength: High input resistance ($10^8\,\Omega$), lowest low-frequency noise, but low transconductance and limited IC scalability.
- MOSFET Strength: Supreme input resistance ($10^{12}\,\Omega$), zero static drive power, fast switching, zero thermal runaway, and dominant VLSI integration.
- Key Paradigm Shift: Modern electronics has shifted predominantly toward MOSFET (CMOS) technology for digital and power systems, retaining BJTs and JFETs for specialized analog niches.