Lecture 8: Enhancement type MOSFET

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: E-MOSFET V-I Characteristics & Modeling

- Operating Modes Overview: Cutoff, Triode, and Saturation region conditions.
- Triode / Ohmic Region Derivation: Low V_{DS} channel resistance modeling.
- Pinch-off Mechanics & Onset of Saturation ($V_{DS(sat)} = V_{GS} - V_{Th}$).
- Saturation Region Derivation: Square-law drain current equation.
- Channel Length Modulation (λ) and Early Voltage (V_A).
- Small-Signal Parameters: Transconductance g_m and Output Resistance r_o formulas.
- Numerical Circuit Problem Walkthrough & Output Curve Plotting.

Cutoff Region Physics ($V_{GS} < V_{Th}$ for NMOS)

- Sub-Threshold Condition: Gate-to-source voltage is less than threshold voltage ($V_{GS} < V_{Th}$).
- Absence of Inversion Channel: Insufficient surface potential prevents formation of mobile electron inversion layer; channel region remains depleted.
- Ideal Current: Ideal drain current is strictly zero ($I_D = 0$ A); device acts as an open switch.
- Subthreshold Conduction (Real-World): Small diffusion-dominated leakage current flows: $I_D(sub) = I_{S0} \exp\left(\frac{V_{GS} - V_{Th}}{nV_T}\right)$.
- Off-State Power Dissipation: In VLSI CMOS chips with billions of transistors, static subthreshold leakage power ($P_{static} = V_{DD} \times I_{sub}$) is a major power constraint.

Triode / Ohmic Region Mechanics ($V_{GS} \geq V_{Th}$ & $V_{DS} < V_{GS} - V_{Th}$)

- Conduction Conditions: Gate voltage exceeds threshold ($V_{GS} \geq V_{Th}$) AND drain voltage is low ($V_{DS} < V_{GS} - V_{Th}$).
- Continuous Channel Profile: Inversion layer remains continuous from Source to Drain along entire channel length L.
- Drain Current Derivation: $I_D = k'_n \frac{W}{L} \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$
- Process Transconductance Parameter (k'_n): Defined as $k'_n = \mu_n C_{ox} = \mu_n \frac{\epsilon_{ox}}{t_{ox}}$ (measured in A/V^2 or $\mu A/V^2$).
- Device Transconductance Parameter (K_n): Defined as $K_n = k'_n \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$.

Deep Triode Region: Voltage-Controlled Resistance (VCR)

- Very Small V_{DS} Limit ($V_{DS} \ll V_{GS} - V_{Th}$): The quadratic term $\frac{1}{2}V_{DS}^2$ becomes negligible compared to $(V_{GS} - V_{Th})V_{DS}$.
- Linearized Drain Current Equation: $I_D \approx k_n' \frac{W}{L}(V_{GS} - V_{Th})V_{DS} = K_n(V_{GS} - V_{Th})V_{DS}$
- Ohmic Channel Resistance Formula ($R_{DS(on)}$): $R_{DS(on)} = \frac{V_{DS}}{I_D} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_{Th})} = \frac{1}{K_n V_{OV}}$
- Gate-Voltage Modulated Resistance: Channel resistance $R_{DS(on)}$ is inversely proportional to overdrive voltage $V_{OV} = V_{GS} - V_{Th}$.
- Practical Applications: Used in analog voltage-controlled attenuators, electronic potentiometers, and analog switches.

Pinch-Off Physics and Saturation Boundary Condition

- Channel Tapering: As V_{DS} increases, potential along channel $V(x)$ rises from 0V at source to V_{DS} at drain, reducing local gate-to-channel voltage $V_{GS} - V(x)$.
- Pinch-Off Onset Voltage ($V_{DS(sat)}$): At the drain end ($x = L$), local gate-to-channel voltage drops to exactly threshold voltage: $V_{GS} - V(L) = V_{Th} \implies V_{DS(sat)} = V_{GS} - V_{Th} = V_{OV}$.
- Physical Pinch-Off Point: Inversion charge at drain drops to zero ($Q_n(L) = 0$), pinching off the channel tip near the drain contact.
- Electron Drift Across Depletion Region: Electrons reaching the pinch-off point are swept across the narrow high-electric-field depletion region into the drain, sustaining steady current flow.
- Current Saturation Independence: Further increases in $V_{DS} > V_{DS(sat)}$ extend the pinch-off region length toward the source, but do not increase the voltage drop across the active channel.

Saturation Region Mathematics: Ideal Square-Law Model

- Saturation Conditions: Gate voltage above threshold ($V_{GS} \geq V_{Th}$) AND drain voltage above saturation onset ($V_{DS} \geq V_{GS} - V_{Th}$).
- Square-Law Equation Derivation: Substituting $V_{DS} = V_{GS} - V_{Th}$ into triode equation yields: $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{Th})^2 = \frac{1}{2} K_n (V_{GS} - V_{Th})^2$
- Drain Voltage Independence: Ideal saturation current I_D depends quadratically on gate overdrive voltage ($V_{GS} - V_{Th}$) and is completely independent of V_{DS}.
- Amplifier Region of Operation: Analog voltage amplifiers bias the MOSFET strictly in Saturation, where high incremental transconductance g_m yields maximum voltage gain.
- PMOS Saturation Equation: $I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{GS} - V_{Th,p})^2 = \frac{1}{2} k_p' \frac{W}{L} (V_{SG} - |V_{Th,p}|)^2$.

Channel Length Modulation (λ) and Output Resistance

- Physical Origin: As V_{DS} increases above $V_{DS(sat)}$, the pinch-off point moves towards the source, reducing effective channel length from L to $L' = L - \Delta L$.
- Aspect Ratio Increase (W/L'): Since effective length L' shrinks, factor W/L' increases, causing drain current to rise slightly with increasing V_{DS}.
- Channel Length Modulation Parameter (λ): Quantifies finite output resistance, measured in V^{-1}; inverse of Early Voltage ($V_A = 1/\lambda$).
- Modified Saturation Current Equation: $I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{Th})^2(1 + \lambda V_{DS})$
- Length Dependency: λ is inversely proportional to nominal channel length L ($\lambda \propto 1/L$); longer channels exhibit flatter saturation curves.

Derivation of Small-Signal Transconductance (g_m)

- Definition of Transconductance: Rate of change of drain current with respect to gate-to-source voltage at a fixed Q-point: $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{const}}$.
- Formulation 1 (Overdrive Voltage Form): $g_m = k_n' \frac{W}{L}(V_{GS} - V_{Th}) = K_n V_{OV}$
- Formulation 2 (Current & Aspect Ratio Form): $g_m = \sqrt{2k_n' \frac{W}{L} I_D} = \sqrt{2K_n I_D}$
- Formulation 3 (Current & Overdrive Form): $g_m = \frac{2I_D}{V_{GS}-V_{Th}} = \frac{2I_D}{V_{OV}}$
- Design Implications: To maximize g_m at a fixed DC bias current I_D, designers must minimize overdrive voltage V_{OV} by increasing channel width W.

Derivation of Small-Signal Output Resistance (r_o)

- Definition of Small-Signal Output Resistance: Incremental internal resistance looking into the drain terminal: $r_o = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}_{V_{GS}=\text{const}}$.
- Mathematical Derivation: Differentiating modified saturation equation yields $\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}K_n(V_{GS} - V_{Th})^2\lambda = \frac{\lambda I_D}{1+\lambda V_{DS}} \approx \lambda I_D$.
- Output Resistance Formulas: $r_o = \frac{1}{\lambda I_{D0}} = \frac{V_A}{I_D}$
- Early Voltage (V_A): Extrapolated negative voltage intercept on the V_{DS} axis where saturation curves converge ($V_A = 1/\lambda$ or $V_A = V'_A L$).
- Impact on Gain: Finite output resistance r_o limits intrinsic voltage gain of single-stage amplifier to $A_{v0} = -g_m r_o = -\frac{2V_A}{V_{GS}-V_{Th}}$.

Drain Output Characteristics Family Curves Analysis

- Three Operating Regions Mapping: Cutoff region along horizontal axis ($V_{GS} < V_{Th}$); Triode region to the left of parabolic boundary ($V_{DS} < V_{GS} - V_{Th}$); Saturation region to the right ($V_{DS} \geq V_{GS} - V_{Th}$).
- Pinch-Off Parabola Boundary: Locus of pinch-off points defined by curve $I_{D(sat)} = \frac{1}{2}K_n V_{DS}^2$.
- Gate Voltage Parameter Steps: Family of curves plotted for increasing V_{GS} steps ($V_{Th} + 0.5$V, $V_{Th} + 1.0$V, $V_{Th} + 1.5$V, etc.).
- Saturation Slope Visualization: Curves slope slightly upward in saturation due to finite λ; extrapolating backward converges at $-V_A$ on horizontal axis.
- Breakdown Boundary: At extreme $V_{DS} > V_{DS(max)}$, drain-substrate junction breakdown causes sharp vertical current rise.

Numerical Analysis of E-MOSFET Bias Point & Region Identification

- Circuit Parameters: Given NMOS with $V_{Th} = 1.0\text{V}$, $k_n' = 100\ \mu\text{A/V}^2$, $W/L = 10$, $\lambda = 0.02\ \text{V}^{-1}$. Circuit biased at $V_{GS} = 3.0\text{V}$ and $V_{DS} = 5.0\text{V}$.
- Step 1: Determine Overdrive Voltage (V_{OV}): $V_{OV} = V_{GS} - V_{Th} = 3.0\text{V} - 1.0\text{V} = 2.0\text{V}$.
- Step 2: Check Saturation Condition: $V_{DS} = 5.0\text{V} \geq V_{OV} = 2.0\text{V} \implies$ Transistor is in SATURATION.
- Step 3: Calculate K_n: $K_n = k_n' \frac{W}{L} = 100\ \mu\text{A/V}^2 \times 10 = 1.0\ \text{mA/V}^2$.
- Step 4: Compute Drain Current I_D:
  $I_D = \frac{1}{2}(1.0\ \text{mA/V}^2)(2.0\text{V})^2 \times [1 + (0.02)(5.0)] = 0.5 \times 4.0 \times (1.10) = 2.20\ \text{mA}$.
- Step 5: Compute Transconductance g_m and Output Resistance r_o:
  $g_m = K_n V_{OV} = (1.0\ \text{mA/V}^2)(2.0\text{V}) = 2.0\ \text{mS}$; $r_o = \frac{1}{\lambda I_{D0}} = \frac{1}{(0.02\ \text{V}^{-1})(2.0\ \text{mA})} = 25\ \text{k}\Omega$.

Parasitic Capacitances and High-Frequency Model

- Gate Oxide Capacitances: Gate-to-Source capacitance C_{gs} and Gate-to-Drain capacitance C_{gd}.
- Triode Region Capacitances: $C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$.
- Saturation Region Capacitances: Channel pinches off at drain; $C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$, while $C_{gd} = WL_{ov}C_{ox}$ (overlap capacitance only).
- Cutoff Region Capacitances: $C_{gs} = C_{gd} = WL_{ov}C_{ox}$; Gate-to-Body capacitance $C_{gb} = WLC_{ox}$.
- Transition Frequency (f_T): Frequency at which short-circuit current gain drops to unity: $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{\mu_n(V_{GS}-V_{Th})}{2\pi L^2}$.

Summary of E-MOSFET Operational Equations

- Cutoff ($V_{GS} < V_{Th}$): $I_D = 0$ A.
- Triode ($V_{GS} \geq V_{Th}, V_{DS} < V_{GS} - V_{Th}$): $I_D = k'_n \frac{W}{L}\left[(V_{GS} - V_{Th})V_{DS} - \frac{1}{2}V_{DS}^2\right]$.
- Deep Triode ($V_{DS} \ll V_{GS} - V_{Th}$): $R_{DS(on)} = \frac{1}{k'_n(W/L)(V_{GS} - V_{Th})}$.
- Saturation ($V_{GS} \geq V_{Th}, V_{DS} \geq V_{GS} - V_{Th}$): $I_D = \frac{1}{2}k'_n \frac{W}{L}(V_{GS} - V_{Th})^2(1 + \lambda V_{DS})$.
- Small-Signal Formulas: $g_m = \sqrt{2K_n I_D} = K_n V_{OV}$; $r_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$.