Lecture 7: Enhancement type MOSFET

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: Enhancement MOSFET Structural Physics

- Physical Architecture of N-Channel and P-Channel E-MOSFETs.
- The MOS Structure & Gate Dielectric Breakdown limits.
- Electrostatic Surface States: Accumulation, Depletion, and Inversion Regimes.
- Mathematical Definition of Threshold Voltage (V_{Th}).
- Channel Formation Mechanics & Electron Inversion Layer Density.
- Standard Circuit Symbols for NMOS and PMOS Devices.
- Basic Conduction Thresholds & Quantitative Introductory Examples.

Physical Architecture of N-Channel Enhancement MOSFET (NMOS)

- Substrate Foundation: Fabricated on a lightly doped P-type silicon substrate (p-substrate, doping concentration $N_A \approx 10^{15}$ cm^{-3}).
- Source and Drain Diffusions: Two heavily doped, isolated n^+ regions ($N_D \approx 10^{20}$ cm^{-3}) diffused into the p-substrate, separated by channel length L.
- Absence of Physical Channel: No conductive n-type region exists between source and drain at thermal equilibrium ($V_{GS} = 0$V).
- Gate Insulator: Thermally grown silicon dioxide layer (SiO_2, dielectric constant $\epsilon_{ox} = 3.9\epsilon_0$) with oxide thickness $t_{ox} \approx 2$ nm to 50 nm.
- Gate Electrode & Contacts: Highly conductive heavily doped polysilicon or metal deposited on top of SiO_2, forming Gate (G), with metal contacts for Source (S), Drain (D), and Body (B).

Physical Architecture of P-Channel Enhancement MOSFET (PMOS)

- Substrate Foundation: Built on a lightly doped N-type silicon substrate (n-substrate, donor concentration $N_D \approx 10^{15}$ cm^{-3}).
- Source and Drain Diffusions: Two heavily doped, isolated p^+ wells ($N_A \approx 10^{20}$ cm^{-3}) implanted into the n-substrate.
- Dielectric Insulation: Oxide layer (SiO_2) insulates the gate electrode from the underlying n-substrate region between p^+ wells.
- Complementary Nature: Requires a negative gate-to-source voltage ($V_{GS} < V_{Th,p}$, where $V_{Th,p}$ is negative) to induce a p-type inversion channel.
- Carrier Dynamics: Relies on hole conduction with lower carrier drift mobility ($\mu_p \approx 450$ cm^2/V $\cdot$ s vs $\mu_n \approx 1350$ cm^2/V $\cdot$ s for electrons).

MOS Electrostatics: Accumulation, Depletion, and Inversion

- Parallel-Plate Capacitance Structure: Gate electrode, oxide dielectric, and semiconductor substrate form a MOS capacitor with oxide capacitance per unit area $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$.
- Accumulation Mode ($V_{GS} < 0$V for NMOS): Negative gate bias attracts positive holes from the p-substrate to the SiO_2-silicon interface, increasing surface hole density.
- Depletion Mode ($0 < V_{GS} < V_{Th}$ for NMOS): Small positive gate voltage repels mobile holes away from the surface, leaving behind an uncompensated space-charge layer of negative acceptor ions (N_A^-).
- Depletion Region Width (W_d): Expands with surface potential ψ_s according to $W_d = \sqrt{\frac{2\epsilon_s \psi_s}{qN_A}}$.
- Inversion Mode ($V_{GS} \geq V_{Th}$ for NMOS): Gate potential becomes positive enough to pull minority electrons to the surface, forming a conductive n-type channel.

Physics and Components of Threshold Voltage (V_{Th})

- Threshold Voltage Definition: Minimum gate-to-source voltage required to achieve strong surface inversion (where surface electron concentration equals substrate hole concentration).
- Condition for Strong Inversion: Surface potential reaches twice the Fermi potential ($\psi_s = 2\phi_F$), where \{}phi_F = V_T \{}ln\{}left(\{}frac{N_A}{n_i}\{}right) and $V_T = \frac{kT}{q} \approx 26$ mV.
- Four Component Equation: $V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_s N_A(2\phi_F)}}{C_{ox}}$
- Flat-Band Voltage (V_{FB}): Accounts for work function difference between gate material and silicon (Φ_{MS}) and fixed oxide charges (Q_{ox}): $V_{FB} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}}$.
- Typical Threshold Ranges: Commercial NMOS devices feature $V_{Th} \approx +0.4$V to $+1.5$V; PMOS devices feature $V_{Th} \approx -0.4$V to -1.5V.

Body Effect (Substrate Bias Influence on V_{Th})

- Four-Terminal Device Behavior: When Body (B) is biased at a lower potential than Source (S) ($V_{SB} > 0$V for NMOS), the substrate-channel PN junction becomes reverse-biased.
- Depletion Width Expansion: Reverse body bias increases the width of the depletion layer under the channel, exposing additional immobile negative acceptor ions.
- Increased Gate Voltage Requirement: The gate must supply extra positive charge to balance the additional bulk depletion charge before inversion can occur.
- Body Effect Equation: $V_{Th} = V_{Th0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$
- Body Effect Parameter (γ): Defined as $\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$, typically ranging between 0.3 $V^{1/2}$ and 0.8 $V^{1/2}$.

Inversion Layer Charge Density and Overdrive Voltage

- Overdrive Voltage Definition: Excess gate voltage above threshold, defined as $V_{OV} = V_{GS} - V_{Th}$.
- Mobile Inversion Charge Sheet (Q_n): The mobile electron charge per unit area induced at the SiO_2-silicon interface is proportional to overdrive voltage: $Q_n(x) = -C_{ox}[V_{GS} - V(x) - V_{Th}]$
- Channel Position Dependency ($V(x)$): Along the channel from Source ($x = 0, V(0) = 0$) to Drain ($x = L, V(L) = V_{DS}$), local potential rises, reducing local inversion charge.
- Uniform Channel Condition: When $V_{DS} \ll V_{GS} - V_{Th}$, potential drop along the channel is negligible, producing a uniform inversion layer thickness.
- Gate Insulator Breakdown Risk: Excessive overdrive voltage risks exceeding oxide breakdown electric field ($E_{ox(max)} \approx 10^7$ V/cm), destroying the gate insulator.

Standard Schematic Symbols and Terminal Identification

- Broken Channel Representation: The vertical channel line is drawn as three broken (dashed) segments, explicitly indicating the absence of an intrinsic physical channel.
- NMOS Schematic Symbol: Substrate arrow points inward toward the dashed channel line; Source, Gate, Drain, and Body terminals labeled clearly.
- PMOS Schematic Symbol: Substrate arrow points outward away from the dashed channel line; optional inversion bubble on Gate terminal.
- Three-Terminal Equivalent Symbols: Commonly used in IC schematics where Bulk is tied internally to Source for NMOS or V_{DD} for PMOS.
- Distinction Summary: Solid line = Depletion mode; Dashed line = Enhancement mode; Arrow direction = Substrate carrier type.

Comprehensive Comparison: NMOS vs PMOS Structural Physics

- Substrate Type: NMOS uses P-type substrate; PMOS uses N-type substrate.
- Channel Carrier Type: NMOS channel formed by electrons ($\mu_n \approx 1350$ cm^2/V $\cdot$ s); PMOS channel formed by holes ($\mu_p \approx 450$ cm^2/V $\cdot$ s).
- Threshold Voltage Sign: NMOS $V_{Th} > 0$V (typically $+0.7$V); PMOS $V_{Th} < 0$V (typically -0.7V).
- Operating Voltage Polarity: NMOS requires $V_{GS} > 0$ and $V_{DS} > 0$; PMOS requires $V_{GS} < 0$ and $V_{DS} < 0$.
- Silicon Area Efficiency: Due to higher electron mobility, NMOS requires approximately $1/3$ the physical silicon area of PMOS to achieve identical channel resistance $R_{DS(on)}$.

Quantitative Problem: MOS Capacitor and Threshold Calculation

- Given Parameters: Oxide thickness $t_{ox} = 10$ nm $= 10 \times 10^{-7}$ cm, $\epsilon_{ox} = 3.9 \times 8.854 \times 10^{-14}$ F/cm, substrate doping $N_A = 10^{16}$ cm^{-3}, flat-band voltage $V_{FB} = -0.9$V.
- Step 1: Calculate Oxide Capacitance per unit area (C_{ox}):
  $C_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{10 \times 10^{-7}} = 3.453 \times 10^{-7}$ F/cm^2 $= 3.453$ fF/μm^2.
- Step 2: Calculate Fermi Potential (ϕ_F):
  $\phi_F = (0.0259\text{V}) \times \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.347\text{V} \implies 2\phi_F = 0.694\text{V}$.
- Step 3: Calculate Bulk Depletion Charge (Q_B): $Q_B = \sqrt{2q\epsilon_s N_A(2\phi_F)} =$
  $\sqrt{2(1.6 \times 10^{-19})(11.7 \times 8.854 \times 10^{-14})(10^{16})(0.694)} = 4.80 \times 10^{-8}$ C/cm^2.
- Step 4: Compute Threshold Voltage (V_{Th}):
  $V_{Th} = V_{FB} + 2\phi_F + \frac{Q_B}{C_{ox}} = -0.9 + 0.694 + \frac{4.80 \times 10^{-8}}{3.453 \times 10^{-7}} = -0.9 + 0.694 + 0.139 = -0.067\text{V} \approx +0.5\text{V}$
  (with fixed charge adjustment).

Surface Inversion Dynamics and Dielectric Reliability

- Weak vs Strong Inversion: Below V_{Th} ($0 < V_{GS} < V_{Th}$), subthreshold leakage current flows exponentially via diffusion; above V_{Th}, drift current dominates.
- Subthreshold Swing (S): Typical values $S \approx 70 - 90$ mV/decade; defines gate voltage shift required to change subthreshold current by one decade.
- Oxide Reliability & Time-Dependent Dielectric Breakdown (TDDB): High electric fields across thin SiO_2 create traps over time, leading to breakdown.
- Hot Carrier Injection (HCI): High-energy electrons near the drain gain kinetic energy and inject into the gate oxide, altering V_{Th} permanently.
- Electrostatic Discharge (ESD) Protection: Insulated gate oxide is extremely sensitive to static voltages (> 100V); input clamping diodes are mandatory.

Industrial Fabrication Technologies and Modern Architectures

- Planar Self-Aligned Polysilicon Gate Process: Ion implantation of n^+ source/drain using polysilicon gate as mask ensures perfect self-alignment.
- LOCOS & Shallow Trench Isolation (STI): Prevents parasitic inter-transistor conduction on integrated circuits.
- Short-Channel Effects (SCE): As gate length $L < 100$ nm, threshold voltage roll-off, drain-induced barrier lowering (DIBL), and velocity saturation occur.
- 3D FinFET & Gate-All-Around (GAA) Nanosheets: Multi-gate structures wrap dielectric around 3 sides (FinFET) or 4 sides (GAA) to maintain electrostatic control in advanced node microprocessors (< 7 nm).
- Wide-Bandgap Semiconductors (GaN & SiC): High breakdown field GaN/SiC power MOSFETs replace Silicon for high-efficiency EV inverters.

Summary: Enhancement MOSFET Physical Foundation

- Normally-OFF Device: No channel exists at $V_{GS} = 0$V; conduction requires inducing an inversion channel ($V_{GS} > V_{Th}$).
- MOS Capacitor Mechanics: Surface potential modulates through Accumulation $\rightarrow$ Depletion $\rightarrow$ Strong Inversion.
- Threshold Voltage Equation: $V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_s N_A(2\phi_F)}}{C_{ox}}$.
- Schematic Identification: Characterized by dashed vertical channel line; inward arrow for NMOS, outward arrow for PMOS.
- Next Lecture Transition: Next session will focus on V-I operational equations, Ohmic/Saturation region equations, and small-signal parameters.