Lecture 6: Depletion type MOSFET

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: Depletion-Type MOSFET Fundamentals

- Physical Construction & Structural Anatomy: Substrate, n^+/p^+ wells, physical channel, and dielectric SiO_2 insulation.
- Circuit Symbols & Terminal Identification: Depletion-mode schematic symbols for N-channel and P-channel D-MOSFETs.
- Depletion-Mode Operation ($V_{GS} < 0$V for N-Channel): Electrostatic repulsion of free electrons and depletion region widening.
- Enhancement-Mode Operation ($V_{GS} > 0$V for N-Channel): Accumulation of majority carriers increasing channel conductivity.
- Mathematical Formulation & Shockley's Relation: Derivation of drain current I_D and transconductance g_m across all bias zones.
- Drain and Transfer Characteristics: Graphical representation of I_D vs V_{DS} and I_D vs V_{GS} with pinch-off voltage V_P.
- Comparative Parameter Analysis: I_{DSS}, V_P, input impedance $R_{in} \approx 10^{10}$ to $10^{14}\,\Omega$, and practical circuit application limits.

Physical Construction and Internal Anatomy of N-Channel D-MOSFET

- Substrate Foundation: Formed on a lightly doped P-type silicon substrate (p-substrate) providing mechanical support and electrical isolation.
- Source & Drain Regions: Heavily doped n^+ regions diffused into the p-substrate, establishing low-resistance ohmic contacts to external terminals.
- Pre-formed Physical Channel: A narrow n-type channel physically diffused between the n^+ source and n^+ drain prior to gate oxide deposition.
- Insulating Gate Dielectric: A thin layer of Silicon Dioxide (SiO_2, thickness $t_{ox} \approx 10$ nm to 100 nm) grown on top of the channel, providing near-infinite DC isolation.
- Gate Electrode: Polysilicon or metallic aluminum deposited over the SiO_2 layer, forming a parallel-plate metal-insulator-semiconductor (MIS) capacitor.

Complementary Construction: P-Channel Depletion MOSFET

- Structural Reversal: Built on an n-type silicon substrate with heavily doped p^+ source and drain diffusion wells.
- P-Type Built-in Channel: Lightly doped p-channel physically connects the p^+ source and drain regions beneath the SiO_2 oxide layer.
- Charge Carrier Mobility: Majority carriers are holes with mobility $\mu_p \approx 450\ \text{cm}^2/(\text{V} \cdot \text{s})$, roughly 2.5 to 3 times lower than electron mobility $\mu_n \approx 1350\ \text{cm}^2/(\text{V} \cdot \text{s})$ in N-channel devices.
- Substrate Terminal (Body): Frequently connected internally to the Source terminal ($V_{BS} = 0\text{V}$) to eliminate body effect threshold shifts.
- Dual Geometry Variations: Lateral planar structures for low-power ICs vs Vertical (VMOS/DMOS) structures for high-voltage power applications.

Schematic Symbols and Terminal Identification for D-MOSFETs

- Continuous Channel Line: Represented by a solid vertical line connecting Drain (D) and Source (S), symbolizing the presence of a physically built-in channel (unlike broken line in E-MOSFETs).
- Gate Insulated Gap: The Gate (G) terminal is drawn separated from the channel line by a distinct gap, representing the non-conductive SiO_2 insulating barrier.
- Substrate/Body Arrow (N-Channel): Arrow on the Bulk (B) terminal points inward toward the *n*-channel, indicating the P-substrate to N-channel PN junction polarity.
- Substrate/Body Arrow (P-Channel): Arrow on the Bulk (B) terminal points outward from the *p*-channel toward the N-substrate.
- Three-Terminal vs Four-Terminal Symbols: Simplified 3-terminal symbols show the internal substrate-to-source connection, eliminating the separate Bulk pin.

Operational Physics at Zero Gate Bias ($V_{GS} = 0$V)

- Unimpeded Conduction Path: When $V_{GS} = 0$V, the built-in n-channel contains an abundance of free electrons provided by n-type dopant atoms.
- Drain-Source Bias ($V_{DS} > 0$V): Applying a positive voltage V_{DS} sets up an electric field along the channel, driving electron flow from Source to Drain.
- Initial Current Flow ($I_D = I_{DSS}$): At low V_{DS}, the channel behaves as an ohmic resistor ($R_{ch} = L/(q\mu_n N_D W t_{ch})$), yielding linear current rise.
- Saturated Drain Current Definition: As V_{DS} increases to the pinch-off point at $V_{GS} = 0$V, the drain current saturates at its maximum zero-bias rating, defined as I_{DSS}.
- Channel Geometry Impact: I_{DSS} is directly proportional to channel width-to-length ratio (W/L) and channel doping level N_D.

Depletion Mode Physics ($V_{GS} < 0$V for N-Channel D-MOSFET)

- Electrostatic Charge Repulsion: A negative gate voltage places negative charges on the gate plate, creating an downward electric field across the SiO_2 layer.
- Channel Electron Depletion: The electric field repels free electrons away from the n-channel into the substrate and attracts positive holes toward the oxide interface.
- Recombination & Depletion Region Formation: Free electrons recombine with attracted holes, leaving behind immobile positive donor ions (N_D^+) and effectively narrowing the conductive channel width.
- Channel Resistance Increase: The effective channel thickness t_{eff} shrinks, causing channel resistance R_{ch} to increase significantly and reducing drain current $I_D < I_{DSS}$.
- Pinch-Off Voltage (V_P or $V_{GS(off)}$): When V_{GS} reaches a sufficiently negative value V_P (e.g., -4V), the channel is completely depleted of mobile carriers, reducing drain current to zero ($I_D = 0$ A).

Enhancement Mode Physics ($V_{GS} > 0$V for N-Channel D-MOSFET)

- Electrostatic Carrier Attraction: Applying a positive voltage to the gate plate creates an upward electric field pointing toward the SiO_2 layer.
- Accumulation of Majority Carriers: The positive gate voltage attracts additional free electrons from the p-substrate into the n-channel.
- Channel Conductivity Enhancement: Extra electron density increases free carrier concentration above the thermal equilibrium doping density N_D.
- Drain Current Overdrive ($I_D > I_{DSS}$): Total channel resistance drops below its zero-bias value, allowing drain current to exceed the nominal I_{DSS} rating.
- Dielectric Voltage Limit: Gate voltage must remain below dielectric breakdown threshold ($V_{GS(max)} \approx \pm 20$V) to prevent permanent gate oxide puncture.

Mathematical Governing Equations Across Depletion & Enhancement Regimes

- Shockley's Drain Current Equation: The drain current in saturation ($V_{DS} \geq V_{GS} - V_P$) is governed by: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- Depletion Mode Bounds: For $V_P \leq V_{GS} \leq 0\text{V}$, I_D decreases quadratically from I_{DSS} down to 0 A.
- Enhancement Mode Bounds: For $V_{GS} > 0\text{V}$, the ratio $(1 - V_{GS}/V_P)$ becomes greater than 1 (since $V_P < 0$), causing $I_D > I_{DSS}$.
- Transconductance Derivation (g_m): $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$
- Maximum Transconductance at Zero Bias: $g_{m0} = \frac{2I_{DSS}}{|V_P|}$, which increases further under positive enhancement bias.

Drain Output Characteristics Curve Analysis

- Ohmic / Linear Region ($V_{DS} < V_{DS(sat)}$): For low drain voltages, I_D rises linearly with V_{DS}; device acts as a gate-controlled variable resistor.
- Pinch-Off Boundary Condition: Saturation onset occurs when $V_{DS} = V_{DS(sat)} = V_{GS} - V_P$.
- Saturation Region ($V_{DS} \geq V_{GS} - V_P$): Drain current flattens to a horizontal line governed by Shockley's equation, nearly independent of V_{DS}.
- Family of Curves: Plotted for negative V_{GS} (depletion curves below I_{DSS}), $V_{GS} = 0$V (I_{DSS} curve), and positive V_{GS} (enhancement curves above I_{DSS}).
- Avalanche Breakdown Region: At excessive $V_{DS} > V_{BR}$, impact ionization in the drain depletion region causes catastrophic current runaway.

Transfer Characteristic Curve and Parabolic Response

- Parabolic Plot: Plots I_D on the vertical axis against V_{GS} on the horizontal axis for a fixed saturation voltage V_{DS}.
- Y-Axis Intercept: Located at $V_{GS} = 0$V, where $I_D = I_{DSS}$.
- X-Axis Intercept (Left Side): Located at $V_{GS} = V_P$ (negative for N-channel), where $I_D = 0$ A.
- Right-Hand Extension: Extends into the positive V_{GS} quadrant (enhancement region), following the continuation of the parabolic curve.
- Tangent Slope = Transconductance: The local slope of the transfer curve at any operating point equals the transconductance $g_m = \Delta I_D / \Delta V_{GS}$.

Numerical Analysis of Depletion-Type MOSFET Circuit

- Device Specifications: Given an N-channel D-MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$V.
- Case 1 (Depletion Mode, $V_{GS} = -2$V): $I_D = 10 \text{ mA} \times \left(1 - \frac{-2}{-4}\right)^2 = 10 \text{ mA} \times (0.5)^2 = 2.5 \text{ mA}$.
- Case 2 (Zero Bias, $V_{GS} = 0$V): $I_D = 10 \text{ mA} \times (1 - 0)^2 = 10 \text{ mA} = I_{DSS}$.
- Case 3 (Enhancement Mode, $V_{GS} = +1$V):
  $I_D = 10 \text{ mA} \times \left(1 - \frac{+1}{-4}\right)^2 = 10 \text{ mA} \times (1.25)^2 = 15.625 \text{ mA}$.
- Transconductance Calculation at $V_{GS} = +1$V: $g_{m0} = \frac{2 \times 10 \text{ mA}}{4\text{V}} = 5 \text{ mS}$;
  $g_m = 5 \text{ mS} \times (1.25) = 6.25 \text{ mS}$.

Circuit Applications and Biasing Configurations of D-MOSFETs

- Zero-Bias Configuration: Operating at $V_{GS} = 0\text{V}$ by grounding the gate (R_G to ground) and tying source directly to ground ($R_S = 0\,\Omega$). Sets Q-point directly at $I_D = I_{DSS}$.
- Constant Current Source: Connecting gate directly to source ($V_{GS} = 0\text{V}$) creates a two-terminal constant current regulator supplying I_{DSS} regardless of supply voltage fluctuations.
- High Input Impedance Buffers: Ultra-high DC input resistance ($R_{in} > 10^{12}\,\Omega$) prevents loading of high-impedance signal sources like piezoelectric transducers.
- Automatic Gain Control (AGC) Stages: Gate-controlled transconductance variation allows linear gain adjustment in RF/IF amplifiers without detuning resonant tanks.
- Voltage Controlled Resistors (VCR): In the ohmic region, small signal channel resistance is modulated by V_{GS} according to $r_{DS} \approx \frac{|V_P|}{2I_{DSS}(1-V_{GS}/V_P)}$.

Summary of Depletion-Type MOSFET Properties

- Physical Construction: Built with a physically existing channel and dielectric SiO_2 gate insulation.
- Dual Mode Capability: Operates in Depletion Mode (V_{GS} opposes channel charge) and Enhancement Mode (V_{GS} aids channel charge).
- Shockley's Relationship: Governed by $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ across both operational modes.
- Key Electrical Ratings: High input resistance ($R_{in} \sim 10^{12}\,\Omega$), zero static gate current ($I_G \approx 0$), I_{DSS} zero-bias current, and V_P pinch-off voltage.
- Primary Advantages: Zero-bias circuit simplicity, dual-polarity flexibility, and extreme input isolation.