Lecture 5: Depletion type MOSFET

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: D-MOSFET Physical Construction, Dual-Mode Dynamics, and Parameters

- Physical Architecture: Substrate foundation, n^+ wells, pre-formed physical channel, and dielectric SiO_2 layer.
- Schematic Symbols: Continuous channel line vs isolated gate representation for N-channel and P-channel D-MOSFETs.
- Zero-Bias Conduction ($V_{GS} = 0$V): Maximum uncontrolled channel current I_{DSS} and non-pinched channel conduction.
- Depletion-Mode Operation ($V_{GS} < 0$V for N-Channel): Electrostatic electron repulsion, channel constriction, and pinch-off voltage V_P.
- Enhancement-Mode Operation ($V_{GS} > 0$V for N-Channel): Carrier accumulation, channel conductivity enhancement, and $I_D > I_{DSS}$.
- Mathematical Formulation: Application of Shockley's square-law equation across negative and positive gate bias zones.
- Drain (I_D vs V_{DS}) & Transfer (I_D vs V_{GS}) Curves: Graphical boundaries, Ohmic region, saturation, and breakdown.
- Comparative Parameter Analysis: Input impedance $R_{in} \geq 10^{14}\,\Omega$, g_m derivation, and practical circuit applications.

Physical Construction and Internal Anatomy of N-Channel D-MOSFET

- Substrate Foundation: Formed on a lightly-doped P-type silicon substrate (p-substrate) providing structural support and electrical isolation.
- Source & Drain Diffusion Wells: Heavily-doped n^+ regions ($N_D \approx 10^{19}$ cm^{-3}) diffused into the substrate forming low-resistance ohmic contacts.
- Pre-formed Physical Channel: A narrow N-type channel is physically diffused between the n^+ Source and Drain wells prior to gate oxide deposition.
- Insulating Gate Dielectric: A thin layer of Silicon Dioxide (SiO_2, thickness $t_{ox} \approx 10$ nm $- 50$ nm) grown directly over the channel region.
- Gate Electrode: Polysilicon or metallic aluminum deposited on top of the SiO_2 layer, forming a parallel-plate metal-insulator-semiconductor capacitor.
- Substrate (Body) Terminal: Connected internally to Source ($V_{BS} = 0$V) or brought out as a fourth terminal.

Schematic Symbols and Terminal Identification for D-MOSFETs

- Continuous Channel Line: Represented by a solid vertical line connecting Drain (D) and Source (S), symbolizing a physically built-in channel (unlike the broken line in E-MOSFETs).
- Insulated Gate Gap: The Gate (G) terminal is drawn separated from the channel line by a distinct dielectric gap, representing the non-conductive SiO_2 insulating barrier.
- Substrate/Body Arrow (N-Channel): Arrow on the Bulk (B) terminal points inward toward the N-channel, indicating the P-substrate to N-channel PN junction polarity.
- Substrate/Body Arrow (P-Channel): Arrow on the Bulk (B) terminal points outward from the P-channel toward the N-substrate.
- Three-Terminal vs Four-Terminal Conventions: Simplified 3-terminal symbols show the internal substrate-to-source connection, eliminating the separate Bulk pin.

Zero-Bias Equilibrium Operation ($V_{GS} = 0$V)

- Unbiased Channel State: With $V_{GS} = 0$V, the physical N-channel retains its initial fabrication width and free electron concentration.
- Drain Current Conduction: Applying $V_{DS} > 0$V causes free electrons to drift from Source to Drain through the built-in channel.
- Definition of I_{DSS}: The saturated drain current flowing through the device at $V_{GS} = 0$V is designated as I_{DSS} (Drain-to-Source Current at Shorted Gate).
- Comparison with JFET and E-MOSFET:
- • JFET: $I_D = I_{DSS}$ at $V_{GS} = 0$V (Gate cannot be forward-biased $> +0.7$V).
- • E-MOSFET: $I_D = 0$ A at $V_{GS} = 0$V (Requires $V_{GS} > V_{th}$ to conduct).
- • D-MOSFET: $I_D = I_{DSS}$ at $V_{GS} = 0$V (Gate can be biased both negatively AND positively!).

Depletion-Mode Operation ($V_{GS} < 0$V for N-Channel)

- Electrostatic Repulsion Mechanics: Applying negative voltage to the Gate ($V_{GS} < 0$V) deposits negative charge on the gate electrode.
- Depletion Layer Formation: Negative gate charge repels free electrons out of the N-channel into the substrate, uncovering positive donor ions (N_D^+).
- Channel Constriction: Repulsion of free electrons widens the depletion region into the channel, reducing effective cross-sectional conducting area.
- Current Reduction: Channel resistance increases, causing drain current I_D to drop below I_{DSS} ($I_D < I_{DSS}$).
- Pinch-Off Cutoff Voltage (V_P): As V_{GS} becomes increasingly negative, reaching $V_{GS} = V_P$ (e.g., -4V), the channel is completely depleted of free electrons, cutting off drain current ($I_D = 0$ A).

Enhancement-Mode Operation ($V_{GS} > 0$V for N-Channel)

- Electrostatic Accumulation Mechanics: Applying positive voltage to the Gate ($V_{GS} > 0$V) deposits positive charge on the gate electrode.
- Carrier Attraction: Positive gate charge attracts additional free electrons from the P-substrate into the physical N-channel.
- Channel Conductivity Enhancement: The concentration of mobile electrons in the channel rises above the initial donor doping concentration ($n > N_D$).
- Current Expansion: Effective channel resistance decreases, causing drain current I_D to increase significantly above I_{DSS} ($I_D > I_{DSS}$).
- No Gate Breakdown Risk: Oxide insulator SiO_2 prevents gate current from flowing ($I_G = 0$ A), even under large positive gate bias (up to oxide breakdown limits).

Unified Shockley Equation Modeling Across Dual Modes

- Mathematical Equation: In the saturation region ($V_{DS} \geq V_{GS} - V_P$), drain current across BOTH depletion and enhancement modes is governed by Shockley's Square Law:
- $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
- Depletion Region Bounds ($V_P \leq V_{GS} \leq 0\text{V}$): Term $\left(1 - \frac{V_{GS}}{V_P}\right) < 1$, resulting in $I_D < I_{DSS}$.
- Enhancement Region Bounds ($V_{GS} > 0\text{V}$): Term $\left(1 - \frac{V_{GS}}{V_P}\right) > 1$ (since V_P is negative), resulting in $I_D > I_{DSS}$.
- Transconductance Expression: $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$.
- Transconductance Enhancement: In enhancement mode ($V_{GS} > 0$), transconductance g_m exceeds zero-bias transconductance g_{m0} ($g_m > g_{m0}$).

Complete Output Drain Characteristics (I_D vs V_{DS})

- Ohmic / Linear Region ($V_{DS} < V_{GS} - V_P$): Linear slope where channel acts as voltage-controlled resistor; slope increases with positive V_{GS}.
- Pinch-Off Saturation Boundary ($V_{DS,sat} = V_{GS} - V_P$): Parabolic boundary separating linear region from saturated constant-current region.
- Saturation Region ($V_{DS} \geq V_{GS} - V_P$): Curves flatten into constant current plateaus corresponding to $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
- Family of Curves Profile:
- • Top Curves ($V_{GS} > 0$V): Enhancement mode operation ($I_D > I_{DSS}$).
- • Middle Curve ($V_{GS} = 0$V): Baseline zero-bias curve ($I_D = I_{DSS}$).
- • Bottom Curves ($V_P < V_{GS} < 0$V): Depletion mode operation ($I_D < I_{DSS}$).
- • Axis Cutoff ($V_{GS} = V_P$): Flat horizontal line along x-axis ($I_D = 0$ A).

Complete Transfer Characteristic (I_D vs V_{GS})

- Continuous Parabolic Curve: A unbroken parabolic arc extending continuously across the y-axis ($V_{GS} = 0\text{V}$).
- Left-Hand Side ($V_P \leq V_{GS} \leq 0\text{V}$): Depletion region where I_D decreases quadratically from I_{DSS} down to zero at $V_{GS} = V_P$.
- Right-Hand Side ($V_{GS} > 0\text{V}$): Enhancement region where I_D increases quadratically above I_{DSS} without upper theoretical bound (limited by thermal power dissipation).
- Point of Inflection (y-intercept): At $V_{GS} = 0\text{V}$, $I_D = I_{DSS}$ and curve slope equals $g_{m0} = \frac{2I_{DSS}}{|V_P|}$.
- Comparison with E-MOSFET: E-MOSFET transfer curve exists strictly for $V_{GS} > V_{th} > 0$, whereas D-MOSFET transfer curve spans negative and positive gate voltages.

Complementary Construction: P-Channel Depletion MOSFET

- Structural Reversal: Built on an N-type silicon substrate (n-sub) with heavily-doped p^+ Source and Drain diffusion wells.
- Built-in P-Channel: A physical P-type channel connects the p^+ Source and Drain regions beneath the SiO_2 oxide layer.
- Polarity Conventions: Conducts majority hole current under negative drain bias ($V_{DS} < 0$V). Pinch-off voltage V_P is POSITIVE ($V_P > 0$V).
- P-Channel Operating Regimes:
- • Depletion Mode ($V_{GS} > 0$V): Positive gate voltage repels holes, reducing channel width and $I_D < I_{DSS}$.
- • Enhancement Mode ($V_{GS} < 0$V): Negative gate voltage attracts additional holes, increasing $I_D > I_{DSS}$.
- • Cutoff State ($V_{GS} \geq V_P > 0$V): Channel completely depleted ($I_D = 0$ A).

Parameter Comparison: JFET vs D-MOSFET vs E-MOSFET

- 1. Built-in Channel Presence:
- • JFET: Yes (Physical channel exists).
- • D-MOSFET: Yes (Physical channel exists).
- • E-MOSFET: No (Induced channel only).
- 2. Gate Isolation Dielectric:
- • JFET: Reverse-biased PN junction ($R_{in} \approx 10^8 - 10^{11}\,\Omega$).
- • D-MOSFET & E-MOSFET: SiO_2 oxide insulator ($R_{in} \approx 10^{14} - 10^{15}\,\Omega$).
- 3. Allowed Gate Bias Polarities (N-Channel):
- • JFET: Negative only ($V_P \leq V_{GS} \leq 0\text{V}$).
- • D-MOSFET: Negative AND Positive ($V_P \leq V_{GS} < +\infty$).
- • E-MOSFET: Positive only ($V_{GS} \geq V_{th} > 0\text{V}$).
- 4. Mathematical Governing Equations:
- • JFET & D-MOSFET: Shockley Square Law ($I_D = I_{DSS}(1 - V_{GS}/V_P)^2$).
- • E-MOSFET: E-MOSFET Square Law ($I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2$).

Quantitative Numerical Example: D-MOSFET Dual-Mode Computations

- Problem Statement: An N-channel D-MOSFET has datasheet parameters $I_{DSS} = 10$ mA and $V_P = -4.0$V. Compute the drain current I_D and transconductance g_m for:
- (a) $V_{GS} = -2.0$V (Depletion Mode)
- (b) $V_{GS} = 0$V (Zero-Bias State)
- (c) $V_{GS} = +1.5$V (Enhancement Mode)
- 1. Calculate Zero-Bias Transconductance g_{m0}:
- $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4.0\text{V}} = 5.0\text{ mS}$$
- 2. Case (a) $V_{GS} = -2.0$V (Depletion Mode):
- $$I_D = 10\text{ mA}\left(1 - \frac{-2.0}{-4.0}\right)^2 = 10(0.5)^2 = 2.50\text{ mA}, \quad g_m = 5.0\text{ mS}(1 - 0.5) = 2.50\text{ mS}$$
- 3. Case (b) $V_{GS} = 0$V (Zero-Bias State):
- $$I_D = 10\text{ mA}\,(1 - 0)^2 = 10.0\text{ mA}, \quad g_m = g_{m0} = 5.00\text{ mS}$$
- 4. Case (c) $V_{GS} = +1.5$V (Enhancement Mode):
- $$I_D = 10\text{ mA}\left(1 - \frac{1.5}{-4.0}\right)^2 = 10\,(1 + 0.375)^2 = 10(1.375)^2 = 18.91\text{ mA}$$
- $$g_m = 5.0\text{ mS}\left(1 - \frac{1.5}{-4.0}\right) = 5.0(1.375) = 6.875\text{ mS}$$

Comprehensive Summary: D-MOSFET Dual-Mode Principles & Circuit Roles

- Physical Structure: Built-in physical channel insulated by SiO_2 dielectric, providing ultra-high input impedance ($R_{in} \geq 10^{14}\,\Omega$).
- Dual-Mode Operating Flexibility:
- 1. Depletion Mode ($V_{GS} < 0$V for N-channel): Negative gate bias repels majority carriers, constricting channel ($I_D < I_{DSS}$).
- 2. Enhancement Mode ($V_{GS} > 0$V for N-channel): Positive gate bias attracts additional carriers, enhancing channel ($I_D > I_{DSS}$).
- 3. Cutoff State ($V_{GS} \leq V_P$): Total channel depletion ($I_D = 0$ A).
- Unified Mathematical Model: Shockley's relation $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ governs both operating modes in saturation.
- Applications: Constant current sources, high-input-impedance AC amplifiers, and zero-bias self-biased stages.