Lecture 4: Metal oxide semiconductor field effect transistor(MOSFET)

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: E-MOSFET Construction, I-V Mathematical Derivation, Saturation, and Advanced Effects

- Physical Architecture: P-substrate foundation, n^+ Source/Drain diffusions, oxide dielectric SiO_2, and Gate electrode layout.
- Normally-OFF Channel Dynamics: Zero-bias isolation ($V_{GS} = 0$) and electrostatic channel induction ($V_{GS} > V_{th}$).
- Linear / Triode Region Derivation: Integral of channel charge profile $Q(x)$ yielding $I_D = k'_n \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$.
- On-Resistance ($R_{DS(on)}$) & Transconductance Parameter: Definition of $k'_n = \mu_n C_{ox}$ and aspect ratio $\frac{W}{L}$.
- Pinch-Off Mechanics & Saturation Transition: Saturation condition $V_{DS} \geq V_{GS} - V_{th}$ and square-law equation $I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{th})^2$.
- Channel Length Modulation (λ): Shortening factor ΔL, finite output resistance $r_o = \frac{1}{\lambda I_D}$, and Early voltage equivalent V_A.
- Subthreshold Conduction: Weak inversion physics, subthreshold slope S (mV/decade), and off-state power dissipation.
- P-Channel E-MOSFET (PMOS) & Numerical Problem: Complementary polarities, carrier mobility differences, and circuit calculations.

Physical Construction of N-Channel E-MOSFET

- Substrate Foundation: Built on a lightly-doped P-type silicon substrate (p-sub, $N_A \approx 10^{15}$ to 10^{16} cm^{-3}).
- Source & Drain Wells: Two heavily-doped n^+ regions ($N_D \approx 10^{19}$ cm^{-3}) diffused into the P-substrate separated by channel length L.
- Absence of Built-in Channel: No physical N-type channel exists between Source and Drain prior to external gate bias (unlike D-MOSFETs or JFETs).
- Back-to-Back Junction Isolation: At zero gate bias ($V_{GS} = 0$), applying $V_{DS} > 0$ reverse-biases the Drain-to-Substrate PN junction, ensuring $I_D = 0$ A (normally-OFF).
- Four Terminals: Source (S), Drain (D), Gate (G), and Body/Substrate (B). Body is usually tied to Source ($V_{SB} = 0$V) in single-ended discrete devices.

Channel Inversion & Electrostatic Charge Distribution ($V_{GS} > V_{th}$)

- Induced Inversion Layer: When V_{GS} exceeds threshold voltage V_{th}, positive gate charge induces a continuous N-type inversion channel connecting the n^+ Source and Drain wells.
- Channel Charge Density Formula: Mobile electron charge density per unit area at position x along the channel:
- $$Q_n(x) = -C_{ox}\left[V_{GS} - V(x) - V_{th}\right]$$
- Channel Potential Boundary Conditions: Channel potential $V(x)$ increases monotonically from $V(0) = 0\text{V}$ at the source end to $V(L) = V_{DS}$ at the drain end.
- Overdrive Voltage (V_{OV}): Defined as $V_{OV} = V_{GS} - V_{th}$ (also called effective gate voltage V_{eff}), quantifying channel strength.

Linear / Triode Region Physics ($V_{GS} > V_{th}, V_{DS} < V_{GS} - V_{th}$)

- Continuous Conductive Path: For small drain voltages ($V_{DS} < V_{GS} - V_{th}$), the channel remains continuous and non-pinched from Source to Drain.
- Carrier Drift Transport: Applied electric field $E_x = -\frac{dV(x)}{dx}$ causes mobile electrons to drift from Source to Drain.
- Differential Current Equation: Local drift current passing position x across channel width W:
- $$I_D = -W \cdot v_d(x) \cdot Q_n(x) = W\mu_n C_{ox} \left[V_{GS} - V(x) - V_{th}\right] \frac{dV(x)}{dx}$$
- Current Uniformity Constraint: By continuity of current under steady-state conditions, I_D is constant at every cross-section x along the channel length L.

Mathematical Derivation of Linear Region Drain Current Equation

- Integration Across Channel Length: Integrating $I_D dx = W\mu_n C_{ox}\left[V_{GS} - V(x) - V_{th}\right] dV$ from $x = 0$ ($V = 0$) to $x = L$ ($V = V_{DS}$):
- $$I_D \int_0^L dx = W\mu_n C_{ox} \int_0^{V_{DS}} \left[(V_{GS} - V_{th}) - V(x)\right] dV$$
- Integral Evaluation: $I_D \cdot L = W\mu_n C_{ox}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$.
- Final Linear Region I-V Expression:
- $$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] = k_n'\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$
- Process Transconductance Parameter: $k_n' = \mu_n C_{ox}$ ($\mathrm{A/V^2}$); Device Conduction Factor $k_n = k_n'\frac{W}{L}$.

Small-Signal On-Resistance ($R_{DS(on)}$) in Linear Region

- Small V_{DS} Approximation: When $V_{DS} \ll 2(V_{GS} - V_{th})$, the $V_{DS}^2/2$ term in the linear current formula is negligible:
- $$I_D \approx k_n' \frac{W}{L}(V_{GS} - V_{th})V_{DS}$$
- Channel Resistance Derivation: Inverse slope of $I_D - V_{DS}$ curve at the origin:
- $$R_{DS(on)} = \frac{V_{DS}}{I_D} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{k_n(V_{GS} - V_{th})}$$
- Voltage-Controlled Resistor Application: $R_{DS(on)}$ can be tuned dynamically across orders of magnitude by varying gate bias V_{GS}.
- Power MOSFET Minimization: In power electronics, maximizing aspect ratio W/L achieves sub-milliohm $R_{DS(on)}$ (< 1 mΩ), minimizing conduction losses.

Channel Pinch-Off & Transition to Saturation Region ($V_{DS} \geq V_{GS} - V_{th}$)

- Pinch-Off Point Location: As V_{DS} is increased, the channel voltage near the drain $V(L) = V_{DS}$ increases, reducing local gate-to-channel drop $V_{GS} - V_{DS}$.
- Saturation Voltage Criterion: When V_{DS} reaches $V_{DS,sat} = V_{GS} - V_{th}$, local gate voltage drop at the drain end equals V_{th}, reducing inversion charge $Q_n(L)$ to zero.
- Pinch-Off Shape: The inversion layer tapers down to zero thickness at $x = L$. Electrons arriving at the pinch-off boundary are swept across the depletion region by the high lateral electric field.
- Current Saturation Mechanism: Further increases in $V_{DS} > V_{DS,sat}$ do not increase channel charge or current; the excess voltage ($V_{DS} - V_{DS,sat}$) drops across the pinched depletion gap.

Saturation Region Current Formula: Square-Law Characteristic

- Derivation from Linear Equation: Substituting $V_{DS} = V_{DS,sat} = V_{GS} - V_{th}$ into the linear current equation:
- $$I_{D,sat} = k'_n \frac{W}{L} \left[(V_{GS} - V_{th})(V_{GS} - V_{th}) - \frac{(V_{GS} - V_{th})^2}{2} \right]$$
- Square-Law Saturation Equation:
- $$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{th})^2$$
- Characteristics of Ideal Saturation:
- 1. Drain current is strictly independent of drain-source voltage V_{DS}.
- 2. Quadratic (square-law) dependence on gate overdrive voltage $(V_{GS} - V_{th})$.
- 3. Transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}} = k'_n \frac{W}{L} (V_{GS} - V_{th}) = \sqrt{2 k'_n \frac{W}{L} I_D}$.

Channel Length Modulation (λ) & Finite Output Resistance (r_o)

- Physical Mechanism: In saturation, increasing $V_{DS} > V_{DS,sat}$ causes the pinch-off point to move inward toward the source by distance ΔL, shortening active channel length to $L' = L - \Delta L$.
- Modified Saturation Current Equation incorporating λ:
- $$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$
- Channel Length Modulation Parameter (λ): Inverse of Early voltage equivalent V_A ($\lambda = \frac{1}{V_A}$), inversely proportional to channel length L ($\lambda \propto \frac{1}{L}$).
- Small-Signal Output Resistance Formula:
- $$r_o = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{V_{GS}} = \frac{1}{\lambda I_{D0}} \approx \frac{V_A}{I_D}$$
- Design Trade-off: Longer channel lengths L reduce λ and increase output resistance r_o, enhancing amplifier intrinsic gain $A_{v0} = g_m r_o$.

Subthreshold Conduction & Weak Inversion Region ($V_{GS} < V_{th}$)

- Subthreshold Current Existence: For $V_{GS} < V_{th}$, surface channel is not in strong inversion, but minority electron concentration is non-zero (weak inversion regime).
- Exponential Current Equation: Transport is dominated by diffusion (rather than drift), yielding exponential dependence on V_{GS}:
- $$I_D \approx I_{D0} \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)\left(1 - e^{-\frac{V_{DS}}{V_T}}\right)$$

  (where subthreshold factor $n = 1 + \frac{C_{dep}}{C_{ox}} \approx 1.1$ to 1.5).
- Subthreshold Swing (S): Gate voltage change required to change subthreshold drain current by one decade (factor of 10):
- $$S = nV_T \ln(10) = n\left(2.303\frac{kT}{q}\right) \approx 60 \text{ mV/decade} \times n$$

- Theoretical Room-Temperature Limit: Ideal $S_{min} \approx 60$ mV/decade at $T = 300$K. Practical MOSFETs achieve 70 to 90 mV/decade.
- Impact on Digital CMOS: Finite subthreshold slope causes off-state leakage current (I_{off}), driving static standby power dissipation in ultra-dense ICs.

Complementary P-Channel E-MOSFET (PMOS) Characteristics

- Physical Structure: Built on an N-type silicon substrate (n-sub) with heavily-doped p^+ Source and Drain diffusion wells.
- Voltage & Current Polarities: Conducts when $V_{GS} < V_{thp} < 0\text{V}$ and $V_{DS} < 0\text{V}$; current flows from Source to Drain ($I_D < 0$ A by standard convention).
- PMOS Saturation Current Equation:
- $$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{thp})^2 = \frac{1}{2}k'_p\frac{W}{L}(V_{SG} - |V_{thp}|)^2$$
- Mobility Ratio Disparity: Electron mobility $\mu_n \approx 2.5 \times \mu_p$ hole mobility in silicon.
- CMOS Sizing Rule: To achieve symmetric pull-up and pull-down drive currents ($I_{D,n} = I_{D,p}$), PMOS width must be designed approximately 2.5 times larger than NMOS width: $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$.

Comprehensive Numerical Problem: E-MOSFET Bias & Operating State Analysis

- Problem Statement: An N-channel E-MOSFET has process parameters $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{th} = 0.8\text{V}$, aspect ratio $\frac{W}{L} = 20$, and channel length modulation $\lambda = 0.02\ \text{V}^{-1}$. The device is biased with $V_{GS} = 2.0\text{V}$.
- 1. Determine Process Transconductance k_n and Overdrive Voltage V_{OV}:
- $$k_n = k_n' \frac{W}{L} = (100\,\mu\text{A/V}^2)(20) = 2.0\ \text{mA/V}^2, \quad V_{OV} = V_{GS} - V_{th} = 2.0 - 0.8 = 1.2\text{V}$$
- 2. Calculate Saturation Transition Voltage $V_{DS,sat}$:
- $$V_{DS,sat} = V_{GS} - V_{th} = 1.2\text{V}$$
- 3. Evaluate Drain Current I_D for $V_{DS} = 0.5\text{V}$ (Linear Region, $V_{DS} < V_{DS,sat}$):
- $$I_D = (2.0\ \text{mA/V}^2)\left[(1.2)(0.5) - \frac{(0.5)^2}{2}\right] = 2.0\,[0.60 - 0.125] = 2.0 \times 0.475 = 0.95\ \text{mA}$$
- 4. Evaluate Drain Current I_D and Output Resistance r_o for $V_{DS} = 3.0\text{V}$ (Saturation Region, $V_{DS} > V_{DS,sat}$):
- $$I_D = \frac{1}{2}(2.0\ \text{mA/V}^2)(1.2)^2\,(1 + 0.02 \times 3.0) = 1.0 \times 1.44 \times 1.06 = 1.526\ \text{mA}$$
- $$r_o \approx \frac{1}{\lambda I_{D0}} = \frac{1}{(0.02\ \text{V}^{-1})(1.44\ \text{mA})} = \frac{1}{0.0288\ \text{mS}} = 34.72\ \text{k}\Omega$$

Comprehensive Summary: E-MOSFET Operating Regimes, Equations & Characteristics

- E-MOSFET Operational Regimes Summary:
- 1. Cutoff Region ($V_{GS} < V_{th}$): $I_D \approx 0$ (weak inversion subthreshold leakage governed by $S \approx 70 - 90$ mV/dec).
- 2. Linear / Triode Region ($V_{GS} > V_{th}, V_{DS} < V_{GS} - V_{th}$):
- $$I_D = k_n' \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right], \quad R_{DS(on)} = \frac{1}{k_n' \frac{W}{L} (V_{GS} - V_{th})}$$
- 3. Saturation Region ($V_{GS} > V_{th}, V_{DS} \geq V_{GS} - V_{th}$):
- $$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}), \quad g_m = \sqrt{2 k_n' \frac{W}{L} I_D}, \quad r_o = \frac{1}{\lambda I_D}$$
- CMOS Sizing: PMOS width $(W/L)_p \approx 2.5 \times (W/L)_n$ compensates for hole mobility reduction.