Lecture 3: Metal oxide semiconductor field effect transistor(MOSFET)

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: MOS Structural Physics, Energy Band Diagrams, and Threshold Derivation

- MOS Structure Architecture: Stack layout, material parameters ($\varepsilon_{ox}, \varepsilon_s$), and oxide thickness t_{ox}.
- Oxide Capacitance & Electrostatics: Formula for unit-area oxide capacitance $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ and total gate charge.
- Flat-Band Condition ($V_G = V_{FB}$): Work function difference Φ_{ms}, fixed oxide charges Q_{ox}, and zero band bending.
- Accumulation Operating Regime ($V_G < V_{FB}$ for P-substrate): Surface hole accumulation and energy band bending upwards.
- Depletion Operating Regime ($V_{FB} < V_G < V_{th}$): Uncovering acceptor ions, depletion width W_{dep}, and downward band bending.
- Strong Inversion Regime ($V_G \geq V_{th}$): Surface inversion criteria $\phi_s = 2\phi_F$, minority carrier channel formation.
- Threshold Voltage (V_{th}) Closed-Form Derivation: Summing flat-band, surface potential, and bulk depletion charge terms.
- Substrate Bias / Body Effect: Impact of $V_{SB} > 0$V on depletion width and threshold voltage shift ΔV_{th}.

The Two-Terminal MOS Structure & Material Dielectric Constants

- Physical Stack Composition: Heavily-doped n^+ polysilicon (or metal) Gate electrode, amorphous Silicon Dioxide (SiO_2) gate dielectric, and P-type monocrystalline silicon substrate (p-sub).
- Gate Oxide Dielectric Properties: Silicon Dioxide relative permittivity $\varepsilon_{r,ox} = 3.9$, oxide permittivity $\varepsilon_{ox} = \varepsilon_{r,ox}\varepsilon_0 \approx 3.45 \times 10^{-13}$ F/cm.
- Silicon Semiconductor Properties: Silicon relative permittivity $\varepsilon_{r,Si} = 11.7$, semiconductor permittivity $\varepsilon_s = \varepsilon_{r,Si}\varepsilon_0 \approx 1.04 \times 10^{-12}$ F/cm.
- Insulation Superiority: SiO_2 energy bandgap $E_g \approx 9.0$ eV provides near-infinite DC resistivity ($> 10^{16}\,\Omega \cdot$ cm), preventing gate leakage current.
- Scaling Trend: Oxide thickness t_{ox} has scaled down from 100 nm in legacy nodes to < 1.5 nm in sub-micron technologies (where high-k metal gates replace SiO_2).

Oxide Electrostatics & Unit-Area Capacitance (C_{ox})

- Unit-Area Oxide Capacitance Formula: Defined as oxide permittivity divided by gate dielectric thickness t_{ox}:
- $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-13}\ \text{F/cm}}{t_{ox}\ (\text{cm})}$$
- Numerical Significance: For $t_{ox} = 10\ \text{nm} = 10^{-6}\ \text{cm}$, $C_{ox} = \frac{3.45 \times 10^{-13}}{10^{-6}} = 3.45 \times 10^{-7}\ \text{F/cm}^2 = 3.45\ \text{fF}/\mu\text{m}^2$.
- Total Gate Capacitance: $C_G = C_{ox} \cdot W \cdot L$, where W is channel width and L is channel length.
- Charge-Voltage Storage Law: Induced gate charge per unit area $Q_G = C_{ox}(V_G - V_{FB} - \phi_s)$, where ϕ_s is semiconductor surface potential.

Flat-Band Condition ($V_G = V_{FB}$) & Work Function Differences

- Ideal MOS Assumption: If metal work function Φ_m matched semiconductor work function Φ_s, zero gate bias ($V_G = 0$) would yield flat energy bands.
- Real Work Function Difference (Φ_{ms}): Difference between gate Fermi level and substrate Fermi level: $\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} + \phi_F\right)$.
- Fermi Potential Formula (P-Substrate): $\phi_F = V_T \ln\left(\frac{N_A}{n_i}\right)$, where $V_T = \frac{kT}{q} \approx 0.0259\text{V}$ at room temperature.
- Fixed Oxide Charge (Q_{ox}): Parasitic positive charges trapped near the $SiO_2 - Si$ interface shift band bending.
- Flat-Band Voltage Formula: The gate voltage required to restore zero band bending across the semiconductor substrate:
- $$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

Accumulation Operating Regime ($V_G < V_{FB}$ for P-Substrate)

- Applied Gate Voltage Condition: Gate is biased negatively relative to flat-band voltage ($V_G < V_{FB}$).
- Electrostatic Field Orientation: Negative charge on gate electrode attracts positive majority carriers (holes) toward the $SiO_2 - Si$ interface.
- Energy Band Behavior: Conduction band E_c, valence band E_v, and intrinsic Fermi level E_i bend upward near the oxide interface.
- Surface Hole Concentration: $p_s = N_A e^{\frac{-q\phi_s}{kT}} > N_A$ (since surface potential $\phi_s < 0$).
- Capacitance State: System acts as a pure parallel-plate capacitor with high capacitance equal to C_{ox} because hole accumulation layer touches the oxide interface.

Depletion Operating Regime ($V_{FB} < V_G < V_{th}$)

- Applied Gate Voltage Condition: Gate potential is increased above flat-band voltage but remains below threshold voltage.
- Majority Carrier Repulsion: Positive gate charge repels mobile holes away from the $SiO_2 - Si$ interface into the bulk substrate.
- Uncovered Acceptor Ions: Leaves behind a space-charge depletion region composed of fixed, negatively charged acceptor ions (N_A^-).
- Depletion Width Formula: Space-charge layer width increases with surface potential $\phi_s > 0$:
- $$W_{dep} = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_A}}$$
- Energy Band Behavior: Bands bend downward near the interface; E_i moves closer to the Fermi level E_F at the surface.

Strong Inversion Regime & Threshold Criteria ($\phi_s = 2\phi_F$)

- Onset of Inversion: As V_G increases further, surface potential ϕ_s increases until intrinsic level E_i crosses below Fermi level E_F at the surface.
- Strong Inversion Definition: Reached when electron concentration at the surface (n_s) equals original hole concentration in the bulk substrate (N_A).
- Surface Potential Criterion for Strong Inversion: Surface potential must reach exactly twice the bulk Fermi potential:
- $$\phi_{s,\text{inv}} = 2\phi_F = 2V_T \ln\left(\frac{N_A}{n_i}\right)$$
- Inversion Conducting Channel: Mobile minority electrons aggregate in an extremely thin surface inversion layer ($t_{inv} \approx 2$ to 5 nm), forming an N-channel.
- Maximum Depletion Layer Width (W_{max}): Once strong inversion occurs, further gate voltage increase adds mobile channel electrons rather than expanding depletion width:
- $$W_{max} = \sqrt{\frac{2\varepsilon_s(2\phi_F)}{qN_A}}$$

Mathematical Derivation of Threshold Voltage (V_{th})

- Charge Balance Conservation Equation: Total applied gate voltage equals flat-band voltage plus surface potential drop plus voltage drop across gate oxide:

$$V_{th} = V_{FB} + \phi_{s,\text{inv}} + V_{ox} = V_{FB} + 2\phi_F + \frac{|Q_{dep}|}{C_{ox}}$$

- Bulk Depletion Charge at Inversion: Charge per unit area of unshielded acceptor ions at W_{max}:

$$|Q_{dep}| = qN_A W_{max} = \sqrt{2\varepsilon_s qN_A(2\phi_F)}$$

- Complete Threshold Voltage Formula (P-Substrate, N-Channel):

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s qN_A(2\phi_F)}}{C_{ox}}$$

- Physical Control Knobs: V_{th} can be engineered via substrate doping N_A, gate oxide thickness t_{ox} (via C_{ox}), gate work function Φ_m, and threshold adjust ion implantation.

Substrate Bias / Body Effect Physics & Shift (ΔV_{th})

- Body Terminal Bias (V_{SB}): When Source and Body (Substrate) terminals are not at equal potential, applying reverse body bias ($V_{SB} > 0$V) increases reverse potential across the substrate-channel junction.
- Depletion Region Expansion: Effective potential across bulk depletion region becomes $(2\phi_F + V_{SB})$, increasing depletion charge to $|Q_{dep}| = \sqrt{2\varepsilon_s q N_A (2\phi_F + V_{SB})}$.
- Body Effect Parameter (γ): Defined as $\gamma = \frac{\sqrt{2\varepsilon_s q N_A}}{C_{ox}}$ (units of $V^{1/2}$).
- Modified Threshold Voltage Equation with Body Effect:
- $$V_{th} = V_{th0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$
- Practical Consequence: Reverse body bias ($V_{SB} > 0$) increases threshold voltage V_{th}, reducing drive current in stacked transistor topologies (e.g., cascode amplifiers, NAND logic gates).

Oxide Charges & Interface Trapped Charge Classification

- 1. Fixed Oxide Charge (Q_f): Stable positive ionic charge located within 2 nm of the $SiO_2 - Si$ transition layer, determined by oxidation thermal profile.
- 2. Mobile Ionic Charge (Q_m): Alkali metal contaminants (e.g., Na^+, K^+) that drift through oxide under electric fields, causing threshold instability.
- 3. Interface Trapped Charge (Q_{it}): Dangling silicon bonds at the interface creating energy traps within forbidden bandgap, reduced by hydrogen anneal.
- 4. Oxide Trapped Charge (Q_{ot}): Holes or electrons trapped in bulk oxide caused by ionizing radiation or hot carrier injection.
- Combined Threshold Voltage Offset: Total parasitic charge $Q_{ox} = Q_f + Q_m + Q_{it} + Q_{ot}$ shifts threshold voltage by $\Delta V_{th} = -\frac{Q_{ox}}{C_{ox}}$.

Architectural Structural Differences: JFET vs MOSFET Comparison

- Gate Isolation Mechanism: JFET relies on reverse-biased PN junction (susceptible to forward breakdown if $V_{GS} > 0.7$V), whereas MOSFET relies on solid oxide insulator SiO_2.
- DC Gate Input Current: JFET $I_G \approx 10^{-9}$ to 10^{-12} A; MOSFET $I_G \approx 10^{-14}$ to 10^{-15} A (femtoamperes).
- Operational Flexibility: JFET operates strictly in depletion mode; MOSFET can be designed for either Depletion-Mode or Enhancement-Mode (normally-OFF).
- Electrostatic Discharge (ESD) Sensitivity: Thin MOSFET gate oxide ($t_{ox} < 10$ nm) is vulnerable to dielectric breakdown from static voltage spikes (> 15V), requiring internal ESD protection diodes.

Quantitative Example: MOS Electrostatics & Threshold Calculation

- Problem Statement: Consider an N-channel MOS structure on a P-type silicon substrate with doping $N_A = 10^{16}$ cm^{-3}, gate oxide thickness $t_{ox} = 15$ nm, flat-band voltage $V_{FB} = -0.85$V, and intrinsic concentration $n_i = 1.5 \times 10^{10}$ cm^{-3}.
- 1. Calculate Unit-Area Oxide Capacitance C_{ox}:
- $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-13}\ \text{F/cm}}{15 \times 10^{-7}\ \text{cm}} = 2.30 \times 10^{-7}\ \text{F/cm}^2 = 0.230\mu\text{F/cm}^2$$
- 2. Compute Substrate Fermi Potential ϕ_F:
- $$\phi_F = (0.0259\text{V}) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.0259 \times 13.41 = 0.347\text{V}$$
- 3. Calculate Maximum Depletion Width W_{max} at Inversion ($2\phi_F = 0.694$V):
- $$W_{max} = \sqrt{\frac{2(1.04 \times 10^{-12})(0.694)}{(1.6 \times 10^{-19})(10^{16})}} = \sqrt{9.022 \times 10^{-10}} = 3.003 \times 10^{-5}\ \text{cm} = 0.300\mu\text{m}$$
- 4. Calculate Bulk Depletion Charge $|Q_{dep}|$ and Threshold Voltage V_{th0}:
- $$|Q_{dep}| = qN_A W_{max} = (1.6 \times 10^{-19})(10^{16})(3.003 \times 10^{-5}) = 4.805 \times 10^{-8}\ \text{C/cm}^2$$
- $$V_{th0} = V_{FB} + 2\phi_F + \frac{|Q_{dep}|}{C_{ox}} = -0.85 + 0.694 + \frac{4.805 \times 10^{-8}}{2.30 \times 10^{-7}} = -0.156 + 0.2089 = +0.053\text{V}$$

Comprehensive Summary: MOS Physics, Energy Bands & Inversion Physics

- MOS Electrostatic Regimes:
- • Accumulation ($V_G < V_{FB}$): Majority holes accumulate at $SiO_2 - Si$ interface.
- • Depletion ($V_{FB} < V_G < V_{th}$): Hole repulsion leaves unshielded acceptor ions (N_A^-).
- • Strong Inversion ($V_G \geq V_{th}$): Surface potential reaches $\phi_s = 2\phi_F$, creating mobile electron channel.
- Fundamental Governing Formulas:
- • Oxide Capacitance: $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.
- • Threshold Voltage: $V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_F)}}{C_{ox}}$.
- • Body Effect Shift: $V_{th} = V_{th0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$.