Lecture 2: Junction field effect transistor(JFET) parameters, small-signal models, breakdown & temperature effects

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: JFET Parameter Derivations, AC Models, and Thermal Sensitivity

- Transconductance (g_m): Definition, derivative from Shockley's equation, and V_{GS} bias dependence.
- Zero-Bias Transconductance (g_{m0}): Maximum transconductance evaluation at $V_{GS} = 0\text{V}$.
- Dynamic Drain Resistance (r_d): Definition, physical cause (channel length modulation), and output conductance (g_{os}).
- Amplification Factor (μ): Inter-relationship $\mu = g_m \cdot r_d$ and theoretical voltage gain ceiling.
- Gate Leakage & Input Impedance: Temperature-dependent reverse saturation current I_{GSS} and $R_{in} \geq 10^9\,\Omega$.
- High-Frequency Parasitics: Inter-electrode capacitances (C_{gs}, C_{gd}, C_{ds}) and Miller multiplication effect.
- Thermal Physics & Breakdown: Zero Temperature Coefficient (ZTC) point and avalanche breakdown (BV_{DGO}).
- Small-Signal Equivalent Circuit & Applied Example: AC load-line analysis and voltage gain computation.

Transconductance (g_m) Parameter Derivation & Non-linear Bias Dependence

- Definition of Transconductance: Measures the control of gate voltage over drain current at a constant drain-source bias: $g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=\text{const}}$.
- Mathematical Derivation from Shockley's Equation: Differentiating $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ with respect to V_{GS} yields:
- $$g_m = \frac{\partial}{\partial V_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right] = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$
- Linear Dependence on Gate Voltage: Unlike BJTs where $g_m = \frac{I_C}{V_T}$ scales linearly with current, JFET transconductance scales linearly with gate voltage V_{GS} (and square-root of current $\sqrt{I_D}$).
- Relation to Saturated Current: Substituting $\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_P}$ yields $g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$.

Zero-Bias Transconductance (g_{m0}) & Graphical Determination

- Maximum Transconductance (g_{m0}): Evaluated at zero gate bias ($V_{GS} = 0\text{V}$):
- $$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$
- Slope of Transfer Curve: g_{m0} represents the maximum slope of the transfer characteristic curve (I_D vs V_{GS}), occurring at the y-intercept ($V_{GS} = 0\text{V}$).
- Typical Parameter Values: For standard signal JFETs (e.g., 2N5457, 2N3819), $I_{DSS} = 2$ to 12 mA and $V_P = -2$ to -6V, yielding $g_{m0} \approx 1000$ to $6000\,\mu\text{S}$ (1 to 6 mS).
- Design Consideration: Higher I_{DSS} and sharper (smaller magnitude) V_P maximize transconductance and resulting AC voltage gain.

Dynamic Drain Resistance (r_d) & Channel Length Modulation

- Definition of Dynamic Drain Resistance: Inverse slope of the drain characteristic curve in the saturation region:
- $$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{const}} = \frac{1}{g_{os}}$$

  (where g_{os} is output admittance).
- Physical Origin: Caused by Channel Length Modulation (λ). As V_{DS} increases beyond $V_{DS,sat}$, the pinch-off point moves closer to the source, reducing effective channel length $L' = L - \Delta L$.
- Modified Current Equation: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 + \lambda V_{DS})$, where λ is the channel length modulation parameter (V^{-1}).
- Typical Values: r_d typically ranges from 10 kΩ to 500 kΩ for signal JFETs, reflecting high output impedance ideal for current sources.

Amplification Factor (μ) & Parameter Inter-relationship

- Definition of Amplification Factor (μ): Ratio of change in drain-source voltage to change in gate-source voltage required to maintain constant drain current:
- $$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D=\text{const}}$$

  (dimensionless quantity).
- Fundamental Relation Derivation: Chain rule expansion yields $\Delta I_D = \left(\frac{\partial I_D}{\partial V_{GS}}\right)\Delta V_{GS} + \left(\frac{\partial I_D}{\partial V_{DS}}\right)\Delta V_{DS} = 0$.
- $$\mu = g_m \cdot r_d$$
- Physical Significance: μ represents the maximum theoretical voltage gain achievable by the JFET in an open-circuit (infinite load resistance) common-source amplifier configuration.
- Typical Range: Standard JFET amplification factors range from $\mu = 40$ to 500.

Gate Leakage Current (I_{GSS}) & Ultra-High Input Impedance

- Reverse Leakage Origin: Gate current I_{GSS} is the reverse saturation leakage current across the reverse-biased Gate-to-Channel PN junction.
- Magnitude at Room Temperature: Typically $I_{GSS} \approx 10$ pA to 1 nA at $T = 25^{\circ}$C for silicon JFETs.
- Input DC Impedance Calculation: $R_{in(DC)} = \frac{|V_{GS}|}{I_{GSS}} \approx \frac{1\text{V}}{10\text{ pA}} = 10^{11}\,\Omega = 100\text{ G}\Omega$.
- Thermal Sensitivity of I_{GSS}: Reverse leakage doubles approximately every 10°C temperature rise:
- $$I_{GSS}(T) = I_{GSS}(25^{\circ}\text{C}) \cdot 2^{\frac{T-25}{10}}$$
- Practical Implication: At $T = 125^{\circ}$C, I_{GSS} increases by $2^{10} = 1024\times$, reducing input resistance to $\sim 100\text{ M}\Omega$.

High-Frequency Parasitic Capacitances (C_{gs}, C_{gd}, C_{ds})

- Gate-Source Junction Capacitance (C_{gs}): Depletion layer transition capacitance across the gate-source PN junction ($C_{gs} \approx 2$ to 10 pF).
- Gate-Drain Junction Capacitance (C_{gd}): Reverse-biased junction capacitance between gate and drain ($C_{gd} \approx 1$ to 5 pF).
- Drain-Source Parasitic Capacitance (C_{ds}): Geometry-dependent capacitive coupling between drain and source metal contacts ($C_{ds} \approx 0.1$ to 1 pF).
- Voltage-Dependent Capacitance: $C_{gd}(V_{GD}) = \frac{C_{gd0}}{\sqrt{1+\frac{V_{GD}}{V_{bi}}}}$, shrinking as reverse bias increases.
- Miller Effect Bandwidth Constraint: In Common-Source amplifiers, C_{gd} is multiplied by voltage gain A_v, creating equivalent input capacitance $C_{in,Miller} = C_{gs} + C_{gd}(1 + |A_v|)$.

Temperature Dependencies of JFET Parameters

- Dual Competing Thermal Effects:
- 1. Carrier Mobility Degradation: Temperature rise increases lattice scattering, reducing electron mobility $\mu_n(T) \propto T^{-3/2}$, which decreases I_{DSS} and g_m.
- 2. Built-in Potential Reduction: Barrier potential V_{bi} decreases by approximately -2.2 mV/°C, narrowing depletion regions and slightly increasing channel width.
- Dominant Effect: At typical operating current levels, mobility degradation dominates, causing I_{DSS} to possess a negative temperature coefficient (NTC).
- Thermal Runaway Immunity: Unlike BJTs whose collector current increases exponentially with temperature (V_{BE} drop), JFET drain current naturally decreases at elevated temperatures, preventing thermal runaway.

Zero Temperature Coefficient (ZTC) Operating Bias Point

- Thermal Compensation Principle: Perfect cancellation occurs when mobility drop precisely balances built-in potential barrier reduction.
- ZTC Gate Bias Condition: The required gate-source voltage for Zero Temperature Coefficient is mathematically derived as:
- $$|V_{GS,ZTC}| = |V_P| - 0.63\text{V}$$
- ZTC Drain Current Formula: Corresponding temperature-independent drain current level:
- $$I_{D,ZTC} = I_{DSS}\left(\frac{0.63\text{V}}{|V_P|}\right)^2$$
- Practical Significance: Biasing a JFET precisely at $(V_{GS,ZTC}, I_{D,ZTC})$ ensures zero drift in Q-point current across wide ambient temperature swings (-55°C to $+125^\circ$C).

JFET Electrical Breakdown Mechanisms (BV_{DGO} & BV_{DS})

- Avalanche Breakdown Location: Occurs across the reverse-biased Gate-Drain PN junction where electric field intensity is highest.
- Maximum Gate-Drain Breakdown Voltage (BV_{DGO}): Datasheet rating for avalanche breakdown between Drain and Gate with Source open-circuited.
- Composite Breakdown Condition: Avalanche occurs when total reverse voltage across the gate-drain junction exceeds BV_{DGO}:
- $$V_{DG} = V_{DS} - V_{GS} = BV_{DGO}$$
- Drain-Source Breakdown Voltage (BV_{DS}): Maximum safe V_{DS} decreases linearly with increasingly negative gate bias V_{GS}:
- $$BV_{DS} = BV_{DGO} - |V_{GS}|$$
- Destructive Avalanche Behavior: Once breakdown occurs, drain current increases exponentially, causing destructive localized dissipation if current is not limited by external circuit resistance.

Small-Signal Low-Frequency and High-Frequency AC Models

- Low-Frequency AC Equivalent Circuit: Voltage-controlled current source $g_m v_{gs}$ in parallel with output resistance r_d; gate input modeled as open-circuit ($R_{in} = \infty$).
- High-Frequency Hybrid-π Model: Incorporates C_{gs} between Gate and Source, C_{gd} between Gate and Drain, and C_{ds} between Drain and Source.
- Voltage Gain Formula (Low-Frequency Common-Source):
- $$A_v = \frac{v_o}{v_{in}} = -g_m(R_D \parallel R_L \parallel r_d)$$
- Unity-Gain Transition Frequency (f_T): Frequency at which short-circuit current gain drops to unity:
- $$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Quantitative Example: Small-Signal Parameter & AC Gain Computation

- Problem Statement: A JFET amplifier operates with $I_{DSS} = 10$ mA, $V_P = -3.5$V, $r_d = 40$ kΩ, and $BV_{DGO} = 30$V. The DC bias is set at $V_{GSQ} = -1.0$V with drain load $R_D = 4.7$ kΩ.
- 1. Calculate g_{m0} and g_m at the Q-point:
- $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{3.5\text{V}} = 5.714\text{ mS}$$
- $$g_m = g_{m0}\left(1 - \frac{-1.0}{-3.5}\right) = 5.714\,(1 - 0.2857) = 4.081\text{ mS}$$
- 2. Compute Amplification Factor μ:
- $$\mu = g_m \cdot r_d = (4.081\text{ mS})(40\text{ kΩ}) = 163.2$$
- 3. Calculate Loaded AC Voltage Gain A_v ($R_L = \infty$):
- $$A_v = -g_m(R_D \parallel r_d) = -(4.081\text{ mS})\left(\frac{4.7 \times 40}{4.7 + 40}\text{ kΩ}\right) = -(4.081)(4.205) = -17.16\text{ V/V}$$
- 4. Evaluate Maximum Safe Breakdown Voltage BV_{DS}:
- $$BV_{DS} = BV_{DGO} - |V_{GSQ}| = 30\text{V} - 1.0\text{V} = 29.0\text{V}$$

Summary of JFET Small-Signal Parameters, Thermal Properties & Limits

- Dynamic AC Parameters Matrix:
- • Transconductance: $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$ where $g_{m0} = \frac{2I_{DSS}}{|V_P|}$.
- • Dynamic Drain Resistance: $r_d = \frac{1}{\lambda I_D} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$.
- • Amplification Factor: $\mu = g_m r_d$ (intrinsic voltage gain upper bound).
- Thermal Stability: ZTC bias condition $|V_{GS,ZTC}| = |V_P| - 0.63\text{V}$ provides temperature-independent Q-point operation.
- High-Frequency & Voltage Boundaries: Miller-multiplied C_{gd} limits RF bandwidth; avalanche breakdown restricts maximum drain bias to $BV_{DS} = BV_{DGO} - |V_{GS}|$.