Lecture 1: Junction field effect transistor(JFET) structure, symbol, working, characteristics, parameters

Field Effect Transistors(FETs)

DI02011011: Electronics Circuit and Application (ECA)

Lecture Outline: JFET Fundamentals, Device Physics, and Analytical Modeling

- Transistor Classification: Comparison between Bipolar Junction Transistors (BJT) and Unipolar Field Effect Transistors (FET).
- Physical Construction & Materials: N-channel and P-channel semiconductor geometries, ohmic contacts, and heavily doped p^+ gate wells.
- Schematic Representation: Circuit symbols, terminal polarities (D, S, G), and conventional current flow vectors.
- Zero-Bias Equilibrium ($V_{GS} = 0\text{V}, V_{DS} = 0\text{V}$): Built-in potential, depletion boundary profile, and equilibrium channel width.
- Ohmic Operating Region ($V_{DS} < |V_P|$): Linear channel resistance r_{ds0}, majority carrier drift, and current dependence on V_{DS}.
- Pinch-Off Mechanics & Saturation ($V_{DS} \geq V_{DS,sat}$): Asymmetric depletion widening, channel constriction, and velocity saturation.
- Gate Voltage Control ($V_{GS} < 0\text{V}$): Electrostatic channel narrowing, modified pinch-off boundaries, and Shockley's parabolic model.

Classification of Transistors & Principles of Voltage Control

- Unipolar vs Bipolar Conduction: BJTs rely on dual carrier injection (electrons and holes), whereas JFET conduction relies strictly on majority carriers (electrons in N-channel, holes in P-channel).
- Control Mechanism: BJT collector current is controlled by base current ($I_C = \beta I_B$), while JFET drain current is modulated by reverse gate voltage V_{GS} ($I_G \approx 0$ A).
- Input Impedance Superiority: Reverse-biased gate-channel PN junction provides ultra-high input impedance ($R_{in} \approx 10^8$ to $10^{11}\,\Omega$), minimizing loading on signal sources.
- Thermal Stability & Noise Performance: Absence of minority carrier storage effects eliminates thermal runaway risks and yields significantly lower flicker/shot noise compared to BJTs.

Physical Construction and Internal Geometry of N-Channel JFET

- Substrate Body & Channel Bar: Consists of a lightly-doped N-type silicon bar ($N_D \approx 10^{15}$ cm^{-3}) providing a conductive path between Source and Drain terminals.
- Heavily Doped Gate Regions: Two high-concentration p^+ regions ($N_A \approx 10^{18}$ cm^{-3}) diffused on opposite sides of the N-channel bar.
- Internal Gate Connection: The two p^+ regions are electrically connected internally or externally to form a single Gate terminal (G).
- Ohmic Contact Terminals: Metallic contacts at both ends of the N-bar form the Source (S) terminal (carrier entry) and Drain (D) terminal (carrier collection).
- Depletion Region Penetration: Due to asymmetrical doping ($N_A \gg N_D$), the PN junction depletion regions extend almost entirely into the lightly-doped N-channel.

Physical Construction & Carrier Mobility of P-Channel JFET

- Complementary Layout: Built using a lightly-doped P-type silicon bar ($N_A \approx 10^{15}$ cm^{-3}) flanked by two heavily-doped n^+ gate diffusion regions ($N_D \approx 10^{18}$ cm^{-3}).
- Majority Carrier Dynamics: Conduction occurs via hole transport through the P-channel under an applied negative drain-to-source bias ($V_{DS} < 0$V).
- Mobility Comparison: Hole drift mobility in silicon ($\mu_p \approx 450$ cm^2/V $\cdot$ s) is roughly one-third of electron mobility ($\mu_n \approx 1350$ cm^2/V $\cdot$ s).
- Performance Implication: For identical physical dimensions, P-channel JFETs exhibit higher channel resistance $R_{DS(on)}$ and lower transconductance g_m compared to N-channel counterparts.

Schematic Symbols, Terminal Conventions, and Voltage Polarities

- N-Channel Symbol: Features an arrow on the Gate terminal pointing inward toward the channel bar (representing $p^+ \rightarrow n$ junction polarity).
- P-Channel Symbol: Features an arrow on the Gate terminal pointing outward away from the channel bar ($p \rightarrow n^+$ polarity).
- Terminal Voltage Definitions: For N-channel, Drain is biased positive relative to Source ($V_{DS} > 0$V); Gate is biased negative relative to Source ($V_{GS} \leq 0$V).
- Gate Current Nullity Constraint: Under normal operating conditions, the Gate-Channel PN junction remains strictly reverse-biased, keeping gate current $I_G = 0$ A (practically $I_{GSS} < 1$ nA).
- Channel Continuity Equation: Kirchoff's Current Law yields $I_S = I_D + I_G \approx I_D$ under all standard bias states.

Zero-Bias Thermal Equilibrium State ($V_{GS} = 0\text{V}, V_{DS} = 0\text{V}$)

- Built-in Potential Bar: With no external voltages applied, a uniform depletion layer forms at the p^+n junctions with built-in potential $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \approx 0.7\text{V}$.
- Equilibrium Depletion Width: Space-charge depletion thickness $W_0 = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}}$ penetrates symmetrically into both sides of the N-channel.
- Unconstricted Conducting Path: A wide, uniform conductive channel exists between Source and Drain, offering maximum initial channel cross-sectional area.
- Zero Net Drift Current: In thermal equilibrium, electron diffusion current is exactly balanced by drift current across the junction barriers, resulting in $I_D = 0$ A.

Low Drain-Source Bias Operation ($V_{DS} > 0\text{V}, V_{GS} = 0\text{V}$): Ohmic Region

- Electric Field Setup: Applying a small positive voltage V_{DS} creates an axial electric field $E_x = \frac{V_{DS}}{L}$ along the length of the channel.
- Linear Majority Drift: Free electrons in the N-channel drift from Source to Drain, producing a drain current I_D proportional to V_{DS}.
- Channel Resistance Model: The channel behaves as an ideal linear resistor r_{ds0} given by $r_{ds0} = \frac{L}{q\mu_n N_D A_c}$, where A_c is the channel cross-sectional area.
- Slight Asymmetric Depletion: Potential along the channel increases from 0V at the source end to V_{DS} at the drain end, causing slightly greater reverse bias ($V_{DG} = V_{DS}$) near the drain.

Asymmetric Depletion Widening and Pinch-Off Mechanism ($V_{DS} = V_P$)

- Voltage-Drop Gradient: Potential at distance x along channel is $V(x)$, making gate-to-channel reverse bias $V_{GC}(x) = V_{GS} - V(x) = -V(x)$ (for $V_{GS} = 0$).
- Maximum Depletion at Drain End: Reverse bias is highest at the Drain terminal where $V_{GC} = -V_{DS}$, causing maximum depletion region width at $x = L$.
- Pinch-Off Point Definition: As V_{DS} reaches the Pinch-off Voltage V_P (e.g., $V_{DS} = |V_P| = 4\text{V}$), the depletion regions touch or nearly touch near the drain end.
- Constricted High-Field Region: Channel cross-section narrows to a minimum wedge shape; electron velocity reaches saturation ($v_{sat} \approx 10^7$ cm/s), preventing further current increase.

Saturation Operating Region Physics ($V_{DS} \geq V_{DS,sat}$)

- Current Clamping Behavior: For $V_{DS} > V_P$ (with $V_{GS} = 0$), the excess voltage ($V_{DS} - V_P$) drops across the narrow pinch-off space-charge region.
- Drain Current Saturation (I_{DSS}): The drain current remains practically constant at its maximum saturated value $I_D = I_{DSS}$ (Drain-to-Source Current at Zero Bias).
- Channel Length Modulation (ΔL): Increasing V_{DS} further shifts the pinch-off point slightly toward the source, effectively shortening the conductive channel length from L to $L - \Delta L$.
- Output Impedance Effect: Channel shortening introduces a slight upward slope in the I_D vs V_{DS} saturation curve, modeling finite output resistance $r_d = \frac{\partial V_{DS}}{\partial I_D}$.

Gate-Source Reverse Bias Modulation ($V_{GS} < 0$V)

- Initial Channel Narrowing: Applying negative gate voltage ($V_{GS} < 0$V) widens depletion regions uniformly along the entire channel prior to applying V_{DS}.
- Reduced Effective Pinch-Off Voltage: Pinch-off occurs at a lower drain voltage: $V_{DS,sat} = V_{GS} - V_P = V_{GS} + |V_P|$ (since V_P is negative for N-channel).
- Complete Cutoff State ($V_{GS} \leq V_P$): When V_{GS} reaches V_P, depletion regions meet completely along the full channel length, reducing drain current to zero ($I_D = 0$ A).
- Effective Channel Width Formula: $W(x) = a - W_{dep}(x)$, where a is physical channel half-width and $W_{dep}(x) \propto \sqrt{V_{bi} - V_{GS} + V(x)}$.

Mathematical Derivation of Shockley's Transconductance Relation

- Integration of Mobile Channel Charge: Integrating Ohm's law along the channel $I_D dx = q\mu_n N_D[2a - 2W_{dep}(x)]W_{width}dV$ yields exact current equations.
- Shockley's Parabolic Approximation: In the saturation region ($V_{DS} \geq V_{GS} - V_P$), the analytical integration reduces to Shockley's Square Law:
- $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
- Parameter Boundaries: I_{DSS} is maximum drain current at $V_{GS} = 0$V; V_P is pinch-off cutoff voltage (negative for N-channel, positive for P-channel).
- Valid Bias Range: Shockley's relation is valid strictly for $V_P \leq V_{GS} \leq 0$V (for N-channel) in the saturation operating region.

Comprehensive Numerical Example: JFET Operating Regimes and Q-Point

- Problem Statement: An N-channel JFET has parameters $I_{DSS} = 12$ mA and $V_P = -4.0$V. Determine the drain current I_D and minimum drain-source saturation voltage $V_{DS,sat}$ for (a) $V_{GS} = 0$V, (b) $V_{GS} = -1.5$V, and (c) $V_{GS} = -3.0$V.
- Case (a) $V_{GS} = 0$V:
- $$I_D = 12 \text{ mA} \left(1 - \frac{0}{-4}\right)^2 = 12.0 \text{ mA}, \quad V_{DS,sat} = 0 - (-4) = 4.0\text{V}$$
- Case (b) $V_{GS} = -1.5$V:
- $$I_D = 12 \text{ mA} \left(1 - \frac{-1.5}{-4}\right)^2 = 12\,(0.625)^2 = 4.6875 \text{ mA}, \quad V_{DS,sat} = -1.5 - (-4) = 2.5\text{V}$$
- Case (c) $V_{GS} = -3.0$V:
- $$I_D = 12 \text{ mA} \left(1 - \frac{-3.0}{-4}\right)^2 = 12\,(0.25)^2 = 0.75 \text{ mA}, \quad V_{DS,sat} = -3.0 - (-4) = 1.0\text{V}$$

Comprehensive Summary: JFET Physical Operating Zones & Fundamental Equations

- Unipolar Device Physics: JFETs control majority carrier drift current using reverse-biased PN junction depletion fields without drawing gate current.
- Three Distinct Operating Zones:
- 1. Ohmic / Linear Region ($V_{DS} < V_{GS} - V_P$): Device acts as voltage-controlled resistor r_{ds}.
- 2. Saturation / Pinch-off Region ($V_{DS} \geq V_{GS} - V_P$): I_D saturates to constant current governed by $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
- 3. Cutoff Region ($V_{GS} \leq V_P$): Depletion regions merge completely across channel; $I_D = 0$ A.
- Key Design Parameters: Maximum drain current I_{DSS}, pinch-off voltage V_P, and high input impedance $R_{in} \geq 10^8\,\Omega$.