Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

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Lecture Outline: JFET Fundamentals, Device Physics, and Analytical Modeling

- Transistor Classification: Comparison between Bipolar Junction Transistors (BJT) and Unipolar Field Effect Transistors (FET).
- Physical Construction & Materials: N-channel and P-channel semiconductor geometries, ohmic contacts, and heavily doped p^+ gate wells.
- Schematic Representation: Circuit symbols, terminal polarities (D, S, G), and conventional current flow vectors.
- Zero-Bias Equilibrium ($V_{GS} = 0\text{V}, V_{DS} = 0\text{V}$): Built-in potential, depletion boundary profile, and equilibrium channel width.
- Ohmic Operating Region ($V_{DS} < |V_P|$): Linear channel resistance r_{ds0}, majority carrier drift, and current dependence on V_{DS}.
- Pinch-Off Mechanics & Saturation ($V_{DS} \geq V_{DS,sat}$): Asymmetric depletion widening, channel constriction, and velocity saturation.
- Gate Voltage Control ($V_{GS} < 0\text{V}$): Electrostatic channel narrowing, modified pinch-off boundaries, and Shockley's parabolic model.

Classification of Transistors & Principles of Voltage Control

- Unipolar vs Bipolar Conduction: BJTs rely on dual carrier injection (electrons and holes), whereas JFET conduction relies strictly on majority carriers (electrons in N-channel, holes in P-channel).
- Control Mechanism: BJT collector current is controlled by base current ($I_C = \beta I_B$), while JFET drain current is modulated by reverse gate voltage V_{GS} ($I_G \approx 0$ A).
- Input Impedance Superiority: Reverse-biased gate-channel PN junction provides ultra-high input impedance ($R_{in} \approx 10^8$ to $10^{11}\,\Omega$), minimizing loading on signal sources.
- Thermal Stability & Noise Performance: Absence of minority carrier storage effects eliminates thermal runaway risks and yields significantly lower flicker/shot noise compared to BJTs.

Physical Construction and Internal Geometry of N-Channel JFET

- Substrate Body & Channel Bar: Consists of a lightly-doped N-type silicon bar ($N_D \approx 10^{15}$ cm^{-3}) providing a conductive path between Source and Drain terminals.
- Heavily Doped Gate Regions: Two high-concentration p^+ regions ($N_A \approx 10^{18}$ cm^{-3}) diffused on opposite sides of the N-channel bar.
- Internal Gate Connection: The two p^+ regions are electrically connected internally or externally to form a single Gate terminal (G).
- Ohmic Contact Terminals: Metallic contacts at both ends of the N-bar form the Source (S) terminal (carrier entry) and Drain (D) terminal (carrier collection).
- Depletion Region Penetration: Due to asymmetrical doping ($N_A \gg N_D$), the PN junction depletion regions extend almost entirely into the lightly-doped N-channel.

Physical Construction & Carrier Mobility of P-Channel JFET

- Complementary Layout: Built using a lightly-doped P-type silicon bar ($N_A \approx 10^{15}$ cm^{-3}) flanked by two heavily-doped n^+ gate diffusion regions ($N_D \approx 10^{18}$ cm^{-3}).
- Majority Carrier Dynamics: Conduction occurs via hole transport through the P-channel under an applied negative drain-to-source bias ($V_{DS} < 0$V).
- Mobility Comparison: Hole drift mobility in silicon ($\mu_p \approx 450$ cm^2/V $\cdot$ s) is roughly one-third of electron mobility ($\mu_n \approx 1350$ cm^2/V $\cdot$ s).
- Performance Implication: For identical physical dimensions, P-channel JFETs exhibit higher channel resistance $R_{DS(on)}$ and lower transconductance g_m compared to N-channel counterparts.

Schematic Symbols, Terminal Conventions, and Voltage Polarities

- N-Channel Symbol: Features an arrow on the Gate terminal pointing inward toward the channel bar (representing $p^+ \rightarrow n$ junction polarity).
- P-Channel Symbol: Features an arrow on the Gate terminal pointing outward away from the channel bar ($p \rightarrow n^+$ polarity).
- Terminal Voltage Definitions: For N-channel, Drain is biased positive relative to Source ($V_{DS} > 0$V); Gate is biased negative relative to Source ($V_{GS} \leq 0$V).
- Gate Current Nullity Constraint: Under normal operating conditions, the Gate-Channel PN junction remains strictly reverse-biased, keeping gate current $I_G = 0$ A (practically $I_{GSS} < 1$ nA).
- Channel Continuity Equation: Kirchoff's Current Law yields $I_S = I_D + I_G \approx I_D$ under all standard bias states.

Zero-Bias Thermal Equilibrium State ($V_{GS} = 0\text{V}, V_{DS} = 0\text{V}$)

- Built-in Potential Bar: With no external voltages applied, a uniform depletion layer forms at the p^+n junctions with built-in potential $V_{bi} = \frac{kT}{q} \ln\left(\frac{N_A N_D}{n_i^2}\right) \approx 0.7\text{V}$.
- Equilibrium Depletion Width: Space-charge depletion thickness $W_0 = \sqrt{\frac{2\varepsilon_s V_{bi}}{qN_D}}$ penetrates symmetrically into both sides of the N-channel.
- Unconstricted Conducting Path: A wide, uniform conductive channel exists between Source and Drain, offering maximum initial channel cross-sectional area.
- Zero Net Drift Current: In thermal equilibrium, electron diffusion current is exactly balanced by drift current across the junction barriers, resulting in $I_D = 0$ A.

Low Drain-Source Bias Operation ($V_{DS} > 0\text{V}, V_{GS} = 0\text{V}$): Ohmic Region

- Electric Field Setup: Applying a small positive voltage V_{DS} creates an axial electric field $E_x = \frac{V_{DS}}{L}$ along the length of the channel.
- Linear Majority Drift: Free electrons in the N-channel drift from Source to Drain, producing a drain current I_D proportional to V_{DS}.
- Channel Resistance Model: The channel behaves as an ideal linear resistor r_{ds0} given by $r_{ds0} = \frac{L}{q\mu_n N_D A_c}$, where A_c is the channel cross-sectional area.
- Slight Asymmetric Depletion: Potential along the channel increases from 0V at the source end to V_{DS} at the drain end, causing slightly greater reverse bias ($V_{DG} = V_{DS}$) near the drain.

Asymmetric Depletion Widening and Pinch-Off Mechanism ($V_{DS} = V_P$)

- Voltage-Drop Gradient: Potential at distance x along channel is $V(x)$, making gate-to-channel reverse bias $V_{GC}(x) = V_{GS} - V(x) = -V(x)$ (for $V_{GS} = 0$).
- Maximum Depletion at Drain End: Reverse bias is highest at the Drain terminal where $V_{GC} = -V_{DS}$, causing maximum depletion region width at $x = L$.
- Pinch-Off Point Definition: As V_{DS} reaches the Pinch-off Voltage V_P (e.g., $V_{DS} = |V_P| = 4\text{V}$), the depletion regions touch or nearly touch near the drain end.
- Constricted High-Field Region: Channel cross-section narrows to a minimum wedge shape; electron velocity reaches saturation ($v_{sat} \approx 10^7$ cm/s), preventing further current increase.

Saturation Operating Region Physics ($V_{DS} \geq V_{DS,sat}$)

- Current Clamping Behavior: For $V_{DS} > V_P$ (with $V_{GS} = 0$), the excess voltage ($V_{DS} - V_P$) drops across the narrow pinch-off space-charge region.
- Drain Current Saturation (I_{DSS}): The drain current remains practically constant at its maximum saturated value $I_D = I_{DSS}$ (Drain-to-Source Current at Zero Bias).
- Channel Length Modulation (ΔL): Increasing V_{DS} further shifts the pinch-off point slightly toward the source, effectively shortening the conductive channel length from L to $L - \Delta L$.
- Output Impedance Effect: Channel shortening introduces a slight upward slope in the I_D vs V_{DS} saturation curve, modeling finite output resistance $r_d = \frac{\partial V_{DS}}{\partial I_D}$.

Gate-Source Reverse Bias Modulation ($V_{GS} < 0$V)

- Initial Channel Narrowing: Applying negative gate voltage ($V_{GS} < 0$V) widens depletion regions uniformly along the entire channel prior to applying V_{DS}.
- Reduced Effective Pinch-Off Voltage: Pinch-off occurs at a lower drain voltage: $V_{DS,sat} = V_{GS} - V_P = V_{GS} + |V_P|$ (since V_P is negative for N-channel).
- Complete Cutoff State ($V_{GS} \leq V_P$): When V_{GS} reaches V_P, depletion regions meet completely along the full channel length, reducing drain current to zero ($I_D = 0$ A).
- Effective Channel Width Formula: $W(x) = a - W_{dep}(x)$, where a is physical channel half-width and $W_{dep}(x) \propto \sqrt{V_{bi} - V_{GS} + V(x)}$.

Mathematical Derivation of Shockley's Transconductance Relation

- Integration of Mobile Channel Charge: Integrating Ohm's law along the channel $I_D dx = q\mu_n N_D[2a - 2W_{dep}(x)]W_{width}dV$ yields exact current equations.
- Shockley's Parabolic Approximation: In the saturation region ($V_{DS} \geq V_{GS} - V_P$), the analytical integration reduces to Shockley's Square Law:
- $$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$
- Parameter Boundaries: I_{DSS} is maximum drain current at $V_{GS} = 0$V; V_P is pinch-off cutoff voltage (negative for N-channel, positive for P-channel).
- Valid Bias Range: Shockley's relation is valid strictly for $V_P \leq V_{GS} \leq 0$V (for N-channel) in the saturation operating region.

Comprehensive Numerical Example: JFET Operating Regimes and Q-Point

- Problem Statement: An N-channel JFET has parameters $I_{DSS} = 12$ mA and $V_P = -4.0$V. Determine the drain current I_D and minimum drain-source saturation voltage $V_{DS,sat}$ for (a) $V_{GS} = 0$V, (b) $V_{GS} = -1.5$V, and (c) $V_{GS} = -3.0$V.
- Case (a) $V_{GS} = 0$V:
- $$I_D = 12 \text{ mA} \left(1 - \frac{0}{-4}\right)^2 = 12.0 \text{ mA}, \quad V_{DS,sat} = 0 - (-4) = 4.0\text{V}$$
- Case (b) $V_{GS} = -1.5$V:
- $$I_D = 12 \text{ mA} \left(1 - \frac{-1.5}{-4}\right)^2 = 12\,(0.625)^2 = 4.6875 \text{ mA}, \quad V_{DS,sat} = -1.5 - (-4) = 2.5\text{V}$$
- Case (c) $V_{GS} = -3.0$V:
- $$I_D = 12 \text{ mA} \left(1 - \frac{-3.0}{-4}\right)^2 = 12\,(0.25)^2 = 0.75 \text{ mA}, \quad V_{DS,sat} = -3.0 - (-4) = 1.0\text{V}$$

Comprehensive Summary: JFET Physical Operating Zones & Fundamental Equations

- Unipolar Device Physics: JFETs control majority carrier drift current using reverse-biased PN junction depletion fields without drawing gate current.
- Three Distinct Operating Zones:
- 1. Ohmic / Linear Region ($V_{DS} < V_{GS} - V_P$): Device acts as voltage-controlled resistor r_{ds}.
- 2. Saturation / Pinch-off Region ($V_{DS} \geq V_{GS} - V_P$): I_D saturates to constant current governed by $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
- 3. Cutoff Region ($V_{GS} \leq V_P$): Depletion regions merge completely across channel; $I_D = 0$ A.
- Key Design Parameters: Maximum drain current I_{DSS}, pinch-off voltage V_P, and high input impedance $R_{in} \geq 10^8\,\Omega$.

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Lecture Outline: JFET Parameter Derivations, AC Models, and Thermal Sensitivity

- Transconductance (g_m): Definition, derivative from Shockley's equation, and V_{GS} bias dependence.
- Zero-Bias Transconductance (g_{m0}): Maximum transconductance evaluation at $V_{GS} = 0\text{V}$.
- Dynamic Drain Resistance (r_d): Definition, physical cause (channel length modulation), and output conductance (g_{os}).
- Amplification Factor (μ): Inter-relationship $\mu = g_m \cdot r_d$ and theoretical voltage gain ceiling.
- Gate Leakage & Input Impedance: Temperature-dependent reverse saturation current I_{GSS} and $R_{in} \geq 10^9\,\Omega$.
- High-Frequency Parasitics: Inter-electrode capacitances (C_{gs}, C_{gd}, C_{ds}) and Miller multiplication effect.
- Thermal Physics & Breakdown: Zero Temperature Coefficient (ZTC) point and avalanche breakdown (BV_{DGO}).
- Small-Signal Equivalent Circuit & Applied Example: AC load-line analysis and voltage gain computation.

Transconductance (g_m) Parameter Derivation & Non-linear Bias Dependence

- Definition of Transconductance: Measures the control of gate voltage over drain current at a constant drain-source bias: $g_m = \frac{\partial I_D}{\partial V_{GS}}\Big|_{V_{DS}=\text{const}}$.
- Mathematical Derivation from Shockley's Equation: Differentiating $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ with respect to V_{GS} yields:
- $$g_m = \frac{\partial}{\partial V_{GS}}\left[I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2\right] = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right)$$
- Linear Dependence on Gate Voltage: Unlike BJTs where $g_m = \frac{I_C}{V_T}$ scales linearly with current, JFET transconductance scales linearly with gate voltage V_{GS} (and square-root of current $\sqrt{I_D}$).
- Relation to Saturated Current: Substituting $\sqrt{\frac{I_D}{I_{DSS}}} = 1 - \frac{V_{GS}}{V_P}$ yields $g_m = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}}$.

Zero-Bias Transconductance (g_{m0}) & Graphical Determination

- Maximum Transconductance (g_{m0}): Evaluated at zero gate bias ($V_{GS} = 0\text{V}$):
- $$g_{m0} = \frac{2I_{DSS}}{|V_P|}$$
- Slope of Transfer Curve: g_{m0} represents the maximum slope of the transfer characteristic curve (I_D vs V_{GS}), occurring at the y-intercept ($V_{GS} = 0\text{V}$).
- Typical Parameter Values: For standard signal JFETs (e.g., 2N5457, 2N3819), $I_{DSS} = 2$ to 12 mA and $V_P = -2$ to -6V, yielding $g_{m0} \approx 1000$ to $6000\,\mu\text{S}$ (1 to 6 mS).
- Design Consideration: Higher I_{DSS} and sharper (smaller magnitude) V_P maximize transconductance and resulting AC voltage gain.

Dynamic Drain Resistance (r_d) & Channel Length Modulation

- Definition of Dynamic Drain Resistance: Inverse slope of the drain characteristic curve in the saturation region:
- $$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{const}} = \frac{1}{g_{os}}$$

  (where g_{os} is output admittance).
- Physical Origin: Caused by Channel Length Modulation (λ). As V_{DS} increases beyond $V_{DS,sat}$, the pinch-off point moves closer to the source, reducing effective channel length $L' = L - \Delta L$.
- Modified Current Equation: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 (1 + \lambda V_{DS})$, where λ is the channel length modulation parameter (V^{-1}).
- Typical Values: r_d typically ranges from 10 kΩ to 500 kΩ for signal JFETs, reflecting high output impedance ideal for current sources.

Amplification Factor (μ) & Parameter Inter-relationship

- Definition of Amplification Factor (μ): Ratio of change in drain-source voltage to change in gate-source voltage required to maintain constant drain current:
- $$\mu = \left.\frac{\Delta V_{DS}}{\Delta V_{GS}}\right|_{I_D=\text{const}}$$

  (dimensionless quantity).
- Fundamental Relation Derivation: Chain rule expansion yields $\Delta I_D = \left(\frac{\partial I_D}{\partial V_{GS}}\right)\Delta V_{GS} + \left(\frac{\partial I_D}{\partial V_{DS}}\right)\Delta V_{DS} = 0$.
- $$\mu = g_m \cdot r_d$$
- Physical Significance: μ represents the maximum theoretical voltage gain achievable by the JFET in an open-circuit (infinite load resistance) common-source amplifier configuration.
- Typical Range: Standard JFET amplification factors range from $\mu = 40$ to 500.

Gate Leakage Current (I_{GSS}) & Ultra-High Input Impedance

- Reverse Leakage Origin: Gate current I_{GSS} is the reverse saturation leakage current across the reverse-biased Gate-to-Channel PN junction.
- Magnitude at Room Temperature: Typically $I_{GSS} \approx 10$ pA to 1 nA at $T = 25^{\circ}$C for silicon JFETs.
- Input DC Impedance Calculation: $R_{in(DC)} = \frac{|V_{GS}|}{I_{GSS}} \approx \frac{1\text{V}}{10\text{ pA}} = 10^{11}\,\Omega = 100\text{ G}\Omega$.
- Thermal Sensitivity of I_{GSS}: Reverse leakage doubles approximately every 10°C temperature rise:
- $$I_{GSS}(T) = I_{GSS}(25^{\circ}\text{C}) \cdot 2^{\frac{T-25}{10}}$$
- Practical Implication: At $T = 125^{\circ}$C, I_{GSS} increases by $2^{10} = 1024\times$, reducing input resistance to ~ 100 MΩ.

High-Frequency Parasitic Capacitances (C_{gs}, C_{gd}, C_{ds})

- Gate-Source Junction Capacitance (C_{gs}): Depletion layer transition capacitance across the gate-source PN junction ($C_{gs} \approx 2$ to 10 pF).
- Gate-Drain Junction Capacitance (C_{gd}): Reverse-biased junction capacitance between gate and drain ($C_{gd} \approx 1$ to 5 pF).
- Drain-Source Parasitic Capacitance (C_{ds}): Geometry-dependent capacitive coupling between drain and source metal contacts ($C_{ds} \approx 0.1$ to 1 pF).
- Voltage-Dependent Capacitance: $C_{gd}(V_{GD}) = \frac{C_{gd0}}{\sqrt{1+\frac{V_{GD}}{V_{bi}}}}$, shrinking as reverse bias increases.
- Miller Effect Bandwidth Constraint: In Common-Source amplifiers, C_{gd} is multiplied by voltage gain A_v, creating equivalent input capacitance $C_{in,Miller} = C_{gs} + C_{gd}(1 + |A_v|)$.

Temperature Dependencies of JFET Parameters

- Dual Competing Thermal Effects:
- 1. Carrier Mobility Degradation: Temperature rise increases lattice scattering, reducing electron mobility $\mu_n(T) \propto T^{-3/2}$, which decreases I_{DSS} and g_m.
- 2. Built-in Potential Reduction: Barrier potential V_{bi} decreases by approximately -2.2 mV/°C, narrowing depletion regions and slightly increasing channel width.
- Dominant Effect: At typical operating current levels, mobility degradation dominates, causing I_{DSS} to possess a negative temperature coefficient (NTC).
- Thermal Runaway Immunity: Unlike BJTs whose collector current increases exponentially with temperature (V_{BE} drop), JFET drain current naturally decreases at elevated temperatures, preventing thermal runaway.

Zero Temperature Coefficient (ZTC) Operating Bias Point

- Thermal Compensation Principle: Perfect cancellation occurs when mobility drop precisely balances built-in potential barrier reduction.
- ZTC Gate Bias Condition: The required gate-source voltage for Zero Temperature Coefficient is mathematically derived as:
- $$|V_{GS,ZTC}| = |V_P| - 0.63\text{V}$$
- ZTC Drain Current Formula: Corresponding temperature-independent drain current level:
- $$I_{D,ZTC} = I_{DSS}\left(\frac{0.63\text{V}}{|V_P|}\right)^2$$
- Practical Significance: Biasing a JFET precisely at $(V_{GS,ZTC}, I_{D,ZTC})$ ensures zero drift in Q-point current across wide ambient temperature swings (-55°C to $+125^\circ$C).

JFET Electrical Breakdown Mechanisms (BV_{DGO} & BV_{DS})

- Avalanche Breakdown Location: Occurs across the reverse-biased Gate-Drain PN junction where electric field intensity is highest.
- Maximum Gate-Drain Breakdown Voltage (BV_{DGO}): Datasheet rating for avalanche breakdown between Drain and Gate with Source open-circuited.
- Composite Breakdown Condition: Avalanche occurs when total reverse voltage across the gate-drain junction exceeds BV_{DGO}:
- $$V_{DG} = V_{DS} - V_{GS} = BV_{DGO}$$
- Drain-Source Breakdown Voltage (BV_{DS}): Maximum safe V_{DS} decreases linearly with increasingly negative gate bias V_{GS}:
- $$BV_{DS} = BV_{DGO} - |V_{GS}|$$
- Destructive Avalanche Behavior: Once breakdown occurs, drain current increases exponentially, causing destructive localized dissipation if current is not limited by external circuit resistance.

Small-Signal Low-Frequency and High-Frequency AC Models

- Low-Frequency AC Equivalent Circuit: Voltage-controlled current source $g_m v_{gs}$ in parallel with output resistance r_d; gate input modeled as open-circuit ($R_{in} = \infty$).
- High-Frequency Hybrid-π Model: Incorporates C_{gs} between Gate and Source, C_{gd} between Gate and Drain, and C_{ds} between Drain and Source.
- Voltage Gain Formula (Low-Frequency Common-Source):
- $$A_v = \frac{v_o}{v_{in}} = -g_m(R_D \parallel R_L \parallel r_d)$$
- Unity-Gain Transition Frequency (f_T): Frequency at which short-circuit current gain drops to unity:
- $$f_T = \frac{g_m}{2\pi(C_{gs} + C_{gd})}$$

Quantitative Example: Small-Signal Parameter & AC Gain Computation

- Problem Statement: A JFET amplifier operates with $I_{DSS} = 10$ mA, $V_P = -3.5$V, $r_d = 40$ kΩ, and $BV_{DGO} = 30$V. The DC bias is set at $V_{GSQ} = -1.0$V with drain load $R_D = 4.7$ kΩ.
- 1. Calculate g_{m0} and g_m at the Q-point:
- $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{3.5\text{V}} = 5.714\text{ mS}$$
- $$g_m = g_{m0}\left(1 - \frac{-1.0}{-3.5}\right) = 5.714\,(1 - 0.2857) = 4.081\text{ mS}$$
- 2. Compute Amplification Factor μ:
- $$\mu = g_m \cdot r_d = (4.081\text{ mS})(40\text{ k}\Omega) = 163.2$$
- 3. Calculate Loaded AC Voltage Gain A_v ($R_L = \infty$):
- $$A_v = -g_m(R_D \parallel r_d) = -(4.081\text{ mS})\left(\frac{4.7 \times 40}{4.7 + 40}\text{ k}\Omega\right) = -(4.081)(4.205) = -17.16\text{ V/V}$$
- 4. Evaluate Maximum Safe Breakdown Voltage BV_{DS}:
- $$BV_{DS} = BV_{DGO} - |V_{GSQ}| = 30\text{V} - 1.0\text{V} = 29.0\text{V}$$

Summary of JFET Small-Signal Parameters, Thermal Properties & Limits

- Dynamic AC Parameters Matrix:
- • Transconductance: $g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$ where $g_{m0} = \frac{2I_{DSS}}{|V_P|}$.
- • Dynamic Drain Resistance: $r_d = \frac{1}{\lambda I_D} = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}}$.
- • Amplification Factor: $\mu = g_m r_d$ (intrinsic voltage gain upper bound).
- Thermal Stability: ZTC bias condition $|V_{GS,ZTC}| = |V_P| - 0.63\text{V}$ provides temperature-independent Q-point operation.
- High-Frequency & Voltage Boundaries: Miller-multiplied C_{gd} limits RF bandwidth; avalanche breakdown restricts maximum drain bias to $BV_{DS} = BV_{DGO} - |V_{GS}|$.

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Lecture Outline: MOS Structural Physics, Energy Band Diagrams, and Threshold Derivation

- MOS Structure Architecture: Stack layout, material parameters ($\varepsilon_{ox}, \varepsilon_s$), and oxide thickness t_{ox}.
- Oxide Capacitance & Electrostatics: Formula for unit-area oxide capacitance $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$ and total gate charge.
- Flat-Band Condition ($V_G = V_{FB}$): Work function difference Φ_{ms}, fixed oxide charges Q_{ox}, and zero band bending.
- Accumulation Operating Regime ($V_G < V_{FB}$ for P-substrate): Surface hole accumulation and energy band bending upwards.
- Depletion Operating Regime ($V_{FB} < V_G < V_{th}$): Uncovering acceptor ions, depletion width W_{dep}, and downward band bending.
- Strong Inversion Regime ($V_G \geq V_{th}$): Surface inversion criteria $\phi_s = 2\phi_F$, minority carrier channel formation.
- Threshold Voltage (V_{th}) Closed-Form Derivation: Summing flat-band, surface potential, and bulk depletion charge terms.
- Substrate Bias / Body Effect: Impact of $V_{SB} > 0$V on depletion width and threshold voltage shift ΔV_{th}.

The Two-Terminal MOS Structure & Material Dielectric Constants

- Physical Stack Composition: Heavily-doped n^+ polysilicon (or metal) Gate electrode, amorphous Silicon Dioxide (SiO_2) gate dielectric, and P-type monocrystalline silicon substrate (p-sub).
- Gate Oxide Dielectric Properties: Silicon Dioxide relative permittivity $\varepsilon_{r,ox} = 3.9$, oxide permittivity $\varepsilon_{ox} = \varepsilon_{r,ox}\varepsilon_0 \approx 3.45 \times 10^{-13}$ F/cm.
- Silicon Semiconductor Properties: Silicon relative permittivity $\varepsilon_{r,Si} = 11.7$, semiconductor permittivity $\varepsilon_s = \varepsilon_{r,Si}\varepsilon_0 \approx 1.04 \times 10^{-12}$ F/cm.
- Insulation Superiority: SiO_2 energy bandgap $E_g \approx 9.0$ eV provides near-infinite DC resistivity ($> 10^{16}\,\Omega \cdot$ cm), preventing gate leakage current.
- Scaling Trend: Oxide thickness t_{ox} has scaled down from 100 nm in legacy nodes to < 1.5 nm in sub-micron technologies (where high-k metal gates replace SiO_2).

Oxide Electrostatics & Unit-Area Capacitance (C_{ox})

- Unit-Area Oxide Capacitance Formula: Defined as oxide permittivity divided by gate dielectric thickness t_{ox}:
- $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-13}\ \text{F/cm}}{t_{ox}\ (\text{cm})}$$
- Numerical Significance: For $t_{ox} = 10\ \text{nm} = 10^{-6}\ \text{cm}$, $C_{ox} = \frac{3.45 \times 10^{-13}}{10^{-6}} = 3.45 \times 10^{-7}\ \text{F/cm}^2 = 3.45\ \text{fF}/\mu\text{m}^2$.
- Total Gate Capacitance: $C_G = C_{ox} \cdot W \cdot L$, where W is channel width and L is channel length.
- Charge-Voltage Storage Law: Induced gate charge per unit area $Q_G = C_{ox}(V_G - V_{FB} - \phi_s)$, where ϕ_s is semiconductor surface potential.

Flat-Band Condition ($V_G = V_{FB}$) & Work Function Differences

- Ideal MOS Assumption: If metal work function Φ_m matched semiconductor work function Φ_s, zero gate bias ($V_G = 0$) would yield flat energy bands.
- Real Work Function Difference (Φ_{ms}): Difference between gate Fermi level and substrate Fermi level: $\Phi_{ms} = \Phi_m - \left(\chi + \frac{E_g}{2q} + \phi_F\right)$.
- Fermi Potential Formula (P-Substrate): $\phi_F = V_T \ln\left(\frac{N_A}{n_i}\right)$, where $V_T = \frac{kT}{q} \approx 0.0259\text{V}$ at room temperature.
- Fixed Oxide Charge (Q_{ox}): Parasitic positive charges trapped near the $SiO_2 - Si$ interface shift band bending.
- Flat-Band Voltage Formula: The gate voltage required to restore zero band bending across the semiconductor substrate:
-

$$V_{FB} = \Phi_{ms} - \frac{Q_{ox}}{C_{ox}}$$

Accumulation Operating Regime ($V_G < V_{FB}$ for P-Substrate)

- Applied Gate Voltage Condition: Gate is biased negatively relative to flat-band voltage ($V_G < V_{FB}$).
- Electrostatic Field Orientation: Negative charge on gate electrode attracts positive majority carriers (holes) toward the $SiO_2 - Si$ interface.
- Energy Band Behavior: Conduction band E_c, valence band E_v, and intrinsic Fermi level E_i bend upward near the oxide interface.
- Surface Hole Concentration: $p_s = N_A e^{\frac{-q\phi_s}{kT}} > N_A$ (since surface potential $\phi_s < 0$).
- Capacitance State: System acts as a pure parallel-plate capacitor with high capacitance equal to C_{ox} because hole accumulation layer touches the oxide interface.

Depletion Operating Regime ($V_{FB} < V_G < V_{th}$)

- Applied Gate Voltage Condition: Gate potential is increased above flat-band voltage but remains below threshold voltage.
- Majority Carrier Repulsion: Positive gate charge repels mobile holes away from the $SiO_2 - Si$ interface into the bulk substrate.
- Uncovered Acceptor Ions: Leaves behind a space-charge depletion region composed of fixed, negatively charged acceptor ions (N_A^-).
- Depletion Width Formula: Space-charge layer width increases with surface potential $\phi_s > 0$:
- $$W_{dep} = \sqrt{\frac{2\varepsilon_s \phi_s}{qN_A}}$$
- Energy Band Behavior: Bands bend downward near the interface; E_i moves closer to the Fermi level E_F at the surface.

Strong Inversion Regime & Threshold Criteria ($\phi_s = 2\phi_F$)

- Onset of Inversion: As V_G increases further, surface potential ϕ_s increases until intrinsic level E_i crosses below Fermi level E_F at the surface.
- Strong Inversion Definition: Reached when electron concentration at the surface (n_s) equals original hole concentration in the bulk substrate (N_A).
- Surface Potential Criterion for Strong Inversion: Surface potential must reach exactly twice the bulk Fermi potential:
- $$\phi_{s,\text{inv}} = 2\phi_F = 2V_T \ln\left(\frac{N_A}{n_i}\right)$$
- Inversion Conducting Channel: Mobile minority electrons aggregate in an extremely thin surface inversion layer ($t_{inv} \approx 2$ to 5 nm), forming an N-channel.
- Maximum Depletion Layer Width (W_{max}): Once strong inversion occurs, further gate voltage increase adds mobile channel electrons rather than expanding depletion width:
- $$W_{max} = \sqrt{\frac{2\varepsilon_s(2\phi_F)}{qN_A}}$$

Mathematical Derivation of Threshold Voltage (V_{th})

- Charge Balance Conservation Equation: Total applied gate voltage equals flat-band voltage plus surface potential drop plus voltage drop across gate oxide:

$$V_{th} = V_{FB} + \phi_{s,\text{inv}} + V_{ox} = V_{FB} + 2\phi_F + \frac{|Q_{dep}|}{C_{ox}}$$

- Bulk Depletion Charge at Inversion: Charge per unit area of unshielded acceptor ions at W_{max}:

$$|Q_{dep}| = qN_A W_{max} = \sqrt{2\varepsilon_s qN_A(2\phi_F)}$$

- Complete Threshold Voltage Formula (P-Substrate, N-Channel):

$$V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s qN_A(2\phi_F)}}{C_{ox}}$$

- Physical Control Knobs: V_{th} can be engineered via substrate doping N_A, gate oxide thickness t_{ox} (via C_{ox}), gate work function Φ_m, and threshold adjust ion implantation.

Substrate Bias / Body Effect Physics & Shift (ΔV_{th})

- Body Terminal Bias (V_{SB}): When Source and Body (Substrate) terminals are not at equal potential, applying reverse body bias ($V_{SB} > 0$V) increases reverse potential across the substrate-channel junction.
- Depletion Region Expansion: Effective potential across bulk depletion region becomes $(2\phi_F + V_{SB})$, increasing depletion charge to $|Q_{dep}| = \sqrt{2\varepsilon_s q N_A (2\phi_F + V_{SB})}$.
- Body Effect Parameter (γ): Defined as $\gamma = \frac{\sqrt{2\varepsilon_s q N_A}}{C_{ox}}$ (units of $V^{1/2}$).
- Modified Threshold Voltage Equation with Body Effect:
- $$V_{th} = V_{th0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$
- Practical Consequence: Reverse body bias ($V_{SB} > 0$) increases threshold voltage V_{th}, reducing drive current in stacked transistor topologies (e.g., cascode amplifiers, NAND logic gates).

Oxide Charges & Interface Trapped Charge Classification

- 1. Fixed Oxide Charge (Q_f): Stable positive ionic charge located within 2 nm of the $SiO_2 - Si$ transition layer, determined by oxidation thermal profile.
- 2. Mobile Ionic Charge (Q_m): Alkali metal contaminants (e.g., Na^+, K^+) that drift through oxide under electric fields, causing threshold instability.
- 3. Interface Trapped Charge (Q_{it}): Dangling silicon bonds at the interface creating energy traps within forbidden bandgap, reduced by hydrogen anneal.
- 4. Oxide Trapped Charge (Q_{ot}): Holes or electrons trapped in bulk oxide caused by ionizing radiation or hot carrier injection.
- Combined Threshold Voltage Offset: Total parasitic charge $Q_{ox} = Q_f + Q_m + Q_{it} + Q_{ot}$ shifts threshold voltage by $\Delta V_{th} = -\frac{Q_{ox}}{C_{ox}}$.

Architectural Structural Differences: JFET vs MOSFET Comparison

- Gate Isolation Mechanism: JFET relies on reverse-biased PN junction (susceptible to forward breakdown if $V_{GS} > 0.7$V), whereas MOSFET relies on solid oxide insulator SiO_2.
- DC Gate Input Current: JFET $I_G \approx 10^{-9}$ to 10^{-12} A; MOSFET $I_G \approx 10^{-14}$ to 10^{-15} A (femtoamperes).
- Operational Flexibility: JFET operates strictly in depletion mode; MOSFET can be designed for either Depletion-Mode or Enhancement-Mode (normally-OFF).
- Electrostatic Discharge (ESD) Sensitivity: Thin MOSFET gate oxide ($t_{ox} < 10$ nm) is vulnerable to dielectric breakdown from static voltage spikes (> 15V), requiring internal ESD protection diodes.

Quantitative Example: MOS Electrostatics & Threshold Calculation

- Problem Statement: Consider an N-channel MOS structure on a P-type silicon substrate with doping $N_A = 10^{16}$ cm^{-3}, gate oxide thickness $t_{ox} = 15$ nm, flat-band voltage $V_{FB} = -0.85$V, and intrinsic concentration $n_i = 1.5 \times 10^{10}$ cm^{-3}.
- 1. Calculate Unit-Area Oxide Capacitance C_{ox}:
- $$C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}} = \frac{3.45 \times 10^{-13}\ \text{F/cm}}{15 \times 10^{-7}\ \text{cm}} = 2.30 \times 10^{-7}\ \text{F/cm}^2 = 0.230\mu\text{F/cm}^2$$
- 2. Compute Substrate Fermi Potential ϕ_F:
- $$\phi_F = (0.0259\text{V}) \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.0259 \times 13.41 = 0.347\text{V}$$
- 3. Calculate Maximum Depletion Width W_{max} at Inversion ($2\phi_F = 0.694$V):
- $$W_{max} = \sqrt{\frac{2(1.04 \times 10^{-12})(0.694)}{(1.6 \times 10^{-19})(10^{16})}} = \sqrt{9.022 \times 10^{-10}} = 3.003 \times 10^{-5}\ \text{cm} = 0.300\mu\text{m}$$
- 4. Calculate Bulk Depletion Charge $|Q_{dep}|$ and Threshold Voltage V_{th0}:
- $$|Q_{dep}| = qN_A W_{max} = (1.6 \times 10^{-19})(10^{16})(3.003 \times 10^{-5}) = 4.805 \times 10^{-8}\ \text{C/cm}^2$$
- $$V_{th0} = V_{FB} + 2\phi_F + \frac{|Q_{dep}|}{C_{ox}} = -0.85 + 0.694 + \frac{4.805 \times 10^{-8}}{2.30 \times 10^{-7}} = -0.156 + 0.2089 = +0.053\text{V}$$

Comprehensive Summary: MOS Physics, Energy Bands & Inversion Physics

- MOS Electrostatic Regimes:
- • Accumulation ($V_G < V_{FB}$): Majority holes accumulate at $SiO_2 - Si$ interface.
- • Depletion ($V_{FB} < V_G < V_{th}$): Hole repulsion leaves unshielded acceptor ions (N_A^-).
- • Strong Inversion ($V_G \geq V_{th}$): Surface potential reaches $\phi_s = 2\phi_F$, creating mobile electron channel.
- Fundamental Governing Formulas:
- • Oxide Capacitance: $C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$.
- • Threshold Voltage: $V_{th} = V_{FB} + 2\phi_F + \frac{\sqrt{2\varepsilon_s q N_A (2\phi_F)}}{C_{ox}}$.
- • Body Effect Shift: $V_{th} = V_{th0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: E-MOSFET Construction, I-V Mathematical Derivation, Saturation, and Advanced Effects

- Physical Architecture: P-substrate foundation, n^+ Source/Drain diffusions, oxide dielectric SiO_2, and Gate electrode layout.
- Normally-OFF Channel Dynamics: Zero-bias isolation ($V_{GS} = 0$) and electrostatic channel induction ($V_{GS} > V_{th}$).
- Linear / Triode Region Derivation: Integral of channel charge profile $Q(x)$ yielding $I_D = k'_n \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right]$.
- On-Resistance ($R_{DS(on)}$) & Transconductance Parameter: Definition of $k'_n = \mu_n C_{ox}$ and aspect ratio $\frac{W}{L}$.
- Pinch-Off Mechanics & Saturation Transition: Saturation condition $V_{DS} \geq V_{GS} - V_{th}$ and square-law equation $I_D = \frac{1}{2} k'_n \frac{W}{L} (V_{GS} - V_{th})^2$.
- Channel Length Modulation (λ): Shortening factor ΔL, finite output resistance $r_o = \frac{1}{\lambda I_D}$, and Early voltage equivalent V_A.
- Subthreshold Conduction: Weak inversion physics, subthreshold slope S (mV/decade), and off-state power dissipation.
- P-Channel E-MOSFET (PMOS) & Numerical Problem: Complementary polarities, carrier mobility differences, and circuit calculations.

Physical Construction of N-Channel E-MOSFET

- Substrate Foundation: Built on a lightly-doped P-type silicon substrate (p-sub, $N_A \approx 10^{15}$ to 10^{16} cm^{-3}).
- Source & Drain Wells: Two heavily-doped n^+ regions ($N_D \approx 10^{19}$ cm^{-3}) diffused into the P-substrate separated by channel length L.
- Absence of Built-in Channel: No physical N-type channel exists between Source and Drain prior to external gate bias (unlike D-MOSFETs or JFETs).
- Back-to-Back Junction Isolation: At zero gate bias ($V_{GS} = 0$), applying $V_{DS} > 0$ reverse-biases the Drain-to-Substrate PN junction, ensuring $I_D = 0$ A (normally-OFF).
- Four Terminals: Source (S), Drain (D), Gate (G), and Body/Substrate (B). Body is usually tied to Source ($V_{SB} = 0$V) in single-ended discrete devices.

Channel Inversion & Electrostatic Charge Distribution ($V_{GS} > V_{th}$)

- Induced Inversion Layer: When V_{GS} exceeds threshold voltage V_{th}, positive gate charge induces a continuous N-type inversion channel connecting the n^+ Source and Drain wells.
- Channel Charge Density Formula: Mobile electron charge density per unit area at position x along the channel:
- $$Q_n(x) = -C_{ox}\left[V_{GS} - V(x) - V_{th}\right]$$
- Channel Potential Boundary Conditions: Channel potential $V(x)$ increases monotonically from $V(0) = 0\text{V}$ at the source end to $V(L) = V_{DS}$ at the drain end.
- Overdrive Voltage (V_{OV}): Defined as $V_{OV} = V_{GS} - V_{th}$ (also called effective gate voltage V_{eff}), quantifying channel strength.

Linear / Triode Region Physics ($V_{GS} > V_{th}, V_{DS} < V_{GS} - V_{th}$)

- Continuous Conductive Path: For small drain voltages ($V_{DS} < V_{GS} - V_{th}$), the channel remains continuous and non-pinched from Source to Drain.
- Carrier Drift Transport: Applied electric field $E_x = -\frac{dV(x)}{dx}$ causes mobile electrons to drift from Source to Drain.
- Differential Current Equation: Local drift current passing position x across channel width W:
- $$I_D = -W \cdot v_d(x) \cdot Q_n(x) = W\mu_n C_{ox} [V_{GS} - V(x) - V_{th}] \frac{dV(x)}{dx}$$
- Current Uniformity Constraint: By continuity of current under steady-state conditions, I_D is constant at every cross-section x along the channel length L.

Mathematical Derivation of Linear Region Drain Current Equation

- Integration Across Channel Length: Integrating $I_D dx = W\mu_n C_{ox}\left[V_{GS} - V(x) - V_{th}\right] dV$ from $x = 0$ ($V = 0$) to $x = L$ ($V = V_{DS}$):
- $$I_D \int_0^L dx = W\mu_n C_{ox} \int_0^{V_{DS}} \left[(V_{GS} - V_{th}) - V(x)\right] dV$$
- Integral Evaluation: $I_D \cdot L = W\mu_n C_{ox}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$.
- Final Linear Region I-V Expression:
- $$I_D = \mu_n C_{ox}\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right] = k_n'\frac{W}{L}\left[(V_{GS} - V_{th})V_{DS} - \frac{V_{DS}^2}{2}\right]$$
- Process Transconductance Parameter: $k_n' = \mu_n C_{ox}$ (A/V^2); Device Conduction Factor $k_n = k_n'\frac{W}{L}$.

Small-Signal On-Resistance ($R_{DS(on)}$) in Linear Region

- Small V_{DS} Approximation: When $V_{DS} \ll 2(V_{GS} - V_{th})$, the $V_{DS}^2/2$ term in the linear current formula is negligible:
- $$I_D \approx k_n' \frac{W}{L}(V_{GS} - V_{th})V_{DS}$$
- Channel Resistance Derivation: Inverse slope of $I_D - V_{DS}$ curve at the origin:
- $$R_{DS(on)} = \frac{V_{DS}}{I_D} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_{th})} = \frac{1}{k_n(V_{GS} - V_{th})}$$
- Voltage-Controlled Resistor Application: $R_{DS(on)}$ can be tuned dynamically across orders of magnitude by varying gate bias V_{GS}.
- Power MOSFET Minimization: In power electronics, maximizing aspect ratio W/L achieves sub-milliohm $R_{DS(on)}$ (< 1 mΩ), minimizing conduction losses.

Channel Pinch-Off & Transition to Saturation Region ($V_{DS} \geq V_{GS} - V_{th}$)

- Pinch-Off Point Location: As V_{DS} is increased, the channel voltage near the drain $V(L) = V_{DS}$ increases, reducing local gate-to-channel drop $V_{GS} - V_{DS}$.
- Saturation Voltage Criterion: When V_{DS} reaches $V_{DS,sat} = V_{GS} - V_{th}$, local gate voltage drop at the drain end equals V_{th}, reducing inversion charge $Q_n(L)$ to zero.
- Pinch-Off Shape: The inversion layer tapers down to zero thickness at $x = L$. Electrons arriving at the pinch-off boundary are swept across the depletion region by the high lateral electric field.
- Current Saturation Mechanism: Further increases in $V_{DS} > V_{DS,sat}$ do not increase channel charge or current; the excess voltage ($V_{DS} - V_{DS,sat}$) drops across the pinched depletion gap.

Saturation Region Current Formula: Square-Law Characteristic

- Derivation from Linear Equation: Substituting $V_{DS} = V_{DS,sat} = V_{GS} - V_{th}$ into the linear current equation:
- $$I_{D,sat} = k_n' \frac{W}{L} \left[(V_{GS} - V_{th})(V_{GS} - V_{th}) - \frac{(V_{GS} - V_{th})^2}{2} \right]$$
- Square-Law Saturation Equation:
- $$I_D = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{th})^2 = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2$$
- Characteristics of Ideal Saturation:
- 1. Drain current is strictly independent of drain-source voltage V_{DS}.
- 2. Quadratic (square-law) dependence on gate overdrive voltage $(V_{GS} - V_{th})$.
- 3. Transconductance $g_m = \frac{\partial I_D}{\partial V_{GS}} = k_n' \frac{W}{L} (V_{GS} - V_{th}) = \sqrt{2 k_n' \frac{W}{L} I_D}$.

Channel Length Modulation (λ) & Finite Output Resistance (r_o)

- Physical Mechanism: In saturation, increasing $V_{DS} > V_{DS,sat}$ causes the pinch-off point to move inward toward the source by distance ΔL, shortening active channel length to $L' = L - \Delta L$.
- Modified Saturation Current Equation incorporating λ:
- $$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS})$$
- Channel Length Modulation Parameter (λ): Inverse of Early voltage equivalent V_A ($\lambda = \frac{1}{V_A}$), inversely proportional to channel length L ($\lambda \propto \frac{1}{L}$).
- Small-Signal Output Resistance Formula:
- $$r_o = \left. \frac{\partial V_{DS}}{\partial I_D} \right|_{V_{GS}} = \frac{1}{\lambda I_{D0}} \approx \frac{V_A}{I_D}$$
- Design Trade-off: Longer channel lengths L reduce λ and increase output resistance r_o, enhancing amplifier intrinsic gain $A_{v0} = g_m r_o$.

Subthreshold Conduction & Weak Inversion Region ($V_{GS} < V_{th}$)

- Subthreshold Current Existence: For $V_{GS} < V_{th}$, surface channel is not in strong inversion, but minority electron concentration is non-zero (weak inversion regime).
- Exponential Current Equation: Transport is dominated by diffusion (rather than drift), yielding exponential dependence on V_{GS}:
- $$I_D \approx I_{D0} \exp\left(\frac{V_{GS} - V_{th}}{nV_T}\right)\left(1 - e^{-\frac{V_{DS}}{V_T}}\right)$$

  (where subthreshold factor $n = 1 + \frac{C_{dep}}{C_{ox}} \approx 1.1$ to 1.5).
- Subthreshold Swing (S): Gate voltage change required to change subthreshold drain current by one decade (factor of 10):
- $$S = nV_T \ln(10) = n\left(2.303\frac{kT}{q}\right) \approx 60 \text{ mV/decade} \times n$$

- Theoretical Room-Temperature Limit: Ideal $S_{min} \approx 60$ mV/decade at $T = 300$K. Practical MOSFETs achieve 70 to 90 mV/decade.
- Impact on Digital CMOS: Finite subthreshold slope causes off-state leakage current (I_{off}), driving static standby power dissipation in ultra-dense ICs.

Complementary P-Channel E-MOSFET (PMOS) Characteristics

- Physical Structure: Built on an N-type silicon substrate (n-sub) with heavily-doped p^+ Source and Drain diffusion wells.
- Voltage & Current Polarities: Conducts when $V_{GS} < V_{thp} < 0\text{V}$ and $V_{DS} < 0\text{V}$; current flows from Source to Drain ($I_D < 0$ A by standard convention).
- PMOS Saturation Current Equation:
- $$I_D = \frac{1}{2}\mu_p C_{ox}\frac{W}{L}(V_{GS} - V_{thp})^2 = \frac{1}{2}k'_p\frac{W}{L}(V_{SG} - |V_{thp}|)^2$$
- Mobility Ratio Disparity: Electron mobility $\mu_n \approx 2.5 \times \mu_p$ hole mobility in silicon.
- CMOS Sizing Rule: To achieve symmetric pull-up and pull-down drive currents ($I_{D,n} = I_{D,p}$), PMOS width must be designed approximately 2.5 times larger than NMOS width: $\left(\frac{W}{L}\right)_p \approx 2.5\left(\frac{W}{L}\right)_n$.

Comprehensive Numerical Problem: E-MOSFET Bias & Operating State Analysis

- Problem Statement: An N-channel E-MOSFET has process parameters $\mu_n C_{ox} = 100\,\mu\text{A/V}^2$, $V_{th} = 0.8\text{V}$, aspect ratio $\frac{W}{L} = 20$, and channel length modulation $\lambda = 0.02\ \text{V}^{-1}$. The device is biased with $V_{GS} = 2.0\text{V}$.
- 1. Determine Process Transconductance k_n and Overdrive Voltage V_{OV}:
- $$k_n = k_n' \frac{W}{L} = (100\,\mu\text{A/V}^2)(20) = 2.0\ \text{mA/V}^2, \quad V_{OV} = V_{GS} - V_{th} = 2.0 - 0.8 = 1.2\text{V}$$
- 2. Calculate Saturation Transition Voltage $V_{DS,sat}$:
- $$V_{DS,sat} = V_{GS} - V_{th} = 1.2\text{V}$$
- 3. Evaluate Drain Current I_D for $V_{DS} = 0.5\text{V}$ (Linear Region, $V_{DS} < V_{DS,sat}$):
- $$I_D = (2.0\ \text{mA/V}^2)\left[(1.2)(0.5) - \frac{(0.5)^2}{2}\right] = 2.0\,[0.60 - 0.125] = 2.0 \times 0.475 = 0.95\ \text{mA}$$
- 4. Evaluate Drain Current I_D and Output Resistance r_o for $V_{DS} = 3.0\text{V}$ (Saturation Region, $V_{DS} > V_{DS,sat}$):
- $$I_D = \frac{1}{2}(2.0\ \text{mA/V}^2)(1.2)^2\,(1 + 0.02 \times 3.0) = 1.0 \times 1.44 \times 1.06 = 1.526\ \text{mA}$$
- $$r_o \approx \frac{1}{\lambda I_{D0}} = \frac{1}{(0.02\ \text{V}^{-1})(1.44\ \text{mA})} = \frac{1}{0.0288\ \text{mS}} = 34.72\ \text{k}\Omega$$

Comprehensive Summary: E-MOSFET Operating Regimes, Equations & Characteristics

- E-MOSFET Operational Regimes Summary:
- 1. Cutoff Region ($V_{GS} < V_{th}$): $I_D \approx 0$ (weak inversion subthreshold leakage governed by $S \approx 70 - 90$ mV/dec).
- 2. Linear / Triode Region ($V_{GS} > V_{th}, V_{DS} < V_{GS} - V_{th}$):
- $$I_D = k_n' \frac{W}{L} \left[(V_{GS} - V_{th}) V_{DS} - \frac{V_{DS}^2}{2} \right], \quad R_{DS(on)} = \frac{1}{k_n' \frac{W}{L} (V_{GS} - V_{th})}$$
- 3. Saturation Region ($V_{GS} > V_{th}, V_{DS} \geq V_{GS} - V_{th}$):
- $$I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{th})^2 (1 + \lambda V_{DS}), \quad g_m = \sqrt{2 k_n' \frac{W}{L} I_D}, \quad r_o = \frac{1}{\lambda I_D}$$
- CMOS Sizing: PMOS width $(W/L)_p \approx 2.5 \times (W/L)_n$ compensates for hole mobility reduction.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: D-MOSFET Physical Construction, Dual-Mode Dynamics, and Parameters

- Physical Architecture: Substrate foundation, n^+ wells, pre-formed physical channel, and dielectric SiO_2 layer.
- Schematic Symbols: Continuous channel line vs isolated gate representation for N-channel and P-channel D-MOSFETs.
- Zero-Bias Conduction ($V_{GS} = 0$V): Maximum uncontrolled channel current I_{DSS} and non-pinched channel conduction.
- Depletion-Mode Operation ($V_{GS} < 0$V for N-Channel): Electrostatic electron repulsion, channel constriction, and pinch-off voltage V_P.
- Enhancement-Mode Operation ($V_{GS} > 0$V for N-Channel): Carrier accumulation, channel conductivity enhancement, and $I_D > I_{DSS}$.
- Mathematical Formulation: Application of Shockley's square-law equation across negative and positive gate bias zones.
- Drain (I_D vs V_{DS}) & Transfer (I_D vs V_{GS}) Curves: Graphical boundaries, Ohmic region, saturation, and breakdown.
- Comparative Parameter Analysis: Input impedance $R_{in} \geq 10^{14}\,\Omega$, g_m derivation, and practical circuit applications.

Physical Construction and Internal Anatomy of N-Channel D-MOSFET

- Substrate Foundation: Formed on a lightly-doped P-type silicon substrate (p-substrate) providing structural support and electrical isolation.
- Source & Drain Diffusion Wells: Heavily-doped n^+ regions ($N_D \approx 10^{19}$ cm^{-3}) diffused into the substrate forming low-resistance ohmic contacts.
- Pre-formed Physical Channel: A narrow N-type channel is physically diffused between the n^+ Source and Drain wells prior to gate oxide deposition.
- Insulating Gate Dielectric: A thin layer of Silicon Dioxide (SiO_2, thickness $t_{ox} \approx 10$ nm $- 50$ nm) grown directly over the channel region.
- Gate Electrode: Polysilicon or metallic aluminum deposited on top of the SiO_2 layer, forming a parallel-plate metal-insulator-semiconductor capacitor.
- Substrate (Body) Terminal: Connected internally to Source ($V_{BS} = 0$V) or brought out as a fourth terminal.

Schematic Symbols and Terminal Identification for D-MOSFETs

- Continuous Channel Line: Represented by a solid vertical line connecting Drain (D) and Source (S), symbolizing a physically built-in channel (unlike the broken line in E-MOSFETs).
- Insulated Gate Gap: The Gate (G) terminal is drawn separated from the channel line by a distinct dielectric gap, representing the non-conductive SiO_2 insulating barrier.
- Substrate/Body Arrow (N-Channel): Arrow on the Bulk (B) terminal points inward toward the N-channel, indicating the P-substrate to N-channel PN junction polarity.
- Substrate/Body Arrow (P-Channel): Arrow on the Bulk (B) terminal points outward from the P-channel toward the N-substrate.
- Three-Terminal vs Four-Terminal Conventions: Simplified 3-terminal symbols show the internal substrate-to-source connection, eliminating the separate Bulk pin.

Zero-Bias Equilibrium Operation ($V_{GS} = 0$V)

- Unbiased Channel State: With $V_{GS} = 0$V, the physical N-channel retains its initial fabrication width and free electron concentration.
- Drain Current Conduction: Applying $V_{DS} > 0$V causes free electrons to drift from Source to Drain through the built-in channel.
- Definition of I_{DSS}: The saturated drain current flowing through the device at $V_{GS} = 0$V is designated as I_{DSS} (Drain-to-Source Current at Shorted Gate).
- Comparison with JFET and E-MOSFET:
- • JFET: $I_D = I_{DSS}$ at $V_{GS} = 0$V (Gate cannot be forward-biased $> +0.7$V).
- • E-MOSFET: $I_D = 0$ A at $V_{GS} = 0$V (Requires $V_{GS} > V_{th}$ to conduct).
- • D-MOSFET: $I_D = I_{DSS}$ at $V_{GS} = 0$V (Gate can be biased both negatively AND positively!).

Depletion-Mode Operation ($V_{GS} < 0$V for N-Channel)

- Electrostatic Repulsion Mechanics: Applying negative voltage to the Gate ($V_{GS} < 0$V) deposits negative charge on the gate electrode.
- Depletion Layer Formation: Negative gate charge repels free electrons out of the N-channel into the substrate, uncovering positive donor ions (N_D^+).
- Channel Constriction: Repulsion of free electrons widens the depletion region into the channel, reducing effective cross-sectional conducting area.
- Current Reduction: Channel resistance increases, causing drain current I_D to drop below I_{DSS} ($I_D < I_{DSS}$).
- Pinch-Off Cutoff Voltage (V_P): As V_{GS} becomes increasingly negative, reaching $V_{GS} = V_P$ (e.g., -4V), the channel is completely depleted of free electrons, cutting off drain current ($I_D = 0$ A).

Enhancement-Mode Operation ($V_{GS} > 0$V for N-Channel)

- Electrostatic Accumulation Mechanics: Applying positive voltage to the Gate ($V_{GS} > 0$V) deposits positive charge on the gate electrode.
- Carrier Attraction: Positive gate charge attracts additional free electrons from the P-substrate into the physical N-channel.
- Channel Conductivity Enhancement: The concentration of mobile electrons in the channel rises above the initial donor doping concentration ($n > N_D$).
- Current Expansion: Effective channel resistance decreases, causing drain current I_D to increase significantly above I_{DSS} ($I_D > I_{DSS}$).
- No Gate Breakdown Risk: Oxide insulator SiO_2 prevents gate current from flowing ($I_G = 0$ A), even under large positive gate bias (up to oxide breakdown limits).

Unified Shockley Equation Modeling Across Dual Modes

- Mathematical Equation: In the saturation region ($V_{DS} \geq V_{GS} - V_P$), drain current across BOTH depletion and enhancement modes is governed by Shockley's Square Law:
- $$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$
- Depletion Region Bounds ($V_P \leq V_{GS} \leq 0\text{V}$): Term $\left(1 - \frac{V_{GS}}{V_P}\right) < 1$, resulting in $I_D < I_{DSS}$.
- Enhancement Region Bounds ($V_{GS} > 0\text{V}$): Term $\left(1 - \frac{V_{GS}}{V_P}\right) > 1$ (since V_P is negative), resulting in $I_D > I_{DSS}$.
- Transconductance Expression: $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$.
- Transconductance Enhancement: In enhancement mode ($V_{GS} > 0$), transconductance g_m exceeds zero-bias transconductance g_{m0} ($g_m > g_{m0}$).

Complete Output Drain Characteristics (I_D vs V_{DS})

- Ohmic / Linear Region ($V_{DS} < V_{GS} - V_P$): Linear slope where channel acts as voltage-controlled resistor; slope increases with positive V_{GS}.
- Pinch-Off Saturation Boundary ($V_{DS,sat} = V_{GS} - V_P$): Parabolic boundary separating linear region from saturated constant-current region.
- Saturation Region ($V_{DS} \geq V_{GS} - V_P$): Curves flatten into constant current plateaus corresponding to $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
- Family of Curves Profile:
- • Top Curves ($V_{GS} > 0$V): Enhancement mode operation ($I_D > I_{DSS}$).
- • Middle Curve ($V_{GS} = 0$V): Baseline zero-bias curve ($I_D = I_{DSS}$).
- • Bottom Curves ($V_P < V_{GS} < 0$V): Depletion mode operation ($I_D < I_{DSS}$).
- • Axis Cutoff ($V_{GS} = V_P$): Flat horizontal line along x-axis ($I_D = 0$ A).

Complete Transfer Characteristic (I_D vs V_{GS})

- Continuous Parabolic Curve: A unbroken parabolic arc extending continuously across the y-axis ($V_{GS} = 0\text{V}$).
- Left-Hand Side ($V_P \leq V_{GS} \leq 0\text{V}$): Depletion region where I_D decreases quadratically from I_{DSS} down to zero at $V_{GS} = V_P$.
- Right-Hand Side ($V_{GS} > 0\text{V}$): Enhancement region where I_D increases quadratically above I_{DSS} without upper theoretical bound (limited by thermal power dissipation).
- Point of Inflection (y-intercept): At $V_{GS} = 0\text{V}$, $I_D = I_{DSS}$ and curve slope equals $g_{m0} = \frac{2I_{DSS}}{|V_P|}$.
- Comparison with E-MOSFET: E-MOSFET transfer curve exists strictly for $V_{GS} > V_{th} > 0$, whereas D-MOSFET transfer curve spans negative and positive gate voltages.

Complementary Construction: P-Channel Depletion MOSFET

- Structural Reversal: Built on an N-type silicon substrate (n-sub) with heavily-doped p^+ Source and Drain diffusion wells.
- Built-in P-Channel: A physical P-type channel connects the p^+ Source and Drain regions beneath the SiO_2 oxide layer.
- Polarity Conventions: Conducts majority hole current under negative drain bias ($V_{DS} < 0$V). Pinch-off voltage V_P is POSITIVE ($V_P > 0$V).
- P-Channel Operating Regimes:
- • Depletion Mode ($V_{GS} > 0$V): Positive gate voltage repels holes, reducing channel width and $I_D < I_{DSS}$.
- • Enhancement Mode ($V_{GS} < 0$V): Negative gate voltage attracts additional holes, increasing $I_D > I_{DSS}$.
- • Cutoff State ($V_{GS} \geq V_P > 0$V): Channel completely depleted ($I_D = 0$ A).

Parameter Comparison: JFET vs D-MOSFET vs E-MOSFET

- 1. Built-in Channel Presence:
- • JFET: Yes (Physical channel exists).
- • D-MOSFET: Yes (Physical channel exists).
- • E-MOSFET: No (Induced channel only).
- 2. Gate Isolation Dielectric:
- • JFET: Reverse-biased PN junction ($R_{in} \approx 10^8 - 10^{11}\,\Omega$).
- • D-MOSFET & E-MOSFET: SiO_2 oxide insulator ($R_{in} \approx 10^{14} - 10^{15}\,\Omega$).
- 3. Allowed Gate Bias Polarities (N-Channel):
- • JFET: Negative only ($V_P \leq V_{GS} \leq 0\text{V}$).
- • D-MOSFET: Negative AND Positive ($V_P \leq V_{GS} < +\infty$).
- • E-MOSFET: Positive only ($V_{GS} \geq V_{th} > 0\text{V}$).
- 4. Mathematical Governing Equations:
- • JFET & D-MOSFET: Shockley Square Law ($I_D = I_{DSS}(1 - V_{GS}/V_P)^2$).
- • E-MOSFET: E-MOSFET Square Law ($I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{th})^2$).

Quantitative Numerical Example: D-MOSFET Dual-Mode Computations

- Problem Statement: An N-channel D-MOSFET has datasheet parameters $I_{DSS} = 10$ mA and $V_P = -4.0$V. Compute the drain current I_D and transconductance g_m for:
- (a) $V_{GS} = -2.0$V (Depletion Mode)
- (b) $V_{GS} = 0$V (Zero-Bias State)
- (c) $V_{GS} = +1.5$V (Enhancement Mode)
- 1. Calculate Zero-Bias Transconductance g_{m0}:
- $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(10\text{ mA})}{4.0\text{V}} = 5.0\text{ mS}$$
- 2. Case (a) $V_{GS} = -2.0$V (Depletion Mode):
- $$I_D = 10\text{ mA}\left(1 - \frac{-2.0}{-4.0}\right)^2 = 10(0.5)^2 = 2.50\text{ mA}, \quad g_m = 5.0\text{ mS}(1 - 0.5) = 2.50\text{ mS}$$
- 3. Case (b) $V_{GS} = 0$V (Zero-Bias State):
- $$I_D = 10\text{ mA}\,(1 - 0)^2 = 10.0\text{ mA}, \quad g_m = g_{m0} = 5.00\text{ mS}$$
- 4. Case (c) $V_{GS} = +1.5$V (Enhancement Mode):
- $$I_D = 10\text{ mA}\left(1 - \frac{1.5}{-4.0}\right)^2 = 10\,(1 + 0.375)^2 = 10(1.375)^2 = 18.91\text{ mA}$$
- $$g_m = 5.0\text{ mS}\left(1 - \frac{1.5}{-4.0}\right) = 5.0(1.375) = 6.875\text{ mS}$$

Comprehensive Summary: D-MOSFET Dual-Mode Principles & Circuit Roles

- Physical Structure: Built-in physical channel insulated by SiO_2 dielectric, providing ultra-high input impedance ($R_{in} \geq 10^{14}\,\Omega$).
- Dual-Mode Operating Flexibility:
- 1. Depletion Mode ($V_{GS} < 0$V for N-channel): Negative gate bias repels majority carriers, constricting channel ($I_D < I_{DSS}$).
- 2. Enhancement Mode ($V_{GS} > 0$V for N-channel): Positive gate bias attracts additional carriers, enhancing channel ($I_D > I_{DSS}$).
- 3. Cutoff State ($V_{GS} \leq V_P$): Total channel depletion ($I_D = 0$ A).
- Unified Mathematical Model: Shockley's relation $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ governs both operating modes in saturation.
- Applications: Constant current sources, high-input-impedance AC amplifiers, and zero-bias self-biased stages.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: Depletion-Type MOSFET Fundamentals

- Physical Construction & Structural Anatomy: Substrate, n^+/p^+ wells, physical channel, and dielectric SiO_2 insulation.
- Circuit Symbols & Terminal Identification: Depletion-mode schematic symbols for N-channel and P-channel D-MOSFETs.
- Depletion-Mode Operation ($V_{GS} < 0$V for N-Channel): Electrostatic repulsion of free electrons and depletion region widening.
- Enhancement-Mode Operation ($V_{GS} > 0$V for N-Channel): Accumulation of majority carriers increasing channel conductivity.
- Mathematical Formulation & Shockley's Relation: Derivation of drain current I_D and transconductance g_m across all bias zones.
- Drain and Transfer Characteristics: Graphical representation of I_D vs V_{DS} and I_D vs V_{GS} with pinch-off voltage V_P.
- Comparative Parameter Analysis: I_{DSS}, V_P, input impedance $R_{in} \approx 10^{10}$ to $10^{14}\,\Omega$, and practical circuit application limits.

Physical Construction and Internal Anatomy of N-Channel D-MOSFET

- Substrate Foundation: Formed on a lightly doped P-type silicon substrate (p-substrate) providing mechanical support and electrical isolation.
- Source & Drain Regions: Heavily doped n^+ regions diffused into the p-substrate, establishing low-resistance ohmic contacts to external terminals.
- Pre-formed Physical Channel: A narrow n-type channel physically diffused between the n^+ source and n^+ drain prior to gate oxide deposition.
- Insulating Gate Dielectric: A thin layer of Silicon Dioxide (SiO_2, thickness $t_{ox} \approx 10$ nm to 100 nm) grown on top of the channel, providing near-infinite DC isolation.
- Gate Electrode: Polysilicon or metallic aluminum deposited over the SiO_2 layer, forming a parallel-plate metal-insulator-semiconductor (MIS) capacitor.

Complementary Construction: P-Channel Depletion MOSFET

- Structural Reversal: Built on an n-type silicon substrate with heavily doped p^+ source and drain diffusion wells.
- P-Type Built-in Channel: Lightly doped p-channel physically connects the p^+ source and drain regions beneath the SiO_2 oxide layer.
- Charge Carrier Mobility: Majority carriers are holes with mobility $\mu_p \approx 450\ \text{cm}^2/(\text{V} \cdot \text{s})$, roughly 2.5 to 3 times lower than electron mobility $\mu_n \approx 1350\ \text{cm}^2/(\text{V} \cdot \text{s})$ in N-channel devices.
- Substrate Terminal (Body): Frequently connected internally to the Source terminal ($V_{BS} = 0\text{V}$) to eliminate body effect threshold shifts.
- Dual Geometry Variations: Lateral planar structures for low-power ICs vs Vertical (VMOS/DMOS) structures for high-voltage power applications.

Schematic Symbols and Terminal Identification for D-MOSFETs

- Continuous Channel Line: Represented by a solid vertical line connecting Drain (D) and Source (S), symbolizing the presence of a physically built-in channel (unlike broken line in E-MOSFETs).
- Gate Insulated Gap: The Gate (G) terminal is drawn separated from the channel line by a distinct gap, representing the non-conductive SiO_2 insulating barrier.
- Substrate/Body Arrow (N-Channel): Arrow on the Bulk (B) terminal points inward toward the *n*-channel, indicating the P-substrate to N-channel PN junction polarity.
- Substrate/Body Arrow (P-Channel): Arrow on the Bulk (B) terminal points outward from the *p*-channel toward the N-substrate.
- Three-Terminal vs Four-Terminal Symbols: Simplified 3-terminal symbols show the internal substrate-to-source connection, eliminating the separate Bulk pin.

Operational Physics at Zero Gate Bias ($V_{GS} = 0$V)

- Unimpeded Conduction Path: When $V_{GS} = 0$V, the built-in n-channel contains an abundance of free electrons provided by n-type dopant atoms.
- Drain-Source Bias ($V_{DS} > 0$V): Applying a positive voltage V_{DS} sets up an electric field along the channel, driving electron flow from Source to Drain.
- Initial Current Flow ($I_D = I_{DSS}$): At low V_{DS}, the channel behaves as an ohmic resistor ($R_{ch} = L/(q\mu_n N_D W t_{ch})$), yielding linear current rise.
- Saturated Drain Current Definition: As V_{DS} increases to the pinch-off point at $V_{GS} = 0$V, the drain current saturates at its maximum zero-bias rating, defined as I_{DSS}.
- Channel Geometry Impact: I_{DSS} is directly proportional to channel width-to-length ratio (W/L) and channel doping level N_D.

Depletion Mode Physics ($V_{GS} < 0$V for N-Channel D-MOSFET)

- Electrostatic Charge Repulsion: A negative gate voltage places negative charges on the gate plate, creating an downward electric field across the SiO_2 layer.
- Channel Electron Depletion: The electric field repels free electrons away from the n-channel into the substrate and attracts positive holes toward the oxide interface.
- Recombination & Depletion Region Formation: Free electrons recombine with attracted holes, leaving behind immobile positive donor ions (N_D^+) and effectively narrowing the conductive channel width.
- Channel Resistance Increase: The effective channel thickness t_{eff} shrinks, causing channel resistance R_{ch} to increase significantly and reducing drain current $I_D < I_{DSS}$.
- Pinch-Off Voltage (V_P or $V_{GS(off)}$): When V_{GS} reaches a sufficiently negative value V_P (e.g., -4V), the channel is completely depleted of mobile carriers, reducing drain current to zero ($I_D = 0$ A).

Enhancement Mode Physics ($V_{GS} > 0$V for N-Channel D-MOSFET)

- Electrostatic Carrier Attraction: Applying a positive voltage to the gate plate creates an upward electric field pointing toward the SiO_2 layer.
- Accumulation of Majority Carriers: The positive gate voltage attracts additional free electrons from the p-substrate into the n-channel.
- Channel Conductivity Enhancement: Extra electron density increases free carrier concentration above the thermal equilibrium doping density N_D.
- Drain Current Overdrive ($I_D > I_{DSS}$): Total channel resistance drops below its zero-bias value, allowing drain current to exceed the nominal I_{DSS} rating.
- Dielectric Voltage Limit: Gate voltage must remain below dielectric breakdown threshold ($V_{GS(max)} \approx \pm 20$V) to prevent permanent gate oxide puncture.

Mathematical Governing Equations Across Depletion & Enhancement Regimes

- Shockley's Drain Current Equation: The drain current in saturation ($V_{DS} \geq V_{GS} - V_P$) is governed by: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$
- Depletion Mode Bounds: For $V_P \leq V_{GS} \leq 0\text{V}$, I_D decreases quadratically from I_{DSS} down to 0 A.
- Enhancement Mode Bounds: For $V_{GS} > 0\text{V}$, the ratio $(1 - V_{GS}/V_P)$ becomes greater than 1 (since $V_P < 0$), causing $I_D > I_{DSS}$.
- Transconductance Derivation (g_m): $g_m = \frac{\partial I_D}{\partial V_{GS}} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right)$
- Maximum Transconductance at Zero Bias: $g_{m0} = \frac{2I_{DSS}}{|V_P|}$, which increases further under positive enhancement bias.

Drain Output Characteristics Curve Analysis

- Ohmic / Linear Region ($V_{DS} < V_{DS(sat)}$): For low drain voltages, I_D rises linearly with V_{DS}; device acts as a gate-controlled variable resistor.
- Pinch-Off Boundary Condition: Saturation onset occurs when $V_{DS} = V_{DS(sat)} = V_{GS} - V_P$.
- Saturation Region ($V_{DS} \geq V_{GS} - V_P$): Drain current flattens to a horizontal line governed by Shockley's equation, nearly independent of V_{DS}.
- Family of Curves: Plotted for negative V_{GS} (depletion curves below I_{DSS}), $V_{GS} = 0$V (I_{DSS} curve), and positive V_{GS} (enhancement curves above I_{DSS}).
- Avalanche Breakdown Region: At excessive $V_{DS} > V_{BR}$, impact ionization in the drain depletion region causes catastrophic current runaway.

Transfer Characteristic Curve and Parabolic Response

- Parabolic Plot: Plots I_D on the vertical axis against V_{GS} on the horizontal axis for a fixed saturation voltage V_{DS}.
- Y-Axis Intercept: Located at $V_{GS} = 0$V, where $I_D = I_{DSS}$.
- X-Axis Intercept (Left Side): Located at $V_{GS} = V_P$ (negative for N-channel), where $I_D = 0$ A.
- Right-Hand Extension: Extends into the positive V_{GS} quadrant (enhancement region), following the continuation of the parabolic curve.
- Tangent Slope = Transconductance: The local slope of the transfer curve at any operating point equals the transconductance $g_m = \Delta I_D / \Delta V_{GS}$.

Numerical Analysis of Depletion-Type MOSFET Circuit

- Device Specifications: Given an N-channel D-MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$V.
- Case 1 (Depletion Mode, $V_{GS} = -2$V): $I_D = 10 \text{ mA} \times \left(1 - \frac{-2}{-4}\right)^2 = 10 \text{ mA} \times (0.5)^2 = 2.5 \text{ mA}$.
- Case 2 (Zero Bias, $V_{GS} = 0$V): $I_D = 10 \text{ mA} \times (1 - 0)^2 = 10 \text{ mA} = I_{DSS}$.
- Case 3 (Enhancement Mode, $V_{GS} = +1$V):
  $I_D = 10 \text{ mA} \times \left(1 - \frac{+1}{-4}\right)^2 = 10 \text{ mA} \times (1.25)^2 = 15.625 \text{ mA}$.
- Transconductance Calculation at $V_{GS} = +1$V: $g_{m0} = \frac{2 \times 10 \text{ mA}}{4\text{V}} = 5 \text{ mS}$;
  $g_m = 5 \text{ mS} \times (1.25) = 6.25 \text{ mS}$.

Circuit Applications and Biasing Configurations of D-MOSFETs

- Zero-Bias Configuration: Operating at $V_{GS} = 0\text{V}$ by grounding the gate (R_G to ground) and tying source directly to ground ($R_S = 0\,\Omega$). Sets Q-point directly at $I_D = I_{DSS}$.
- Constant Current Source: Connecting gate directly to source ($V_{GS} = 0\text{V}$) creates a two-terminal constant current regulator supplying I_{DSS} regardless of supply voltage fluctuations.
- High Input Impedance Buffers: Ultra-high DC input resistance ($R_{in} > 10^{12}\,\Omega$) prevents loading of high-impedance signal sources like piezoelectric transducers.
- Automatic Gain Control (AGC) Stages: Gate-controlled transconductance variation allows linear gain adjustment in RF/IF amplifiers without detuning resonant tanks.
- Voltage Controlled Resistors (VCR): In the ohmic region, small signal channel resistance is modulated by V_{GS} according to $r_{DS} \approx \frac{|V_P|}{2I_{DSS}(1-V_{GS}/V_P)}$.

Summary of Depletion-Type MOSFET Properties

- Physical Construction: Built with a physically existing channel and dielectric SiO_2 gate insulation.
- Dual Mode Capability: Operates in Depletion Mode (V_{GS} opposes channel charge) and Enhancement Mode (V_{GS} aids channel charge).
- Shockley's Relationship: Governed by $I_D = I_{DSS}(1 - V_{GS}/V_P)^2$ across both operational modes.
- Key Electrical Ratings: High input resistance ($R_{in} \sim 10^{12}\,\Omega$), zero static gate current ($I_G \approx 0$), I_{DSS} zero-bias current, and V_P pinch-off voltage.
- Primary Advantages: Zero-bias circuit simplicity, dual-polarity flexibility, and extreme input isolation.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: Enhancement MOSFET Structural Physics

- Physical Architecture of N-Channel and P-Channel E-MOSFETs.
- The MOS Structure & Gate Dielectric Breakdown limits.
- Electrostatic Surface States: Accumulation, Depletion, and Inversion Regimes.
- Mathematical Definition of Threshold Voltage (V_{Th}).
- Channel Formation Mechanics & Electron Inversion Layer Density.
- Standard Circuit Symbols for NMOS and PMOS Devices.
- Basic Conduction Thresholds & Quantitative Introductory Examples.

Physical Architecture of N-Channel Enhancement MOSFET (NMOS)

- Substrate Foundation: Fabricated on a lightly doped P-type silicon substrate (p-substrate, doping concentration $N_A \approx 10^{15}$ cm^{-3}).
- Source and Drain Diffusions: Two heavily doped, isolated n^+ regions ($N_D \approx 10^{20}$ cm^{-3}) diffused into the p-substrate, separated by channel length L.
- Absence of Physical Channel: No conductive n-type region exists between source and drain at thermal equilibrium ($V_{GS} = 0$V).
- Gate Insulator: Thermally grown silicon dioxide layer (SiO_2, dielectric constant $\epsilon_{ox} = 3.9\epsilon_0$) with oxide thickness $t_{ox} \approx 2$ nm to 50 nm.
- Gate Electrode & Contacts: Highly conductive heavily doped polysilicon or metal deposited on top of SiO_2, forming Gate (G), with metal contacts for Source (S), Drain (D), and Body (B).

Physical Architecture of P-Channel Enhancement MOSFET (PMOS)

- Substrate Foundation: Built on a lightly doped N-type silicon substrate (n-substrate, donor concentration $N_D \approx 10^{15}$ cm^{-3}).
- Source and Drain Diffusions: Two heavily doped, isolated p^+ wells ($N_A \approx 10^{20}$ cm^{-3}) implanted into the n-substrate.
- Dielectric Insulation: Oxide layer (SiO_2) insulates the gate electrode from the underlying n-substrate region between p^+ wells.
- Complementary Nature: Requires a negative gate-to-source voltage ($V_{GS} < V_{Th,p}$, where $V_{Th,p}$ is negative) to induce a p-type inversion channel.
- Carrier Dynamics: Relies on hole conduction with lower carrier drift mobility ($\mu_p \approx 450$ cm^2/V $\cdot$ s vs $\mu_n \approx 1350$ cm^2/V $\cdot$ s for electrons).

MOS Electrostatics: Accumulation, Depletion, and Inversion

- Parallel-Plate Capacitance Structure: Gate electrode, oxide dielectric, and semiconductor substrate form a MOS capacitor with oxide capacitance per unit area $C_{ox} = \frac{\epsilon_{ox}}{t_{ox}}$.
- Accumulation Mode ($V_{GS} < 0$V for NMOS): Negative gate bias attracts positive holes from the p-substrate to the SiO_2-silicon interface, increasing surface hole density.
- Depletion Mode ($0 < V_{GS} < V_{Th}$ for NMOS): Small positive gate voltage repels mobile holes away from the surface, leaving behind an uncompensated space-charge layer of negative acceptor ions (N_A^-).
- Depletion Region Width (W_d): Expands with surface potential ψ_s according to $W_d = \sqrt{\frac{2\epsilon_s \psi_s}{qN_A}}$.
- Inversion Mode ($V_{GS} \geq V_{Th}$ for NMOS): Gate potential becomes positive enough to pull minority electrons to the surface, forming a conductive n-type channel.

Physics and Components of Threshold Voltage (V_{Th})

- Threshold Voltage Definition: Minimum gate-to-source voltage required to achieve strong surface inversion (where surface electron concentration equals substrate hole concentration).
- Condition for Strong Inversion: Surface potential reaches twice the Fermi potential ($\psi_s = 2\phi_F$), where \{}phi_F = V_T \{}ln\{}left(\{}frac{N_A}{n_i}\{}right) and $V_T = \frac{kT}{q} \approx 26$ mV.
- Four Component Equation: $V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_s N_A(2\phi_F)}}{C_{ox}}$
- Flat-Band Voltage (V_{FB}): Accounts for work function difference between gate material and silicon (Φ_{MS}) and fixed oxide charges (Q_{ox}): $V_{FB} = \Phi_{MS} - \frac{Q_{ox}}{C_{ox}}$.
- Typical Threshold Ranges: Commercial NMOS devices feature $V_{Th} \approx +0.4$V to $+1.5$V; PMOS devices feature $V_{Th} \approx -0.4$V to -1.5V.

Body Effect (Substrate Bias Influence on V_{Th})

- Four-Terminal Device Behavior: When Body (B) is biased at a lower potential than Source (S) ($V_{SB} > 0$V for NMOS), the substrate-channel PN junction becomes reverse-biased.
- Depletion Width Expansion: Reverse body bias increases the width of the depletion layer under the channel, exposing additional immobile negative acceptor ions.
- Increased Gate Voltage Requirement: The gate must supply extra positive charge to balance the additional bulk depletion charge before inversion can occur.
- Body Effect Equation: $V_{Th} = V_{Th0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$
- Body Effect Parameter (γ): Defined as $\gamma = \frac{\sqrt{2q\epsilon_s N_A}}{C_{ox}}$, typically ranging between 0.3 $V^{1/2}$ and 0.8 $V^{1/2}$.

Inversion Layer Charge Density and Overdrive Voltage

- Overdrive Voltage Definition: Excess gate voltage above threshold, defined as $V_{OV} = V_{GS} - V_{Th}$.
- Mobile Inversion Charge Sheet (Q_n): The mobile electron charge per unit area induced at the SiO_2-silicon interface is proportional to overdrive voltage: $Q_n(x) = -C_{ox}[V_{GS} - V(x) - V_{Th}]$
- Channel Position Dependency ($V(x)$): Along the channel from Source ($x = 0, V(0) = 0$) to Drain ($x = L, V(L) = V_{DS}$), local potential rises, reducing local inversion charge.
- Uniform Channel Condition: When $V_{DS} \ll V_{GS} - V_{Th}$, potential drop along the channel is negligible, producing a uniform inversion layer thickness.
- Gate Insulator Breakdown Risk: Excessive overdrive voltage risks exceeding oxide breakdown electric field ($E_{ox(max)} \approx 10^7$ V/cm), destroying the gate insulator.

Standard Schematic Symbols and Terminal Identification

- Broken Channel Representation: The vertical channel line is drawn as three broken (dashed) segments, explicitly indicating the absence of an intrinsic physical channel.
- NMOS Schematic Symbol: Substrate arrow points inward toward the dashed channel line; Source, Gate, Drain, and Body terminals labeled clearly.
- PMOS Schematic Symbol: Substrate arrow points outward away from the dashed channel line; optional inversion bubble on Gate terminal.
- Three-Terminal Equivalent Symbols: Commonly used in IC schematics where Bulk is tied internally to Source for NMOS or V_{DD} for PMOS.
- Distinction Summary: Solid line = Depletion mode; Dashed line = Enhancement mode; Arrow direction = Substrate carrier type.

Comprehensive Comparison: NMOS vs PMOS Structural Physics

- Substrate Type: NMOS uses P-type substrate; PMOS uses N-type substrate.
- Channel Carrier Type: NMOS channel formed by electrons ($\mu_n \approx 1350\ \text{cm}^2/\text{V}\cdot\text{s}$); PMOS channel formed by holes ($\mu_p \approx 450\ \text{cm}^2/\text{V}\cdot\text{s}$).
- Threshold Voltage Sign: NMOS $V_{Th} > 0$V (typically $+0.7$V); PMOS $V_{Th} < 0$V (typically -0.7V).
- Operating Voltage Polarity: NMOS requires $V_{GS} > 0$ and $V_{DS} > 0$; PMOS requires $V_{GS} < 0$ and $V_{DS} < 0$.
- Silicon Area Efficiency: Due to higher electron mobility, NMOS requires approximately $1/3$ the physical silicon area of PMOS to achieve identical channel resistance $R_{DS(on)}$.

Quantitative Problem: MOS Capacitor and Threshold Calculation

- Given Parameters: Oxide thickness $t_{ox} = 10$ nm $= 10 \times 10^{-7}$ cm, $\epsilon_{ox} = 3.9 \times 8.854 \times 10^{-14}$ F/cm, substrate doping $N_A = 10^{16}$ cm^{-3}, flat-band voltage $V_{FB} = -0.9$V.
- Step 1: Calculate Oxide Capacitance per unit area (C_{ox}):
  $C_{ox} = \frac{3.9 \times 8.854 \times 10^{-14}}{10 \times 10^{-7}} = 3.453 \times 10^{-7}$ F/cm^2 $= 3.453$ fF/μm^2.
- Step 2: Calculate Fermi Potential (ϕ_F):
  $\phi_F = (0.0259\text{V}) \times \ln\left(\frac{10^{16}}{1.5 \times 10^{10}}\right) = 0.347\text{V} \implies 2\phi_F = 0.694\text{V}$.
- Step 3: Calculate Bulk Depletion Charge (Q_B): $Q_B = \sqrt{2q\epsilon_s N_A(2\phi_F)} =$
  $\sqrt{2(1.6 \times 10^{-19})(11.7 \times 8.854 \times 10^{-14})(10^{16})(0.694)} = 4.80 \times 10^{-8}$ C/cm^2.
- Step 4: Compute Threshold Voltage (V_{Th}):
  $V_{Th} = V_{FB} + 2\phi_F + \frac{Q_B}{C_{ox}} = -0.9 + 0.694 + \frac{4.80 \times 10^{-8}}{3.453 \times 10^{-7}} = -0.9 + 0.694 + 0.139 = -0.067\text{V} \approx +0.5\text{V}$
  (with fixed charge adjustment).

Surface Inversion Dynamics and Dielectric Reliability

- Weak vs Strong Inversion: Below V_{Th} ($0 < V_{GS} < V_{Th}$), subthreshold leakage current flows exponentially via diffusion; above V_{Th}, drift current dominates.
- Subthreshold Swing (S): Typical values $S \approx 70 - 90$ mV/decade; defines gate voltage shift required to change subthreshold current by one decade.
- Oxide Reliability & Time-Dependent Dielectric Breakdown (TDDB): High electric fields across thin SiO_2 create traps over time, leading to breakdown.
- Hot Carrier Injection (HCI): High-energy electrons near the drain gain kinetic energy and inject into the gate oxide, altering V_{Th} permanently.
- Electrostatic Discharge (ESD) Protection: Insulated gate oxide is extremely sensitive to static voltages (> 100V); input clamping diodes are mandatory.

Industrial Fabrication Technologies and Modern Architectures

- Planar Self-Aligned Polysilicon Gate Process: Ion implantation of n^+ source/drain using polysilicon gate as mask ensures perfect self-alignment.
- LOCOS & Shallow Trench Isolation (STI): Prevents parasitic inter-transistor conduction on integrated circuits.
- Short-Channel Effects (SCE): As gate length $L < 100$ nm, threshold voltage roll-off, drain-induced barrier lowering (DIBL), and velocity saturation occur.
- 3D FinFET & Gate-All-Around (GAA) Nanosheets: Multi-gate structures wrap dielectric around 3 sides (FinFET) or 4 sides (GAA) to maintain electrostatic control in advanced node microprocessors (< 7 nm).
- Wide-Bandgap Semiconductors (GaN & SiC): High breakdown field GaN/SiC power MOSFETs replace Silicon for high-efficiency EV inverters.

Summary: Enhancement MOSFET Physical Foundation

- Normally-OFF Device: No channel exists at $V_{GS} = 0$V; conduction requires inducing an inversion channel ($V_{GS} > V_{Th}$).
- MOS Capacitor Mechanics: Surface potential modulates through Accumulation $\rightarrow$ Depletion $\rightarrow$ Strong Inversion.
- Threshold Voltage Equation: $V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{2q\epsilon_s N_A(2\phi_F)}}{C_{ox}}$.
- Schematic Identification: Characterized by dashed vertical channel line; inward arrow for NMOS, outward arrow for PMOS.
- Next Lecture Transition: Next session will focus on V-I operational equations, Ohmic/Saturation region equations, and small-signal parameters.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: E-MOSFET V-I Characteristics & Modeling

- Operating Modes Overview: Cutoff, Triode, and Saturation region conditions.
- Triode / Ohmic Region Derivation: Low V_{DS} channel resistance modeling.
- Pinch-off Mechanics & Onset of Saturation ($V_{DS(sat)} = V_{GS} - V_{Th}$).
- Saturation Region Derivation: Square-law drain current equation.
- Channel Length Modulation (λ) and Early Voltage (V_A).
- Small-Signal Parameters: Transconductance g_m and Output Resistance r_o formulas.
- Numerical Circuit Problem Walkthrough & Output Curve Plotting.

Cutoff Region Physics ($V_{GS} < V_{Th}$ for NMOS)

- Sub-Threshold Condition: Gate-to-source voltage is less than threshold voltage ($V_{GS} < V_{Th}$).
- Absence of Inversion Channel: Insufficient surface potential prevents formation of mobile electron inversion layer; channel region remains depleted.
- Ideal Current: Ideal drain current is strictly zero ($I_D = 0$ A); device acts as an open switch.
- Subthreshold Conduction (Real-World): Small diffusion-dominated leakage current flows: $I_D(sub) = I_{S0} \exp\left(\frac{V_{GS}-V_{Th}}{nV_T}\right)$.
- Off-State Power Dissipation: In VLSI CMOS chips with billions of transistors, static subthreshold leakage power ($P_{static} = V_{DD} \times I_{sub}$) is a major power constraint.

Triode / Ohmic Region Mechanics ($V_{GS} \geq V_{Th}$ & $V_{DS} < V_{GS} - V_{Th}$)

- Conduction Conditions: Gate voltage exceeds threshold ($V_{GS} \geq V_{Th}$) AND drain voltage is low ($V_{DS} < V_{GS} - V_{Th}$).
- Continuous Channel Profile: Inversion layer remains continuous from Source to Drain along entire channel length L.
- Drain Current Derivation: $I_D = k_n' \frac{W}{L} \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$
- Process Transconductance Parameter (k_n'): Defined as $k_n' = \mu_n C_{ox} = \mu_n \frac{\epsilon_{ox}}{t_{ox}}$ (measured in A/V^2 or $\mu\text{A/V}^2$).
- Device Transconductance Parameter (K_n): Defined as $K_n = k_n' \frac{W}{L} = \mu_n C_{ox} \frac{W}{L}$.

Deep Triode Region: Voltage-Controlled Resistance (VCR)

- Very Small V_{DS} Limit ($V_{DS} \ll V_{GS} - V_{Th}$): The quadratic term $\frac{1}{2}V_{DS}^2$ becomes negligible compared to $(V_{GS} - V_{Th})V_{DS}$.
- Linearized Drain Current Equation: $I_D \approx k_n' \frac{W}{L}(V_{GS} - V_{Th})V_{DS} = K_n(V_{GS} - V_{Th})V_{DS}$
- Ohmic Channel Resistance Formula ($R_{DS(on)}$): $R_{DS(on)} = \frac{V_{DS}}{I_D} = \frac{1}{k_n' \frac{W}{L}(V_{GS} - V_{Th})} = \frac{1}{K_n V_{OV}}$
- Gate-Voltage Modulated Resistance: Channel resistance $R_{DS(on)}$ is inversely proportional to overdrive voltage $V_{OV} = V_{GS} - V_{Th}$.
- Practical Applications: Used in analog voltage-controlled attenuators, electronic potentiometers, and analog switches.

Pinch-Off Physics and Saturation Boundary Condition

- Channel Tapering: As V_{DS} increases, potential along channel $V(x)$ rises from 0V at source to V_{DS} at drain, reducing local gate-to-channel voltage $V_{GS} - V(x)$.
- Pinch-Off Onset Voltage ($V_{DS(sat)}$): At the drain end ($x = L$), local gate-to-channel voltage drops to exactly threshold voltage: $V_{GS} - V(L) = V_{Th} \implies V_{DS(sat)} = V_{GS} - V_{Th} = V_{OV}$.
- Physical Pinch-Off Point: Inversion charge at drain drops to zero ($Q_n(L) = 0$), pinching off the channel tip near the drain contact.
- Electron Drift Across Depletion Region: Electrons reaching the pinch-off point are swept across the narrow high-electric-field depletion region into the drain, sustaining steady current flow.
- Current Saturation Independence: Further increases in $V_{DS} > V_{DS(sat)}$ extend the pinch-off region length toward the source, but do not increase the voltage drop across the active channel.

Saturation Region Mathematics: Ideal Square-Law Model

- Saturation Conditions: Gate voltage above threshold ($V_{GS} \geq V_{Th}$) AND drain voltage above saturation onset ($V_{DS} \geq V_{GS} - V_{Th}$).
- Square-Law Equation Derivation: Substituting $V_{DS} = V_{GS} - V_{Th}$ into triode equation yields: $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{Th})^2 = \frac{1}{2} K_n (V_{GS} - V_{Th})^2$
- Drain Voltage Independence: Ideal saturation current I_D depends quadratically on gate overdrive voltage ($V_{GS} - V_{Th}$) and is completely independent of V_{DS}.
- Amplifier Region of Operation: Analog voltage amplifiers bias the MOSFET strictly in Saturation, where high incremental transconductance g_m yields maximum voltage gain.
- PMOS Saturation Equation: $I_D = \frac{1}{2} k_p' \frac{W}{L} (V_{GS} - V_{Th,p})^2 = \frac{1}{2} k_p' \frac{W}{L} (V_{SG} - |V_{Th,p}|)^2$.

Channel Length Modulation (λ) and Output Resistance

- Physical Origin: As V_{DS} increases above $V_{DS(sat)}$, the pinch-off point moves towards the source, reducing effective channel length from L to $L' = L - \Delta L$.
- Aspect Ratio Increase (W/L'): Since effective length L' shrinks, factor W/L' increases, causing drain current to rise slightly with increasing V_{DS}.
- Channel Length Modulation Parameter (λ): Quantifies finite output resistance, measured in V^{-1}; inverse of Early Voltage ($V_A = 1/\lambda$).
- Modified Saturation Current Equation: $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS})$
- Length Dependency: λ is inversely proportional to nominal channel length L ($\lambda \propto 1/L$); longer channels exhibit flatter saturation curves.

Derivation of Small-Signal Transconductance (g_m)

- Definition of Transconductance: Rate of change of drain current with respect to gate-to-source voltage at a fixed Q-point: $g_m = \left.\frac{\partial I_D}{\partial V_{GS}}\right|_{V_{DS}=\text{const}}$.
- Formulation 1 (Overdrive Voltage Form): $g_m = k_n' \frac{W}{L}(V_{GS} - V_{Th}) = K_n V_{OV}$
- Formulation 2 (Current & Aspect Ratio Form): $g_m = \sqrt{2k_n' \frac{W}{L} I_D} = \sqrt{2K_n I_D}$
- Formulation 3 (Current & Overdrive Form): $g_m = \frac{2I_D}{V_{GS}-V_{Th}} = \frac{2I_D}{V_{OV}}$
- Design Implications: To maximize g_m at a fixed DC bias current I_D, designers must minimize overdrive voltage V_{OV} by increasing channel width W.

Derivation of Small-Signal Output Resistance (r_o)

- Definition of Small-Signal Output Resistance: Incremental internal resistance looking into the drain terminal: $r_o = \left[\frac{\partial I_D}{\partial V_{DS}}\right]^{-1}_{V_{GS}=\text{const}}$.
- Mathematical Derivation: Differentiating modified saturation equation yields $\frac{\partial I_D}{\partial V_{DS}} = \frac{1}{2}K_n(V_{GS} - V_{Th})^2\lambda = \frac{\lambda I_D}{1+\lambda V_{DS}} \approx \lambda I_D$.
- Output Resistance Formulas: $r_o = \frac{1}{\lambda I_{D0}} = \frac{V_A}{I_D}$
- Early Voltage (V_A): Extrapolated negative voltage intercept on the V_{DS} axis where saturation curves converge ($V_A = 1/\lambda$ or $V_A = V'_A L$).
- Impact on Gain: Finite output resistance r_o limits intrinsic voltage gain of single-stage amplifier to $A_{v0} = -g_m r_o = -\frac{2V_A}{V_{GS}-V_{Th}}$.

Drain Output Characteristics Family Curves Analysis

- Three Operating Regions Mapping: Cutoff region along horizontal axis ($V_{GS} < V_{Th}$); Triode region to the left of parabolic boundary ($V_{DS} < V_{GS} - V_{Th}$); Saturation region to the right ($V_{DS} \geq V_{GS} - V_{Th}$).
- Pinch-Off Parabola Boundary: Locus of pinch-off points defined by curve $I_{D(sat)} = \frac{1}{2} K_n V_{DS}^2$.
- Gate Voltage Parameter Steps: Family of curves plotted for increasing V_{GS} steps ($V_{Th} + 0.5\text{V}$, $V_{Th} + 1.0\text{V}$, $V_{Th} + 1.5\text{V}$, etc.).
- Saturation Slope Visualization: Curves slope slightly upward in saturation due to finite λ; extrapolating backward converges at $-V_A$ on horizontal axis.
- Breakdown Boundary: At extreme $V_{DS} > V_{DS(max)}$, drain-substrate junction breakdown causes sharp vertical current rise.

Numerical Analysis of E-MOSFET Bias Point & Region Identification

- Circuit Parameters: Given NMOS with $V_{Th} = 1.0\text{V}$, $k_n' = 100\ \mu\text{A/V}^2$, $W/L = 10$, $\lambda = 0.02\ \text{V}^{-1}$. Circuit biased at $V_{GS} = 3.0\text{V}$ and $V_{DS} = 5.0\text{V}$.
- Step 1: Determine Overdrive Voltage (V_{OV}): $V_{OV} = V_{GS} - V_{Th} = 3.0\text{V} - 1.0\text{V} = 2.0\text{V}$.
- Step 2: Check Saturation Condition: $V_{DS} = 5.0\text{V} \geq V_{OV} = 2.0\text{V} \implies$ Transistor is in SATURATION.
- Step 3: Calculate K_n: $K_n = k_n' \frac{W}{L} = 100\ \mu\text{A/V}^2 \times 10 = 1.0\ \text{mA/V}^2$.
- Step 4: Compute Drain Current I_D:
  $I_D = \frac{1}{2}(1.0\ \text{mA/V}^2)(2.0\text{V})^2 \times [1 + (0.02)(5.0)] = 0.5 \times 4.0 \times (1.10) = 2.20\ \text{mA}$.
- Step 5: Compute Transconductance g_m and Output Resistance r_o:
  $g_m = K_n V_{OV} = (1.0\ \text{mA/V}^2)(2.0\text{V}) = 2.0\ \text{mS}$; $r_o = \frac{1}{\lambda I_{D0}} = \frac{1}{(0.02\ \text{V}^{-1})(2.0\ \text{mA})} = 25\ \text{k}\Omega$.

Parasitic Capacitances and High-Frequency Model

- Gate Oxide Capacitances: Gate-to-Source capacitance C_{gs} and Gate-to-Drain capacitance C_{gd}.
- Triode Region Capacitances: $C_{gs} = C_{gd} = \frac{1}{2}WLC_{ox} + WL_{ov}C_{ox}$.
- Saturation Region Capacitances: Channel pinches off at drain; $C_{gs} = \frac{2}{3}WLC_{ox} + WL_{ov}C_{ox}$, while $C_{gd} = WL_{ov}C_{ox}$ (overlap capacitance only).
- Cutoff Region Capacitances: $C_{gs} = C_{gd} = WL_{ov}C_{ox}$; Gate-to-Body capacitance $C_{gb} = WLC_{ox}$.
- Transition Frequency (f_T): Frequency at which short-circuit current gain drops to unity: $f_T = \frac{g_m}{2\pi(C_{gs}+C_{gd})} \approx \frac{\mu_n(V_{GS}-V_{Th})}{2\pi L^2}$.

Summary of E-MOSFET Operational Equations

- Cutoff ($V_{GS} < V_{Th}$): $I_D = 0$ A.
- Triode ($V_{GS} \geq V_{Th}, V_{DS} < V_{GS} - V_{Th}$): $I_D = k_n' \frac{W}{L} \left[(V_{GS} - V_{Th}) V_{DS} - \frac{1}{2} V_{DS}^2 \right]$.
- Deep Triode ($V_{DS} \ll V_{GS} - V_{Th}$): $R_{DS(on)} = \frac{1}{k_n'(W/L)(V_{GS} - V_{Th})}$.
- Saturation ($V_{GS} \geq V_{Th}, V_{DS} \geq V_{GS} - V_{Th}$): $I_D = \frac{1}{2} k_n' \frac{W}{L} (V_{GS} - V_{Th})^2 (1 + \lambda V_{DS})$.
- Small-Signal Formulas: $g_m = \sqrt{2 K_n I_D} = K_n V_{OV}$; $r_o = \frac{V_A}{I_D} = \frac{1}{\lambda I_D}$.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: Three-Way Transistor Comparison

- Fundamental Device Physics & Carrier Types (Bipolar vs Unipolar).
- Control Mechanism Comparison: $I_C = \beta I_B$ vs Shockley & Square-Law models.
- Input Impedance Analysis ($r_\pi \sim 1$ kΩ vs $R_{in} \sim 10^8\,\Omega$ vs $R_{in} \sim 10^{12}\,\Omega$).
- Transconductance (g_m) & Voltage Gain Comparison.
- Noise Performance, Thermal Stability, and Thermal Runaway.
- Switching Speed, Power Dissipation, and High-Frequency Limits.
- Comprehensive Summary Comparison Matrix & Application Selection Guide.

Device Physics: Bipolar vs. Unipolar Carrier Transport

- BJT (Bipolar Junction Transistor): Bipolar transport; current conduction involves BOTH majority and minority charge carriers (electrons and holes).
- JFET (Junction Field-Effect Transistor): Unipolar transport; current conducted strictly by majority carriers (electrons in N-channel, holes in P-channel) flowing through a physical channel.
- MOSFET (Metal-Oxide-Semiconductor FET): Unipolar transport; current conducted exclusively by majority carriers flowing through a physically built-in or field-induced inversion channel.
- Minority Carrier Storage Effect: BJTs suffer from minority carrier storage delay in the base during turn-off; FETs exhibit zero minority carrier storage delay.
- Radiation Hardness: Unipolar FETs demonstrate significantly higher resistance to nuclear radiation damage than BJTs, as radiation creates recombination centers affecting minority carrier lifetime.

Control Mechanism: Current-Controlled vs. Voltage-Controlled

- BJT Control Equation: Current-controlled device; small input base current I_B controls large output collector current: $I_C = \beta I_B = I_S \exp\left(\frac{V_{BE}}{V_T}\right)$.
- JFET Control Equation: Voltage-controlled device; gate-to-source reverse voltage V_{GS} modulates depletion channel width: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$ (for $V_P \leq V_{GS} \leq 0$).
- D-MOSFET Control Equation: Voltage-controlled device; insulated gate potential operates across depletion and enhancement: $I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$.
- E-MOSFET Control Equation: Voltage-controlled device; gate bias induces channel above threshold: $I_D = \frac{1}{2}k_n' \frac{W}{L}(V_{GS} - V_{Th})^2$.
- Static Drive Power: BJTs demand continuous DC base drive power ($P_{drive} = V_{BE} I_B$); FETs require ZERO static DC gate current ($I_G \approx 0$ A).

Input Impedance Analysis (R_{in} / Z_{in} Comparison)

- BJT Input Impedance: Low to moderate ($R_{in} = r_\pi = \frac{\beta V_T}{I_{CQ}} \approx 1$ kΩ to 10 kΩ); forward-biased base-emitter PN junction draws continuous base current.
- JFET Input Impedance: High ($R_{in} = R_{gate} \parallel R_{reverse\_PN} \approx 10^8\Omega$ to $10^{10}\Omega$); reverse-biased gate-channel PN junction limits gate leakage to nanoamperes ($I_{GSS} \sim 1$ nA).
- MOSFET Input Impedance: Extremely High ($R_{in} \approx 10^{12}\Omega$ to $10^{15}\Omega$); dielectric SiO_2 oxide layer provides true physical DC isolation with picoampere leakage ($I_{GSS} \sim 1$ pA).
- Loading Effects: High input impedance of FETs eliminates loading errors when buffering high-impedance sensors (e.g., pH probes, piezoelectric crystals, capacitive transducers).
- ESD Susceptibility: Extreme insulation makes MOSFET gates vulnerable to Electrostatic Discharge (ESD) damage, whereas BJTs are robust against static charge accumulation.

Transconductance (g_m) and Voltage Gain Capabilities

- BJT Transconductance: Extremely High; proportional to DC bias current: $g_{m(BJT)} = \frac{I_C}{V_T} \approx \frac{I_C}{26\text{ mV}} \approx 38.5 \times I_C$ mS (at 1 mA, $g_m = 38.5$ mS).
- JFET Transconductance: Moderate; $g_{m(JFET)} = \frac{2I_{DSS}}{|V_P|}\left(1 - \frac{V_{GS}}{V_P}\right) \approx 1$ mS to 5 mS.
- MOSFET Transconductance: Moderate to High; $g_{m(MOS)} = \sqrt{2\mu C_{ox}(W/L)I_D} \approx 1$ mS to 20 mS (scalable by increasing channel width W).
- Voltage Gain Comparison: Single-stage BJT amplifier achieves higher voltage gain ($A_v = -g_m R_C \approx 100 - 500$) than standard FET stages ($A_v = -g_m R_D \approx 10 - 50$) due to superior g_m per unit bias current.
- Gain-Bandwidth Product: BJT provides high transconductance-to-current ratio (g_m/I_D), making it ideal for ultra-high-frequency analog RF amplifiers.

Noise Characteristics: Shot Noise vs. Thermal & Surface Noise

- BJT Noise Profile: Exhibits Shot Noise due to charge carriers crossing potential barriers ($i_{n,shot}^2 = 2qI_B\Delta f$) and Thermal Noise from base resistance $r_{bb'}$.
- JFET Noise Profile: Lowest noise at low-to-medium frequencies; zero shot noise (no carrier junction crossing in channel), low $1/f$ flicker noise because channel is buried inside bulk silicon away from surface traps.
- MOSFET Noise Profile: Higher $1/f$ flicker noise at low frequencies due to carrier trapping at the SiO_2-silicon surface interface traps; thermal channel noise $i_{n,ch}^2 = 4kT(\frac{2}{3}g_m)\Delta f$ dominates at high frequencies.
- Low-Noise Audio Applications: JFETs are the premier choice for ultra-low-noise preamplifiers (condenser microphones, audio pickup cartridges).
- RF Noise Performance: Dual-gate MOSFETs and GaAs MESFETs excel in RF Low-Noise Amplifiers (LNAs) above 1 GHz.

Thermal Behavior and Thermal Runaway Resistance

- BJT Temperature Coefficient: Positive temperature coefficient of collector current (I_C increases with temperature T as V_{BE} decreases by -2 mV/$^\circ$C).
- Thermal Runaway Hazard in BJTs: Higher $T \implies$ Higher $I_C \implies$ Higher power dissipation $P_D \implies$ Higher T, leading to destructive thermal runaway unless stabilized by emitter resistor R_E.
- FET Temperature Coefficient: Negative temperature coefficient of drain current at high bias levels; carrier mobility decreases with temperature ($\mu_n \propto T^{-1.5}$) due to increased lattice scattering.
- Self-Limiting Safety in FETs: Higher $T \implies$ Lower carrier mobility $\mu_n \implies$ Lower drain current $I_D \implies$ Lower power dissipation, inherently preventing thermal runaway.
- Parallel Operation: MOSFETs can be connected in parallel without current-hogging resistors; BJTs in parallel require ballasting resistors to prevent one device from hogging all current.

Frequency Response and Switching Speed Comparison

- BJT Switching Delays: Limited by minority carrier storage time (t_s) during saturation turn-off; transition frequency $f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$ reaches tens of GHz in advanced SiGe heterojunction BJTs (HBTs).
- JFET Frequency Response: Limited by large gate-to-channel PN junction capacitance ($C_{iss} \sim 10 - 50$ pF); generally restricted to frequencies below 500 MHz.
- MOSFET Switching Speed: Extremely fast switching (nanoseconds); zero minority carrier storage delay allows multi-megahertz operation in switching power supplies (SMPS).
- MOSFET Parasitic Gate Drive Delay: High input capacitance requires substantial transient current to charge/discharge C_{gs} and C_{gd} (Miller capacitance) rapidly during switching transitions.
- RF Power Supremacy: LDMOS (Lateral Diffused MOS) and GaN HEMT devices dominate modern cellular basestation RF power amplifiers.

Fabrication Scalability and VLSI Integration Density

- BJT Fabrication Complexity: Requires complex multi-step isolation diffusion wells, deep collector sinks, and larger silicon area per transistor; limited integration density.
- JFET Fabrication Density: Difficult to integrate in high-density VLSI; primarily manufactured as discrete devices or specialized bi-FET op-amp front-ends.
- MOSFET VLSI Dominance: Extremely simple planar self-aligned structure; occupies minimal silicon real estate; enables billions of transistors per chip in modern CMOS microprocessors.
- CMOS Power Advantage: Complementary MOS (NMOS + PMOS) logic consumes ZERO static DC power, drawing power only during switching transients ($P = CfV_{DD}^2$).
- BiCMOS Technology: Combines high-input-impedance MOSFETs and high-drive BJT output stages on a single IC substrate for premium analog/digital performance.

Quantitative Problem: Transconductance & Drive Power Comparison

- Scenario: Compare a BJT ($I_{CQ} = 2$ mA, $\beta = 100$) and an NMOS ($K_n = 4$ mA/V^2, $I_{DQ} = 2$ mA) operating at room temperature ($V_T = 26$ mV).
- BJT Transconductance ($g_{m,BJT}$): $g_{m,BJT} = \frac{I_{CQ}}{V_T} = \frac{2 \text{ mA}}{26 \text{ mV}} = 76.92$ mS.
- MOSFET Transconductance ($g_{m,MOS}$):
  $g_{m,MOS} = \sqrt{2K_n I_{DQ}} = \sqrt{2 \times 4 \text{ mA/V}^2 \times 2 \text{ mA}} = \sqrt{16} = 4.0$ mS.
- BJT DC Input Drive Current (I_B): $I_B = \frac{I_{CQ}}{\beta} = \frac{2 \text{ mA}}{100} = 20$ μA.
- MOSFET DC Input Drive Current (I_G): $I_G = 0.00$ μA (ideal dielectric oxide isolation).
- Conclusion: BJT achieves $\approx 19.2\times$ higher transconductance, but demands 20 μA continuous DC drive current compared to 0 μA for MOSFET.

Master Technical Comparison Matrix: BJT vs. JFET vs. MOSFET

- Primary Carrier: BJT = Bipolar (n & p); JFET = Unipolar (majority); MOSFET = Unipolar (majority).
- Control Mechanism: BJT = Current (I_B); JFET = Voltage (V_{GS}); MOSFET = Voltage (V_{GS}).
- Input Resistance (R_{in}): BJT = $1 - 10$ kΩ; JFET = $10^8 - 10^{10}\,\Omega$; MOSFET = $10^{12} - 10^{15}\,\Omega$.
- Transconductance (g_m): BJT = Extremely High (I_C/V_T); JFET = Low-Moderate; MOSFET = Moderate-High (scalable).
- Thermal Coefficient: BJT = Positive (runaway risk); JFET = Negative (self-limiting); MOSFET = Negative (self-limiting).
- Low-Frequency Noise: BJT = Moderate (shot noise); JFET = Lowest (buried channel); MOSFET = High ($1/f$ surface noise).
- Static Power Dissipation: BJT = High ($V_{BE}I_B$); JFET = Very Low; MOSFET = Zero ($I_G = 0$).

Engineering Selection Guide: Choosing the Optimal Transistor

- Select BJT when: Requiring maximum voltage gain per stage, ultra-high transconductance, low output resistance drive, or discrete high-frequency RF amplification.
- Select JFET when: Designing ultra-low-noise front-end audio preamplifiers, high-input-impedance electrometers, or low-distortion analog switches.
- Select MOSFET when: Designing high-density digital VLSI microprocessors (CMOS), high-efficiency switch-mode power supplies (SMPS), or high-voltage EV inverters.
- Select IGBT (Insulated-Gate Bipolar Transistor) when: Combining MOSFET insulated gate drive with BJT low saturation voltage in mega-watt grid power electronics.

Summary: Comparative Transistor Performance Synthesis

- BJT Strength: Highest transconductance (g_m), superior voltage gain, but low input resistance and thermal runaway risk.
- JFET Strength: High input resistance ($10^8\,\Omega$), lowest low-frequency noise, but low transconductance and limited IC scalability.
- MOSFET Strength: Supreme input resistance ($10^{12}\,\Omega$), zero static drive power, fast switching, zero thermal runaway, and dominant VLSI integration.
- Key Paradigm Shift: Modern electronics has shifted predominantly toward MOSFET (CMOS) technology for digital and power systems, retaining BJTs and JFETs for specialized analog niches.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Outline: Industrial & Circuit Applications of FETs

- Application 1: Voltage Variable Resistors (VVR) in the Ohmic Region.
- Application 2: Analog Switches, Multiplexers, and CMOS Transmission Gates.
- Application 3: High Input Impedance Buffers & Source Followers.
- Application 4: Active Loads & Constant Current Sources in Integrated Circuits.
- Application 5: CMOS Digital Logic Gate Design & Power Dissipation.
- Application 6: Power MOSFETs in SMPS, Buck Converters, and H-Bridges.
- Application 7: RF / Microwave Low-Noise Amplifiers & AGC Systems.
- Quantitative Application Examples, Selection Guidelines, and Future Trends.

FET as a Voltage Variable Resistor (VVR)

- Operating Region Requirement: Operated strictly in the Deep Triode / Linear region where drain-source voltage is kept very small ($V_{DS} \ll V_{GS} - V_{Th}$).
- Resistance Formula (JFET / D-MOSFET): Channel resistance varies inversely with gate voltage: $r_{DS} = \frac{r_o}{\left(1 - \frac{V_{GS}}{V_P}\right)} = \frac{|V_P|}{2I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)}$.
- Resistance Formula (E-MOSFET): $r_{DS} = \frac{1}{\mu_n C_{ox} \frac{W}{L}(V_{GS} - V_{Th})} = \frac{1}{K_n(V_{GS} - V_{Th})}$.
- AC Distortion Reduction: Small AC signals ($\Delta v_{ds} < 100$ mV) prevent non-linear harmonic distortion; feedback resistors from drain to gate cancel second-harmonic distortion.
- Practical Uses: Automatic Gain Control (AGC) attenuators, voltage-controlled filters (VCF), volume control stages, and electronic equalizers.

FET as an Analog Switch & CMOS Transmission Gate

- Single-FET Analog Switch: An E-MOSFET acts as an ON/OFF switch for analog signals. When $V_{GS} > V_{Th}$, switch is ON ($R_{ON} \approx 10 - 100\,\Omega$); when $V_{GS} < V_{Th}$, switch is OFF ($R_{OFF} > 10^9\,\Omega$).
- Signal Amplitude Limitation: A single NMOS switch suffers from signal distortion when analog input voltage v_{in} approaches $V_{DD} - V_{Th}$, increasing R_{ON} drastically.
- CMOS Transmission Gate (TG): Connects an NMOS and a PMOS transistor in parallel, driven by complementary control signals (C and $\bar{C}$).
- Complementary Resistance Compensation: As v_{in} rises, NMOS R_{ON} increases while PMOS R_{ON} decreases, maintaining a nearly constant total switch resistance ($R_{TG} \approx$ const) across full signal rail 0V to V_{DD}.
- Applications: Sample-and-Hold (S/H) circuits for ADCs, switched-capacitor filters, analog multiplexers (MUX), and crossbar matrix switches.

Source Follower (Common Drain) Buffer Amplifier

- Circuit Topology: Input signal applied to Gate; output taken from Source across resistor R_S; Drain connected to DC supply V_{DD}.
- Near-Unity Voltage Gain: $A_v = \frac{v_o}{v_i} = \frac{g_m R_S}{1+g_m R_S} \approx 1$ (typically 0.95 to 0.99).
- Ultra-High Input Resistance: $R_{in} = R_G \approx 10^7\,\Omega$ to $10^{12}\,\Omega$ (can be bootstrapped to $> 10^{14}\,\Omega$).
- Low Output Resistance: $R_{out} = R_S \parallel \frac{1}{g_m} \approx \frac{1}{g_m}$ (typically $50\,\Omega$ to $500\,\Omega$).
- Primary Function: Impedance matching buffer; steps down high source impedance to drive low-impedance coaxial cables or heavy capacitive loads without signal attenuation.

FET Constant Current Sources and Active Loads in ICs

- Two-Terminal JFET Current Regulator: Tying Gate to Source ($V_{GS} = 0\text{V}$) forces a JFET to operate at constant saturation current $I_D = I_{DSS}$.
- MOSFET Current Mirror: Uses a diode-connected MOSFET ($V_{DS} = V_{GS}$) to bias a secondary MOSFET in saturation, replicating reference current: $I_{out} = I_{ref} \left(\frac{W_2/L_2}{W_1/L_1} \right)$.
- Active Load Superiority: Replacing passive collector/drain resistors with MOSFET current mirrors in integrated amplifiers yields extremely high incremental load resistance ($R_L \approx r_o \sim 100$ kΩ to 1 MΩ).
- Ultra-High Voltage Gain: Enables single-stage IC amplifier gain $A_v = -g_m(r_{o1} \parallel r_{o2}) \approx 100 - 1000$ without requiring large DC supply voltages or silicon area.
- Cascode Current Mirrors: Stacked FET current sources increase output resistance to $R_{out} \approx g_m r_o^2$, providing near-ideal current regulation.

CMOS Digital Logic Architecture and Power Efficiency

- Complementary Topology: Integrates Pull-Up PMOS network connected to V_{DD} and Pull-Down NMOS network connected to Ground (GND).
- CMOS Inverter Operation: When $V_{in} = 0$V (Logic 0), NMOS is OFF, PMOS is ON $\implies V_{out} = V_{DD}$ (Logic 1). When $V_{in} = V_{DD}$ (Logic 1), NMOS is ON, PMOS is OFF $\implies V_{out} = 0$V (Logic 0).
- Zero Static DC Power Dissipation: In both logic states, one network is completely OFF ($I_{DC} \approx 0$ A), yielding near-zero static power dissipation: $P_{static} = V_{DD} I_{leak}$.
- Dynamic Power Dissipation: Power is consumed ONLY during switching transitions to charge load capacitance: $P_{dynamic} = C_L V_{DD}^2 f_{clock}$.
- CMOS NAND & NOR Gates: NAND uses series NMOS / parallel PMOS; NOR uses parallel NMOS / series PMOS, forming the foundation of all microprocessors and microcontrollers.

Power MOSFETs in Switching Power Electronics

- Vertical Double-Diffused MOSFET (VDMOS / HEXFET): Vertical current flow through substrate allows high breakdown voltages (> 1000V) and low ON-resistance ($R_{DS(on)} < 10$ mΩ).
- Switch-Mode Power Supplies (SMPS): High switching speeds (100 kHz to 5 MHz) drastically reduce size of inductors and capacitors in DC-DC Buck/Boost converters.
- H-Bridge Motor Drive Circuits: Four Power MOSFETs arranged in an H-bridge configuration enable bidirectional speed and direction control of DC and BLDC motors via Pulse-Width Modulation (PWM).
- Freewheeling Body Diode: Intrinsic parasitic PN body diode in Power MOSFETs provides automatic freewheeling conduction paths for inductive motor currents.
- Thermal Management: Power MOSFETs parallel easily due to negative temperature coefficient of carrier mobility, preventing thermal hot-spots.

RF / Microwave Amplifiers and Dual-Gate MOSFETs

- Low-Noise Amplifiers (LNAs): High input impedance and low high-frequency noise figure make GaAs MESFETs and SiGe MOSFETs preferred for wireless receiver front-ends (GPS, Wi-Fi, 5G).
- Dual-Gate MOSFET Architecture: Features two gates in series over a single channel, creating an integrated Cascode structure inside a single physical package.
- Reduction of Miller Effect: Gate 2 (ac grounded) shields Gate 1 from Drain, reducing feedback capacitance C_{gd} to near zero and boosting bandwidth above 1 GHz.
- Automatic Gain Control (AGC) Function: Varying DC voltage on Gate 2 modulates channel transconductance g_m continuously, adjusting RF amplifier gain over a 50 dB range without changing input tuning.
- RF Power Amplifiers: Lateral Diffused MOS (LDMOS) provides tens of watts of linear RF power for cellular basestation transmitters.

FETs in Sample-and-Hold (S/H) Circuits for ADCs

- Sample-and-Hold Function: Captures fast-changing analog voltage levels and holds them constant during Analog-to-Digital Converter (ADC) conversion cycles.
- Circuit Components: An input FET switch (or CMOS Transmission Gate), a hold capacitor (C_H), and a high-input-impedance Source Follower or Op-Amp buffer.
- Sample Phase: Gate control signal turns FET switch ON ($R_{ON} \sim 20\,\Omega$), rapidly charging hold capacitor C_H to input signal voltage v_{in}.
- Hold Phase: Control signal turns FET switch OFF ($R_{OFF} > 10^{10}\,\Omega$); capacitor holds charge with minimal leakage current ($I_{leak} < 1$ pA).
- Key Performance Metrics: Low aperture jitter, fast settling time, minimal charge injection from gate clock, and low droop rate ($dV/dt = I_{leak}/C_H$).

FET Sensor Interfacing and Ion-Sensitive FETs (ISFET)

- High-Impedance Sensor Interface: FET buffers interface directly with high-impedance sensors such as piezoelectric accelerometers, pH electrodes, and pyroelectric infrared (PIR) detectors.
- Ion-Sensitive FET (ISFET): Replaces metal gate electrode with an chemically sensitive ion-selective membrane exposed to an aqueous electrolyte solution.
- ISFET Operation: Hydronium ion concentration (pH) in solution generates an electrostatic surface potential at membrane boundary, shifting V_{Th} linearly according to Nernst Equation.
- Bio-FETs & DNA Chips: Functionalized gate surfaces bind specific biomolecules or DNA strands, modulating channel current for real-time label-free biosensing.
- CMOS Sensor Integration: Enables smart single-chip sensors combining bio-transducers, amplification, and digital signal processing on one silicon die.

Quantitative Problem: Voltage Variable Resistor Design

- Design Goal: Design an N-channel JFET Voltage Variable Resistor (VVR) operating between $R_{min} = 200\,\Omega$ and $R_{max} = 5$ kΩ.
- Given JFET Parameters: $I_{DSS} = 10$ mA, $V_P = -4.0$V.
- Step 1: Calculate Minimum Resistance at $V_{GS} = 0$V: $r_{DS(min)} = \frac{|V_P|}{2I_{DSS}} = \frac{4.0\text{V}}{2(10\text{ mA})} = \frac{4.0}{0.020} = 200\,\Omega$ (Matches R_{min} specification!).
- Step 2: Calculate Required Gate Bias for $R_{max} = 5$ kΩ: $r_{DS} = \frac{r_{DS(min)}}{1 - V_{GS}/V_P} \implies 5000 = \frac{200}{1 - V_{GS}/(-4.0)}$.
- Step 3: Solve for V_{GS}: $1 - \frac{V_{GS}}{-4.0} = \frac{200}{5000} = 0.04 \implies \frac{V_{GS}}{4.0} = 0.04 - 1 = -0.96 \implies V_{GS} = -3.84$V.
- Conclusion: Adjusting gate voltage V_{GS} from 0V to -3.84V controls channel resistance continuously from $200\,\Omega$ up to $5000\,\Omega$.

Emerging Trends: Gallium Nitride (GaN) & Silicon Carbide (SiC) FETs

- Silicon Physical Limits: Silicon MOSFETs approach material limits in breakdown voltage ($E_{crit} \approx 0.3$ MV/cm) and thermal conductivity.
- Wide-Bandgap Advantages: GaN (3.4 eV) and SiC (3.2 eV) feature $10\times$ higher critical breakdown electric field ($E_{crit} \approx 3.0$ MV/cm) than Silicon (1.1 eV).
- High-Electron-Mobility Transistor (GaN HEMT): Utilizes 2D Electron Gas (2DEG) at AlGaN/GaN heterojunction, achieving ultra-low $R_{DS(on)}$ and switching speeds > 10 MHz.
- Electric Vehicle (EV) Power Inverters: SiC MOSFETs operate at junction temperatures $> 200°C$ and voltages > 1200V, improving EV drive range by $5 - 10\%$.
- Compact Fast Chargers: GaN power switches enable ultra-compact USB-C laptop/smartphone chargers operating at megahertz frequencies.

Summary: Comprehensive Application Taxonomy of FETs

- Analog Signal Modulation: Voltage Variable Resistors (VVR), AGC attenuators, and CMOS Transmission Gates.
- High-Impedance Amplification: Source Followers, buffer stages, and electrometer interfaces.
- Integrated Circuit Design: Active current sources, MOSFET current mirrors, and cascode amplifiers.
- Digital VLSI Systems: CMOS logic gates (Inverter, NAND, NOR) with near-zero static power dissipation.
- Power & RF Electronics: VDMOS/HEXFET in SMPS and H-Bridges; GaN/SiC FETs in EV power electronics; Dual-Gate MOSFETs in RF LNAs.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Plan & Topics Outline

- Need for DC Biasing in Transistor Amplifiers & Concept of Quiescent State
- Definition and Graphical Representation of Operating Point (Q-Point)
- Regions of BJT Operation: Cutoff, Active, and Saturation Limits
- DC Load Line Equation and Determination of Boundary Conditions
- DC Equivalent Circuit Derivation: Capacitive Open-Circuit Analysis
- Basic Fixed-Bias Circuit: Mathematical Analysis and Limitations
- Thermal Stability Factors & Parameters Affecting Q-Point Drift (β, V_{BE}, I_{CBO})
- Worked Numerical Problem: Calculating I_{CQ}, V_{CEQ}, and Power Dissipation
- Summary of Core Biasing Concepts and Q-Point Criteria

Need for DC Biasing in Transistor Amplifiers

- Superposition of AC Signal on DC Bias: BJT is a non-linear active device; to achieve linear operation for small-signal amplification, an external DC bias voltage V_{CC} must set a steady DC operating voltage and current before applying the AC input signal $v_{in}(t)$.
- Conduction Control in Base-Emitter Junction: The base-emitter PN junction requires a forward-bias voltage ($V_{BE} \approx 0.7$ V for Silicon, 0.3 V for Germanium) to maintain forward current conduction $I_B > 0$ throughout the entire 360-degree cycle of the AC input.
- Prevention of Distortion and Cutoff: Without proper DC bias, negative half-cycles of an AC input signal would drive $V_{BE} < 0.7$ V, turning the transistor OFF and causing extreme output distortion (cutoff clipping).
- Energy Conversion Function: Amplifiers do not create energy; they convert DC electrical power supplied by the bias source V_{CC} into AC signal power delivered to the load resistor R_L under the control of the input signal.

Definition of the Operating Point (Q-Point)

- Quiescent State Definition: The Operating Point, commonly called the Quiescent Point or Q-point, is the set of DC current and voltage values (V_{CEQ}, I_{CQ}) that exist in the transistor circuit in the complete absence of any AC input signal ($v_{in} = 0$ V).
- DC Coordinate Pair: For a Common-Emitter (CE) BJT amplifier, the Q-point is uniquely specified by two parameters: the DC collector current I_{CQ} (in mA) and the DC collector-emitter voltage V_{CEQ} (in Volts).
- Input Characteristic Dependency: Base current at the Q-point is governed by $I_{BQ} = \frac{V_{CC} - V_{BEQ}}{R_B}$, establishing the specific output characteristic curve $I_C = f(V_{CE})|_{I_B = I_{BQ}}$.
- Graphical Location: Geometrically, the Q-point is the exact point of intersection between the DC Load Line equation and the transistor's static collector characteristic curve corresponding to $I_B = I_{BQ}$.

BJT Regions of Operation & Q-Point Boundaries

- Active Region (Linear Amplifier Mode): Base-Emitter junction is forward biased ($V_{BE} \approx 0.7$ V), Collector-Base junction is reverse biased ($V_{CB} > 0$ V). Collector current is proportional to base current: $I_{CQ} = \beta_{DC} I_{BQ}$. This is the required region for low-distortion linear amplification.
- Saturation Region (Switch ON Mode): Base-Emitter and Collector-Base junctions are both forward biased ($V_{BE} \approx 0.8$ V, $V_{BC} > 0$ V). Collector-emitter voltage collapses to saturation level $V_{CE(\text{sat})} \approx 0.2$ V, and $I_C < \beta I_B$ (current limited by external collector resistor R_C).
- Cutoff Region (Switch OFF Mode): Base-Emitter junction is zero or reverse biased ($V_{BE} \leq 0$ V). Base current $I_B = 0$, collector current falls to leakage current $I_{CQ} = I_{CEO} \approx 0$ A, and $V_{CEQ} = V_{CC}$.
- Boundary Criteria for Undistorted Swing: To maximize symmetric AC voltage swing without hitting Saturation ($V_{CE(\text{sat})}$) or Cutoff (V_{CC}), the Q-point must be located precisely at the midpoint of the active region: $V_{CEQ} \approx \frac{V_{CC}}{2}$.

Derivation of the DC Load Line Equation

- DC Circuit Reduction: Apply Kirchhoff's Voltage Law (KVL) to the output collector-emitter loop of a common-emitter amplifier operating under pure DC bias.
- Loop Equation: Starting from V_{CC} through collector resistor R_C, transistor collector-emitter junction V_{CE}, and emitter resistor R_E to ground: $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$.
- Current Approximation: Since $I_E = I_C + I_B \approx I_C$ (for $\beta \gg 1$), simplify the KVL loop to: $V_{CC} - I_C(R_C + R_E) - V_{CE} = 0$.
- Standard Line Form ($y = mx + c$): Expressing I_C as a function of V_{CE}: $I_C = -\frac{1}{R_C+R_E} V_{CE} + \frac{V_{CC}}{R_C+R_E}$.
- Physical Slope Interpretation: The slope of the DC Load Line is given by $m = -\frac{1}{R_{DC}} = -\frac{1}{R_C+R_E}$, determined entirely by external circuit resistors and independent of transistor parameters.

DC Load Line Endpoints & Graphical Construction

- Cutoff Endpoint ($I_C = 0$ mA): Set collector current to zero in the DC load line equation. The collector-emitter voltage reaches its maximum value equal to the supply voltage: $V_{CE(\text{off})} = V_{CC}$. Point A on graph: $(V_{CC}, 0)$.
- Saturation Endpoint ($V_{CE} = 0$ V): Assuming ideal zero saturation voltage $V_{CE} = 0$ V, the collector current reaches its theoretical maximum saturation limit: $I_{C(\text{sat})} = \frac{V_{CC}}{R_C + R_E}$. Point B on graph: $(0, \frac{V_{CC}}{R_C + R_E})$.
- Constructing the Line: Connecting Point A $(V_{CC}, 0)$ on the horizontal voltage axis to Point B $(0, I_{C(\text{sat})})$ on the vertical current axis yields the DC Load Line.
- Q-Point Intersection: Substituting base bias current $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$ yields $I_{CQ} = \beta I_{BQ}$. The Q-point is the intersection of the line with the static curve $I_B = I_{BQ}$, giving coordinates (V_{CEQ}, I_{CQ}) where $V_{CEQ} = V_{CC} - I_{CQ}(R_C + R_E)$.

DC Equivalent Circuit Analysis Procedure

- Capacitor Behavior at DC ($f = 0$ Hz): The capacitive reactance is $X_C = \frac{1}{2\pi fC} \to \infty\ \Omega$. All input coupling ($C_{in}$), output coupling ($C_{out}$), and emitter bypass ($C_E$) capacitors act as complete OPEN CIRCUITS.
- Isolation of DC Biasing Network: Removing open-circuited capacitors isolates the DC bias circuit from AC input signal sources and external load resistance R_L.
- AC Source Deactivation: All independent AC voltage sources $v_{in}(t)$ are set to zero (replaced by short circuits to ground).
- DC Circuit Analysis Steps: 1. Calculate base current I_{BQ} from input loop KVL. 2. Calculate collector current $I_{CQ} = \beta_{DC} I_{BQ}$. 3. Calculate collector voltage $V_{CEQ} = V_{CC} - I_{CQ}R_C - I_{EQ}R_E$. 4. Verify that $V_{CEQ} > V_{CE(\text{sat})} \approx 0.2$ V to confirm active region operation.

Basic Fixed-Bias Circuit & Mathematical Formulations

- Circuit Configuration: A single base resistor R_B is connected directly between the supply voltage V_{CC} and the transistor base terminal. Collector resistor R_C is connected from V_{CC} to collector. Emitter is tied directly to ground ($R_E = 0$).
- Input Loop Analysis (Base-Emitter Loop): Applying KVL:
  $V_{CC} - I_B R_B - V_{BE} = 0 \implies I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B}$.
- Output Loop Analysis (Collector-Emitter Loop): Applying KVL:
  $V_{CC} - I_C R_C - V_{CE} = 0 \implies V_{CEQ} = V_{CC} - I_{CQ} R_C$, where $I_{CQ} = \beta_{DC} I_{BQ}$.
- Major Drawback & Instability: Base current I_{BQ} is constant for a given R_B, but collector current $I_{CQ} = \beta \cdot I_{BQ}$ depends heavily on β_{DC}. Since β_{DC} varies widely (e.g., 50 to 300 due to manufacturing spread and temperature), the Q-point is extremely unstable.

Factors Influencing Q-Point Instability & Thermal Drift

- Transistor Parameter Sensitivity: The operating point (V_{CEQ}, I_{CQ}) drifts significantly due to temperature variations and component replacement.
- Temperature Variation of Reverse Saturation Current (I_{CBO}): Reverse leakage current doubles approximately every 10°C rise in temperature: $I_{CBO}(T_2) = I_{CBO}(T_1) \cdot 2^{\frac{T_2 - T_1}{10}}$. Rise in I_{CBO} directly increases total $I_C = \beta I_B + (1 + \beta) I_{CBO}$.
- Temperature Variation of Base-Emitter Voltage (V_{BE}): V_{BE} decreases linearly with temperature at a rate of $\frac{dV_{BE}}{dT} \approx -2.5$ mV/°C (or -2.3 mV/°C). As T increases, V_{BE} drops, causing base current I_B and collector current I_C to increase.
- Temperature Sensitivity of Current Gain (β_{DC}): Beta increases with temperature at approximately $+0.5\%$ to $+1\%$ per °C, further amplifying the drift of I_{CQ}.

Thermal Runaway Mechanism in BJT Circuits

- Definition: Thermal Runaway is a destructive self-reinforcing positive feedback loop where increased junction temperature causes collector current to rise, which increases power dissipation, leading to further temperature rise until transistor destruction.
- Positive Feedback Chain: $\uparrow T_j \longrightarrow \uparrow I_{CBO}$ & $\uparrow \beta$ & $\downarrow V_{BE} \longrightarrow \uparrow I_C \longrightarrow \uparrow P_D(V_{CE}I_C) \longrightarrow \uparrow T_j$.
- Power Dissipation Formula: Collector junction power dissipation is $P_D = V_{CE}I_C + V_{BE}I_B \approx V_{CE}I_C$. Heat generated elevates junction temperature $T_j = T_A + \theta_{JA}P_D$, where θ_{JA} is thermal resistance (°C/W).
- Thermal Stability Condition: To prevent thermal runaway, the rate of increase of heat dissipation capability must exceed the rate of increase of heat generation: $\frac{\partial P_D}{\partial T_j} < \frac{1}{\theta_{JA}}$.
- Mitigation Strategy: Incorporating an emitter resistor R_E provides negative feedback to stabilize I_C against thermal drift.

Worked Example: Q-Point Calculation for Fixed-Bias Circuit

- Problem Statement: For a fixed-bias common-emitter amplifier circuit with $V_{CC} = 12$ V, base resistor $R_B = 240$ kΩ, collector resistor $R_C = 2.2$ kΩ, and silicon transistor with $\beta = 100$ ($V_{BE} = 0.7$ V): 1. Calculate quiescent base current I_{BQ} and collector current I_{CQ}. 2. Calculate quiescent collector-emitter voltage V_{CEQ}. 3. Determine saturation collector current $I_{C(\text{sat})}$. 4. Calculate total DC power dissipated by the transistor.
- Step 1 (Base Current): $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240 \times 10^3\ \Omega} = \frac{11.3\text{ V}}{240\text{ k}\Omega} = 47.08\ \mu\text{A}$.
- Step 2 (Collector Current): $I_{CQ} = \beta \cdot I_{BQ} = 100 \times 47.08\ \mu\text{A} = 4.708$ mA.
- Step 3 (Collector-Emitter Voltage): $V_{CEQ} = V_{CC} - I_{CQ}R_C = 12\text{ V} - (4.708\text{ mA} \times 2.2\text{ k}\Omega) = 12\text{ V} - 10.358\text{ V} = 1.642$ V.
- Step 4 (Saturation & Power): $I_{C(\text{sat})} = \frac{V_{CC}}{R_C} = \frac{12\text{ V}}{2.2\text{ k}\Omega} = 5.455$ mA. Transistor power $P_D = V_{CEQ} \cdot I_{CQ} = 1.642\text{ V} \times 4.708\text{ mA} = 7.73$ mW.

Worked Example: Evaluating β Sensitivity in Fixed Bias

- Problem Statement: Using the same circuit parameters ($V_{CC} = 12$ V, $R_B = 240$ kΩ, $R_C = 2.2$ kΩ), evaluate the shift in Q-point if the transistor is replaced with one having $\beta = 150$ (50% increase).
- Base Current Calculation: $I_{BQ} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = 47.08\ \mu$A (remains completely unchanged by transistor replacement).
- New Collector Current: $I_{CQ(\text{new})} = \beta_{\text{new}} \cdot I_{BQ} = 150 \times 47.08\ \mu\text{A} = 7.062$ mA.
- Attempted V_{CEQ} Calculation: $V_{CEQ} = V_{CC} - I_{CQ(\text{new})} R_C = 12\text{ V} - (7.062\text{ mA} \times 2.2\text{ k}\Omega) = 12\text{ V} - 15.536\text{ V} = -3.536$ V.
- Physical Analysis & Saturation Verification: Since calculated $V_{CEQ} < 0$ V (impossible in passive circuits), the transistor has been driven completely into SATURATION! Actual $V_{CE(\text{sat})} \approx 0.2$ V, and actual $I_{C(\text{sat})} = \frac{12 - 0.2}{2.2\text{ k}\Omega} = 5.36$ mA.
- Engineering Conclusion: Fixed bias fails to maintain active region operation under normal β parameter variations, proving the imperative need for stabilized biasing schemes like Voltage Divider Bias.

Summary of Lecture 11 & Key Engineering Insights

- Purpose of Biasing: DC biasing establishes quiescent conditions (V_{CEQ}, I_{CQ}) to ensure linear, unclipped small-signal amplification.
- DC Load Line Mechanics: Defined by $I_C = -\frac{1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}$, connecting $(V_{CC}, 0)$ to $(0, \frac{V_{CC}}{R_{DC}})$. It depends exclusively on passive supply and resistor values.
- Optimal Q-Point Selection: Center of the active region ($V_{CEQ} \approx V_{CC}/2$) offers maximum symmetrical peak-to-peak signal swing.
- Thermal Sensitivity Factors: Junction temperature rise elevates I_{CBO} and β while reducing V_{BE}, threatening thermal runaway.
- Fixed Bias Limitation: Unacceptable Q-point instability due to direct β-dependence, necessitating emitter degeneration feedback circuits.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Q-Point Dynamics & Stability Analysis

- Maximum Undistorted Peak-to-Peak Signal Swing ($V_{o(p-p)}$)
- Graphical Analysis of Saturation Clipping vs. Cutoff Clipping
- Non-linear Signal Distortion and Harmonic Generation
- Derivation of Stability Factor $S = \frac{\partial I_C}{\partial I_{CBO}}$
- Stability Factors S' ($\partial I_C / \partial V_{BE}$) and S'' ($\partial I_C / \partial \beta$)
- Emitter Degeneration Resistor R_E and Negative Bias Feedback
- Comparative Evaluation of Biasing Networks against Thermal Drift
- Comprehensive Step-by-Step Numerical Stability Analysis
- Summary & Practical Circuit Design Rules

Maximum Undistorted Signal Swing Mechanics

- Dynamic AC Swing Concept: When an AC signal $v_{in}(t)$ is applied, collector current $i_C(t) = I_{CQ} + i_c(t)$ and collector-emitter voltage $v_{CE}(t) = V_{CEQ} + v_{ce}(t)$ oscillate along the load line around the quiescent Q-point.
- Saturation Limit (Positive Collector Current Peak): As i_c increases, v_{CE} decreases toward saturation $V_{CE(\text{sat})}$. The maximum positive swing in collector current before saturation clipping is: \{}Delta I_{C(\{}text{sat})} = I_{C(\{}text{sat})} - I_{CQ} = \{}frac{V_{CEQ} - V_{CE(\{}text{sat})}}{r_c}.
- Cutoff Limit (Negative Collector Current Peak): As i_c decreases toward zero ($i_C = 0$), v_{CE} increases toward cutoff $v_{ce(\text{off})}$. The maximum negative swing in collector current before cutoff clipping is: \{}Delta I_{C(\{}text{off})} = I_{CQ}.
- Symmetrical Swing Condition: To prevent asymmetric clipping, the maximum unclipped peak AC collector current is: $I_{c(\text{peak})} = \min\left(I_{CQ}, \frac{V_{CEQ} - V_{CE(\text{sat})}}{r_c}\right)$.

Mathematical Derivation of Maximum Peak-to-Peak Voltage Swing

- AC Output Voltage Swing Definition: The AC output voltage swing across collector AC load resistance $r_c = R_C \parallel R_L$ is given by $v_{ce(p-p)} = 2 \cdot V_{ce(peak)}$.
- Voltage Swing Bound 1 (Saturation Limited): $V_{ce(peak1)} = V_{CEQ} - V_{CE(\text{sat})} \approx V_{CEQ}$ (assuming $V_{CE(\text{sat})} \approx 0$ V).
- Voltage Swing Bound 2 (Cutoff Limited): $V_{ce(peak2)} = I_{CQ} \cdot r_c$.
- Unclipped Voltage Swing Equation: $V_{o(p-p)\,\max} = 2 \cdot \min\left(V_{CEQ} - V_{CE(\text{sat})},\ I_{CQ} \cdot r_c\right)$.
- Optimum Q-Point for Maximum Swing: Setting $V_{CEQ} - V_{CE(\text{sat})} = I_{CQ} r_c$ yields identical clipping boundaries on both positive and negative peaks, achieving maximum possible output power efficiency.

Waveform Distortion: Saturation vs. Cutoff Clipping

- Saturation Clipping Characteristics: Occurs when input signal amplitude pushes V_{CE} below $V_{CE(\text{sat})} \approx 0.2$ V. The output voltage waveform flattens out at the bottom peak (or top peak depending on phase inversion), introducing heavy odd-harmonic frequency components.
- Cutoff Clipping Characteristics: Occurs when base-emitter junction becomes reverse-biased during input troughs ($i_B \leq 0$). Collector current drops to zero, flattening the opposite peak of the AC output voltage waveform.
- Non-Linear Transfer Characteristic: BJT exponential collector current equation $I_C = I_S e^{V_{BE}/V_T}$ causes harmonic generation even prior to sharp clipping when signal amplitude exceeds thermal voltage $V_T \approx 26$ mV.
- Total Harmonic Distortion (THD): Defined as $\text{THD} = \frac{\sqrt{V_2^2+V_3^2+V_4^2+\cdots}}{V_1} \times 100\%$. Severe clipping elevates THD beyond 10%, rendering the amplifier unusable for high-fidelity audio.

Introduction to Thermal Stability Factor S

- Definition of Stability Factor S: The stability factor S measures the rate of change of collector current I_C with respect to reverse saturation leakage current I_{CBO}, holding V_{BE} and β constant: $S = \frac{\partial I_C}{\partial I_{CBO}}$.
- Ideal vs. Worst-Case Values: Lower S signifies superior thermal stability. Ideal stability factor is $S = 1$ (where change in I_C equals change in I_{CBO}). Poor stability circuits exhibit $S = 1 + \beta \approx 100$ to 300.
- General Derivative Formula Derivation: Starting with collector current relation $I_C = \beta I_B + (1 + \beta) I_{CBO}$. Differentiating both sides with respect to I_C: $1 = \beta \frac{\partial I_B}{\partial I_C} + (1 + \beta) \frac{\partial I_{CBO}}{\partial I_C}$.
- General Stability Equation: Rearranging terms yields: $S = \frac{\partial I_C}{\partial I_{CBO}} = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$.

Secondary Stability Factors S' and S''

- Stability Factor S' (V_{BE} Sensitivity): Measures change in I_C relative to base-emitter voltage drop V_{BE}, holding I_{CBO} and β constant: $S' = \frac{\partial I_C}{\partial V_{BE}}$.
- Mathematical Formulation for S': For circuit with feedback resistance, $S' = \frac{-\beta}{R_{Th}+(1+\beta)R_E}$. Since V_{BE} decreases by -2.5 mV/$^\circ$C, collector current shift is $\Delta I_C = S' \cdot \Delta V_{BE}$.
- Stability Factor S'' (β Sensitivity): Measures change in I_C relative to transistor current gain β, holding I_{CBO} and V_{BE} constant: $S'' = \frac{\partial I_C}{\partial \beta}$.
- Mathematical Formulation for S'': Differentiating I_C with respect to β yields $S'' = \frac{I_{C1}}{\beta_1(1+\beta_2)} \cdot S_2$, where S_2 is the stability factor of the target state.
- Total Collector Current Drift: Total drift combining all three thermal effects is: $\Delta I_C = S \cdot \Delta I_{CBO} + S' \cdot \Delta V_{BE} + S'' \cdot \Delta\beta$.

Emitter Degeneration Resistor R_E & Negative Bias Feedback

- Role of Emitter Resistor R_E: Introducing an emitter resistor R_E between transistor emitter and ground creates automatic negative voltage feedback that stabilizes the Q-point against thermal changes.
- Self-Stabilization Feedback Mechanism: 1. Temperature increases $\rightarrow I_C$ attempts to increase. 2. Emitter voltage $V_E = I_E R_E \approx I_C R_E$ increases. 3. Base-emitter junction voltage $V_{BE} = V_B - V_E$ decreases. 4. Decreased V_{BE} reduces base current I_B, opposing the initial rise in I_C.
- Quantitative Stabilization Requirement: Effective stabilization occurs when the voltage drop across emitter resistor $V_E = I_E R_E$ is much larger than thermal variations in V_{BE} ($V_E \approx 1$ V to 2 V, or $0.1V_{CC}$ to $0.2V_{CC}$).
- AC Bypass Capacitor C_E: To prevent R_E from reducing AC voltage gain (A_v), a large bypass capacitor C_E is connected in parallel with R_E, shorting AC signals to ground while retaining DC feedback.

Evaluation of Stability Factor S in Fixed Bias

- Circuit Base Current Equation: $I_B = \frac{V_{CC} - V_{BE}}{R_B}$.
- Derivative $\frac{\partial I_B}{\partial I_C}$: Since I_B depends only on constant parameters V_{CC}, V_{BE}, R_B, base current is completely independent of I_C: $\frac{\partial I_B}{\partial I_C} = 0$.
- Substitution into General Stability Formula: $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}} = \frac{1+\beta}{1-0} = 1 + \beta$.
- Numerical Impact: For a typical transistor with $\beta = 100$, $S = 101$. Any increase in leakage current ΔI_{CBO} is amplified by 101 times in collector current!
- Conclusion: Fixed bias offers zero feedback stabilization ($\frac{\partial I_B}{\partial I_C} = 0$), resulting in the worst possible stability factor $S = 1 + \beta$.

Evaluation of Stability Factor S in Collector-to-Base Bias

- Circuit Configuration: Base resistor R_B is tied between collector terminal and base terminal.
- Input Loop Equation: $V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0 \implies I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$.
- Derivative Calculation: Differentiating I_B with respect to I_C: $\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B + R_C}$.
- Substitution into Stability Equation: $S = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_B+R_C}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}$.
- Stability Improvement Analysis: Because the denominator is $(1 + \text{positive term}) > 1$, S is significantly smaller than $1 + \beta$. If $\beta R_C \gg (R_B + R_C)$, $S \approx 1 + \frac{R_B}{R_C}$.

Worked Example: Calculating S and S' for Voltage Divider Bias

- Circuit Parameters: Silicon transistor with $\beta = 100$, $V_{CC} = 15$ V, $R_1 = 33$ kΩ, $R_2 = 10$ kΩ, $R_C = 2.7$ kΩ, $R_E = 1$ kΩ.
- Step 1 (Thevenin Equivalent): $V_{Th} = V_{CC}\frac{R_2}{R_1+R_2} = 15\text{ V} \times \frac{10\text{ k}\Omega}{43\text{ k}\Omega} = 3.488$ V.
  $R_{Th} = R_1 \parallel R_2 = \frac{33\times 10}{43}\ \text{k}\Omega = 7.674\ \text{k}\Omega$.
- Step 2 (Derivative $\frac{\partial I_B}{\partial I_C}$): Base loop KVL: $V_{Th} - I_B R_{Th} - V_{BE} - I_E R_E = 0$. Since $I_E = I_B + I_C$, $I_B = \frac{V_{Th}-V_{BE}-I_C R_E}{R_{Th}+R_E}$. Differentiating wrt I_C: $\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_{Th}+R_E}$.
- Step 3 (Calculate Stability Factor S):
  $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_{Th}+R_E}\right)} = \frac{101}{1+100\left(\frac{1\text{ k}\Omega}{7.674\text{ k}\Omega+1\text{ k}\Omega}\right)} = \frac{101}{1+100\left(\frac{1}{8.674}\right)} = \frac{101}{1+11.529} = \frac{101}{12.529} = 8.06.$
- Step 4 (Calculate Stability Factor S'):
  $S' = \frac{-\beta}{R_{Th}+(1+\beta)R_E} = \frac{-100}{7.674\text{ k}\Omega+101\times 1\text{ k}\Omega} = \frac{-100}{108.674\text{ k}\Omega} = -0.920$ mA/V.

Worked Example: Collector Current Shift under Temperature Rise

- Problem Statement: Using the Voltage Divider Bias circuit from Slide 11 ($S = 8.06, S' = -0.92$ mA/V), calculate the change in collector current ΔI_C when ambient temperature rises from 25°C to 75°C ($\Delta T = 50°C$). Given at 25°C: $I_{CBO} = 0.2\ \mu$A, $V_{BE} = 0.7$ V. At 75°C: I_{CBO} doubles every 10°C, $\frac{dV_{BE}}{dT} = -2.5$ mV/°C.
- Step 1 (ΔI_{CBO} Calculation): $\Delta T = 50°C \implies$ 5 doublings ($2^{50/10} = 32$). $I_{CBO}(75°C) = 0.2\ \mu\text{A} \times 2^5 = 0.2 \times 32 = 6.4\ \mu$A. $\Delta I_{CBO} = 6.4\ \mu\text{A} - 0.2\ \mu\text{A} = 6.2\ \mu$A.
- Step 2 (ΔV_{BE} Calculation): $\Delta V_{BE} = (-2.5\ \text{mV}/°\text{C}) \times 50°\text{C} = -125$ mV $= -0.125$ V.
- Step 3 (Drift due to I_{CBO}): $\Delta I_{C1} = S \cdot \Delta I_{CBO} = 8.06 \times 6.2\ \mu\text{A} = 49.97\ \mu\text{A} \approx 0.050$ mA.
- Step 4 (Drift due to V_{BE}): $\Delta I_{C2} = S' \cdot \Delta V_{BE} = (-0.920\ \text{mA/V}) \times (-0.125\ \text{V}) = +0.115$ mA.
- Step 5 (Total Shift ΔI_C): $\Delta I_C = \Delta I_{C1} + \Delta I_{C2} = 0.050\ \text{mA} + 0.115\ \text{mA} = +0.165$ mA.

Comparative Analysis of Biasing Stability Factors

- Fixed Bias: Stability Factor $S = 1 + \beta$. No feedback loop ($\partial I_B / \partial I_C = 0$). Poor stability; unusable in precision circuits.
- Collector-to-Base Feedback Bias: Stability Factor $S = \frac{1+\beta}{1+\beta \frac{R_C}{R_B + R_C}}$. Negative voltage feedback improves S moderately ($S \approx 10$ to 30).
- Voltage Divider Bias (Self-Bias): Stability Factor $S = \frac{1+\beta}{1+\beta \frac{R_E}{R_{Th} + R_E}} \approx 1 + \frac{R_{Th}}{R_E}$ (when $\beta R_E \gg R_{Th}$). Best overall stability ($S < 10$ easily achievable).
- Design Criterion for Minimal Drift: Select $R_{Th} \leq 0.1 \beta R_E$. Under this condition, $S \approx 1 + \frac{0.1 \beta R_E}{R_E} \approx 1 + 0.1\beta$, ensuring complete independence from transistor β variations.

Summary of Lecture 12 & Advanced Q-Point Rules

- Max Undistorted Swing: Bounded by $V_{o(p-p)\,\max} = 2 \cdot \min(V_{CEQ} - V_{CE(\text{sat})}, I_{CQ} r_c)$. Symmetrical headroom requires $V_{CEQ} = I_{CQ} r_c$.
- Harmonic Clipping: Saturation clips positive collector current peaks; cutoff clips negative peaks, producing high Total Harmonic Distortion (THD).
- Stability Factor S: Quantifies sensitivity to leakage current: $S = \frac{1+\beta}{1-\beta \frac{\partial I_B}{\partial I_C}}$. Target low values ($S \to 1$).
- Role of Negative Feedback: Emitter resistor R_E introduces negative current feedback to oppose thermal drift in I_C.
- Optimal Topology: Voltage Divider Bias provides the most predictable Q-point stability when designed with $R_{Th} \ll \beta R_E$.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Plan: Load Line Fundamentals

- Concept and Purpose of Load Lines in Electronic Circuit Analysis
- DC Load Line: Mathematical Derivation, Slopes, and Boundary Coordinates
- AC Load Line: Concept of AC Load Resistance ($r_c = R_C \parallel R_L$)
- Mathematical Derivation of the AC Load Line Equation
- AC Load Line Endpoints: AC Saturation Current and AC Cutoff Voltage
- Comparative Analysis of DC vs AC Load Line Parameters
- Effect of Coupling/Bypass Capacitors on AC Load Line Slope
- Optimum Q-Point Placement for Maximum Symmetrical AC Swing
- Comprehensive Worked Numerical Example with Graph Plotting
- Summary & Key Takeaways

Overview and Fundamental Concept of Load Lines

- Graphical Interface: A load line is a straight line drawn on the transistor's output characteristic curves (I_C vs V_{CE}) that represents all possible combined operating states allowed by external circuit resistors and power supplies.
- Dual Nature of Amplifiers: An amplifier operates simultaneously under two operational modes: DC steady-state bias (zero input signal) and AC dynamic response (time-varying input signal).
- DC Load Line Function: Determines the static quiescent operating point (Q-point) under zero-signal conditions based solely on DC resistance paths.
- AC Load Line Function: Determines the trajectory along which instantaneous voltage $v_{CE}(t)$ and current $i_C(t)$ move when an AC input signal $v_{in}(t)$ is applied, based on AC load impedance.

D.C. Load Line: Derivation & Characteristics

- Circuit Model: Consider a Common-Emitter amplifier powered by V_{CC} with collector resistor R_C and emitter resistor R_E.
- Output KVL Equation: $V_{CC} - I_C R_C - V_{CE} - I_E R_E = 0$.
- DC Resistance Definition: Defining total DC resistance $R_{DC} = R_C + R_E$ (since $I_E \approx I_C$), the KVL equation simplifies to: $V_{CE} = V_{CC} - I_C R_{DC}$.
- Linear Equation Form: $I_C = -\frac{1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}$.
- DC Slope & Intercepts: - Slope $m_{DC} = -\frac{1}{R_{DC}} = -\frac{1}{R_C + R_E}$. - Voltage Intercept (Cutoff): $V_{CE(\text{off})} = V_{CC}$ (when $I_C = 0$). - Current Intercept (Saturation): $I_{C(\text{sat})} = \frac{V_{CC}}{R_{DC}} = \frac{V_{CC}}{R_C + R_E}$ (when $V_{CE} = 0$).

A.C. Equivalent Resistance (r_c) Derivation

- Capacitors at Signal Frequencies: At operational AC frequencies ($f > 20$ Hz), coupling capacitors (C_1, C_2) and emitter bypass capacitors (C_E) have negligible reactance ($X_C \to 0\ \Omega$) and act as short circuits.
- DC Supply Behavior at AC: The DC voltage source V_{CC} has zero internal AC impedance and acts as an AC ground reference.
- Collector AC Path: Under AC conditions, collector resistor R_C is connected between collector and AC ground. External load resistor R_L is connected through coupling capacitor C_2 between collector and AC ground.
- Effective AC Load Resistance (r_c): R_C and R_L appear in parallel to AC signals: $r_c = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L}$.
- Emitter AC Path: Bypass capacitor C_E short-circuits R_E to ground ($r_e = 0\ \Omega$ for AC path in bypassed CE amplifier). Therefore, total AC load resistance seen by collector is r_c.

Derivation of the A.C. Load Line Equation

- AC Ohm's Law Relationship: Small-signal collector voltage variation $v_{ce}(t)$ and current variation $i_c(t)$ are related by the AC load resistance: $i_c = -\frac{v_{ce}}{r_c}$.
- Superposition of AC and DC Values: Instantaneous collector current $i_C(t) = I_{CQ} + i_c(t)$ and instantaneous collector-emitter voltage $v_{CE}(t) = V_{CEQ} + v_{ce}(t)$.
- Substituting Instantaneous Variations: $i_c(t) = i_C(t) - I_{CQ}$ and $v_{ce}(t) = v_{CE}(t) - V_{CEQ}$.
- AC Load Line Formula: Substituting variations into AC Ohm's law: $(i_C - I_{CQ}) = -\frac{1}{r_c}(v_{CE} - V_{CEQ})$.
- Standard Point-Slope Form: $i_C = -\frac{1}{r_c} v_{CE} + \left(I_{CQ} + \frac{V_{CEQ}}{r_c}\right)$.
- Constraint: The AC load line MUST pass directly through the quiescent Q-point coordinate (V_{CEQ}, I_{CQ}).

A.C. Load Line Intercepts & Boundary Coordinates

- AC Saturation Current Point ($v_{CE} = 0$ V): Setting instantaneous voltage $v_{CE} = 0$ in the AC load line equation yields the maximum peak AC collector saturation current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c}$.
- AC Cutoff Voltage Point ($i_C = 0$ mA): Setting instantaneous current $i_C = 0$ yields the maximum peak AC collector-emitter cutoff voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} \cdot r_c$.
- Graphical Construction: Connect Point A $(v_{ce(\text{off})}, 0) = (V_{CEQ} + I_{CQ} r_c,\ 0)$ on the voltage axis to Point B $(0, i_{C(\text{sat})}) = (0,\ I_{CQ} + \frac{V_{CEQ}}{r_c})$ on the current axis.
- Pivotal Property: The AC load line intersects the DC load line precisely at the Q-point (V_{CEQ}, I_{CQ}).
- Slope Steepness Comparison: Because $r_c = R_C \parallel R_L < R_{DC} = R_C + R_E$, the magnitude of the AC slope $|-1/r_c|$ is STEEPER than the DC slope $|-1/R_{DC}|$.

Comparative Table: D.C. Load Line vs. A.C. Load Line

- Parameter Comparison: 1. Governing Resistance: DC resistance $R_{DC} = R_C + R_E$ vs AC load resistance $r_c = R_C \parallel R_L$. 2. Slope: DC slope $m_{DC} = -\frac{1}{R_C+R_E}$ vs AC slope $m_{AC} = -\frac{1}{R_C \parallel R_L}$. 3. Line Equation: $I_C = -\frac{1}{R_{DC}} V_{CE} + \frac{V_{CC}}{R_{DC}}$ vs $i_C - I_{CQ} = -\frac{1}{r_c}(v_{CE} - V_{CEQ})$. 4. Voltage Axis Intercept: $V_{CE(\text{off})} = V_{CC}$ vs $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} r_c$. 5. Current Axis Intercept: $I_{C(\text{sat})} = \frac{V_{CC}}{R_C+R_E}$ vs $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c}$. 6. Role in Circuit Design: Sets static DC Q-point vs determines max AC signal swing & output power.

Effect of Load Resistance R_L on AC Load Line Slope

- Unloaded Amplifier ($R_L = \infty$): If no external load is connected, $r_c = R_C \parallel \infty = R_C$. If emitter is bypassed (R_E shorted at AC), AC slope is -\{}frac{1}{R_C}, which is steeper than DC slope -\{}frac{1}{R_C + R_E}.
- Heavy AC Loading ($R_L \ll R_C$): Connecting a small load resistance R_L sharply reduces $r_c = \frac{R_C R_L}{R_C + R_L} \approx R_L$.
- Graphical Rotation: As R_L decreases, r_c decreases, causing the AC load line to rotate CLOCKWISE around the fixed Q-point (steeper slope).
- Impact on Signal Swing: Heavy loading (smaller r_c) dramatically reduces the cutoff voltage swing limit $v_{ce(\text{peak})} = I_{CQ} r_c$, causing early cutoff clipping at lower AC input signal levels.

Optimum Q-Point Location for Maximum AC Voltage Swing

- Equal Swing Headroom Condition: To achieve maximum symmetrical undistorted AC output swing, the AC saturation current headroom must equal the AC cutoff voltage headroom expressed in equivalent current.
- Mathematical Condition: \{}Delta V_{ce(\{}text{sat})} = \{}Delta V_{ce(\{}text{cutoff})} \{}implies V_{CEQ} - V_{CE(\{}text{sat})} = I_{CQ} \{}cdot r_c.
- Assuming $V_{CE(\text{sat})} \approx 0$ V: $V_{CEQ} = I_{CQ} \cdot r_c$.
- Derivation of Optimum V_{CEQ}: Substitute $I_{CQ} = \frac{V_{CC} - V_{CEQ}}{R_{DC}}$ into optimum condition:
  $V_{CEQ} = \left(\frac{V_{CC} - V_{CEQ}}{R_{DC}}\right) r_c \implies V_{CEQ}\left(1 + \frac{r_c}{R_{DC}}\right) = V_{CC}\frac{r_c}{R_{DC}}$.
- Optimum Q-Point Equation: $V_{CEQ(\text{opt})} = \frac{V_{CC}}{1 + \frac{R_{DC}}{r_c}} = \frac{V_{CC} \cdot r_c}{r_c + R_{DC}}$.
- Optimum Current Equation: $I_{CQ(\text{opt})} = \frac{V_{CC}}{r_c + R_{DC}}$.

Worked Example: DC and AC Load Line Calculation

- Circuit Specification: A CE amplifier has $V_{CC} = 15$ V, $R_C = 3.3$ kΩ, $R_E = 1.2$ kΩ, $R_L = 4.7$ kΩ, and Q-point coordinates $I_{CQ} = 2.0$ mA, $V_{CEQ} = 6.0$ V.
- Step 1 (DC Resistance & DC Load Line): $R_{DC} = R_C + R_E = 3.3\ \text{k}\Omega + 1.2\ \text{k}\Omega = 4.5\ \text{k}\Omega$. DC Cutoff Voltage: $V_{CE(\text{off})} = V_{CC} = 15$ V. DC Saturation Current: $I_{C(\text{sat})} = \frac{V_{CC}}{R_{DC}} = \frac{15\ \text{V}}{4.5\ \text{k}\Omega} = 3.33$ mA.
- Step 2 (AC Load Resistance r_c): $r_c = R_C \parallel R_L = \frac{3.3 \times 4.7}{3.3+4.7}\ \text{k}\Omega = \frac{15.51}{8.0}\ \text{k}\Omega = 1.939\ \text{k}\Omega$.
- Step 3 (AC Load Line Intercepts): AC Saturation Current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c} = 2.0\ \text{mA} + \frac{6.0\ \text{V}}{1.939\ \text{k}\Omega} = 2.0 + 3.094 = 5.094$ mA. AC Cutoff Voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} r_c = 6.0\ \text{V} + (2.0\ \text{mA} \times 1.939\ \text{k}\Omega) = 6.0 + 3.878 = 9.878$ V.

Worked Example: Max Swing & Clipping Determination

- Continuing from Slide 11: Q-point (6.0 V, 2.0 mA), $r_c = 1.939$ kΩ.
- Step 1 (Calculate Saturation-Limited Peak Voltage):
  $V_{ce(peak1)} = V_{CEQ} - V_{CE(\text{sat})} = 6.0\text{ V} - 0.2\text{ V} = 5.80\text{ V}$.
- Step 2 (Calculate Cutoff-Limited Peak Voltage):
  $V_{ce(peak2)} = I_{CQ} \cdot r_c = 2.0\text{ mA} \times 1.939\text{ k}\Omega = 3.878\text{ V}$.
- Step 3 (Determine Maximum Unclipped Output Swing):
  $V_{ce(peak)} = \min(5.80\text{ V}, 3.878\text{ V}) = 3.878\text{ V}$. $V_{o(p-p)\,\max} = 2 \times 3.878\text{ V} = 7.756\text{ V}$.
- Step 4 (Clipping Analysis): Since $V_{ce(peak2)}(3.878\text{ V}) < V_{ce(peak1)}(5.80\text{ V})$, the amplifier will experience CUTOFF CLIPPING first if overdriven beyond 7.76 V_{p-p}.

Graphical Plotting Guidelines for Load Lines

- Step 1: Plot transistor output characteristic curves (I_C vs V_{CE}) for various base currents I_B.
- Step 2: Plot the DC Load Line using endpoints $(V_{CC}, 0)$ and $(0, \frac{V_{CC}}{R_{DC}})$. Draw a straight line between them.
- Step 3: Mark the Q-point at the intersection of the DC Load Line and the operating base current curve $I_B = I_{BQ}$.
- Step 4: Compute AC load resistance $r_c = R_C \parallel R_L$ and find AC endpoints $(V_{CEQ} + I_{CQ} r_c,\ 0)$ and $(0,\ I_{CQ} + \frac{V_{CEQ}}{r_c})$.
- Step 5: Draw the AC Load Line passing through both AC endpoints and verify that it pivots directly through the Q-point.
- Step 6: Draw input AC signal waveform $i_b(t)$ on base axis and project output AC signals $i_c(t)$ and $v_{ce}(t)$ along the AC Load Line.

Summary of Lecture 13 & Load Line Principles

- Dual Load Line Concept: DC load line determines static Q-point; AC load line dictates dynamic AC signal variations.
- Slope Differences: DC slope $m_{DC} = -1/(R_C + R_E)$ vs AC slope $m_{AC} = -1/(R_C \parallel R_L)$. AC slope is always steeper due to $r_c < R_{DC}$.
- AC Intercepts: Saturation $i_{C(\text{sat})} = I_{CQ} + V_{CEQ}/r_c$; Cutoff $v_{ce(\text{off})} = V_{CEQ} + I_{CQ}r_c$.
- Optimum Q-Point: Maximum symmetrical AC swing occurs when $V_{CEQ(\text{opt})} = \frac{V_{CC}r_c}{r_c + R_{DC}}$.
- Engineering Application: Crucial tool for designing high-efficiency power amplifiers and preventing waveform clipping.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Plan: Dynamic Design & Power Efficiency

- Dynamic Load Line Mechanics across Transistor Configurations (CE, CC, CB)
- AC Collector Power Output Calculation (P_{ac})
- DC Supply Power (P_{dc}) and Transistor Collector Dissipation (P_C)
- Derivation of Series-Fed Class-A Amplifier Efficiency ($\eta = P_{ac}/P_{dc}$)
- Transformer-Coupled Class-A Load Lines and Efficiency Limit (50%)
- Dynamic Q-Point Shift under Large-Signal Overdrive
- Thermal Hyperbola and Transistor Power Dissipation Ratings ($P_{D(\max)}$)
- Design Problem 1: Designing Biasing for Target AC Power Output
- Design Problem 2: Symmetrical Swing Optimization with Real-World Tolerances
- Summary & Practical Engineering Principles

Dynamic Load Lines Across BJT Configurations

- Common-Emitter (CE) Configuration: Highest combined voltage and current gain. DC load resistance $R_{DC} = R_C + R_E$, AC load resistance $r_c = R_C \parallel R_L$. High input impedance, inverted output AC phase (180°).
- Common-Collector (CC / Emitter Follower): Unity voltage gain ($A_v \approx 1$), high current gain ($\beta + 1$). Collector tied to DC supply ($R_C = 0$). Load resistor R_L is placed in emitter circuit. $R_{DC} = R_E$, $r_e = R_E \parallel R_L$. AC load line equation: $i_e - I_{EQ} = -\frac{1}{r_e}(v_{ce} - V_{CEQ})$.
- Common-Base (CB) Configuration: High voltage gain, unity current gain ($\alpha \approx 1$). Low input impedance, high output impedance. Used in high-frequency RF amplification. $R_{DC} = R_C + R_E$, $r_c = R_C \parallel R_L$.

AC Power Output Derivation (P_{ac})

- RMS Signal Quantities: For a sinusoidal AC signal, RMS voltage across load r_c is $V_{ce(rms)} = \frac{V_{ce(peak)}}{\sqrt{2}}$ and RMS current is $I_{c(rms)} = \frac{I_{c(peak)}}{\sqrt{2}}$.
- AC Power Delivered to Load Resistance (P_{ac}): $P_{ac} = V_{ce(rms)} \cdot I_{c(rms)} = \frac{V_{ce(peak)}}{\sqrt{2}} \cdot \frac{I_{c(peak)}}{\sqrt{2}} = \frac{V_{ce(peak)} \cdot I_{c(peak)}}{2}$.
- Peak-to-Peak Expression: Expressing in terms of peak-to-peak voltage $V_{o(p-p)}$ and current $I_{o(p-p)}$: $P_{ac} = \frac{V_{o(p-p)} \cdot I_{o(p-p)}}{8} = \frac{V_{o(p-p)}^2}{8r_c}$.
- Maximum Unclipped AC Power Output: Under maximum unclipped symmetrical swing condition ($V_{ce(peak)} = V_{CEQ}, I_{c(peak)} = I_{CQ}$): $P_{ac(\max)} = \frac{V_{CEQ} \cdot I_{CQ}}{2}$.

DC Power Supply & Collector Dissipation

- Total DC Power Input (P_{dc}): Supplied by the DC voltage source V_{CC} to the entire amplifier circuit: $P_{dc} = V_{CC} \cdot I_{CC} \approx V_{CC} \cdot I_{CQ}$ (neglecting minor base bias current).
- DC Power Dissipated in Resistors (P_R): Power consumed as heat in collector and emitter resistors: $P_R = I_{CQ}^2(R_C + R_E) = I_{CQ}^2 R_{DC}$.
- Collector Junction Power Dissipation (P_C): Under zero AC signal conditions, transistor collector junction absorbs all remaining DC power: $P_{C(\text{quiescent})} = V_{CEQ} \cdot I_{CQ}$.
- Signal-Dependent Collector Power ($P_C(ac)$): When AC signal is present, AC power P_{ac} is delivered to load, REDUCING transistor heating: $P_C = P_{C(\text{quiescent})} - P_{ac}$.
- Worst-Case Thermal Condition: Maximum transistor heating occurs at ZERO AC INPUT SIGNAL ($v_{in} = 0$), where $P_C = V_{CEQ} \cdot I_{CQ}$.

Derivation of Max Efficiency for Series-Fed Class-A

- Power Conversion Efficiency Definition: Efficiency η measures the capability of an amplifier to convert DC supply power into useful AC signal power: $\eta = \frac{P_{ac}}{P_{dc}} \times 100\%$.
- Series-Fed Configuration: Load resistor is directly connected as the collector resistor ($R_C = R_L$, $R_{DC} = r_c = R_C$).
- DC Load Line Endpoints: Saturation $I_{C(\text{sat})} = \frac{V_{CC}}{R_C}$, Cutoff $V_{CE(\text{off})} = V_{CC}$.
- Optimum Q-Point for Max Swing: $V_{CEQ} = \frac{V_{CC}}{2}$ and $I_{CQ} = \frac{V_{CC}}{2R_C}$.
- Max AC Power Output: $P_{ac(\text{max})} = \frac{V_{CEQ} \cdot I_{CQ}}{2} = \frac{(V_{CC}/2)(V_{CC}/2R_C)}{2} = \frac{V_{CC}^2}{8R_C}$.
- Total DC Power Input: $P_{dc} = V_{CC} \cdot I_{CQ} = V_{CC} \cdot \frac{V_{CC}}{2R_C} = \frac{V_{CC}^2}{2R_C}$.
- Efficiency Derivation: $\eta_{\text{max}} = \frac{P_{ac(\text{max})}}{P_{dc}} = \frac{V_{CC}^2/8R_C}{V_{CC}^2/2R_C} = \frac{2}{8} = 0.25 = 25\%$.

Transformer-Coupled Class-A Amplifier Load Line

- Topology Advantage: Replacing collector resistor R_C with a step-down transformer primary winding reduces DC collector resistance to near zero ($R_{DC} \approx 0\ \Omega$).
- DC Load Line Behavior: Since $R_{DC} \approx 0$, the DC load line is nearly VERTICAL at $V_{CEQ} \approx V_{CC}$.
- Reflected AC Load Resistance (r'_c): Impedance transformation by transformer turns ratio $n = N_1/N_2$: $r'_c = n^2 R_L = \left(\frac{N_1}{N_2}\right)^2 R_L$.
- AC Load Line Voltage Induction: Primary winding inductance allows collector voltage to swing UP TO TWICE V_{CC} ($v_{ce(\text{off})} \approx 2V_{CC}$) during negative current swings due to inductive kickback.
- Efficiency Derivation: Max AC swing $V_{ce(peak)} = V_{CC}$ and $I_{c(peak)} = I_{CQ}$. $P_{ac(\max)} = \frac{V_{CC} I_{CQ}}{2}$, $P_{dc} = V_{CC} I_{CQ}$. Efficiency $\eta_{\max} = \frac{V_{CC} I_{CQ}/2}{V_{CC} I_{CQ}} = 50\%$.

The Maximum Thermal Power Dissipation Hyperbola

- Transistor Rating Limits: Manufacturers specify maximum junction power rating $P_{D(\text{max})}$ at ambient temperature 25°C (e.g., 500 mW for 2N2222, 10 W for TIP31).
- Thermal Hyperbola Equation: Plotting $V_{CE} \cdot I_C = P_{D(\text{max})}$ on output characteristics yields a rectangular hyperbola curve.
- Safe Operating Area (SOA): The region under the hyperbola bounded by $V_{CE(\text{max})}$ breakdown voltage and $I_{C(\text{max})}$ saturation current.
- Q-Point Boundary Constraint: To prevent transistor destruction from overheating, the quiescent Q-point MUST lie strictly BELOW the $P_{D(\text{max})}$ hyperbola curve.
- Derating Factor: At higher operating temperatures ($T_A > 25°\text{C}$), $P_{D(\text{max})}$ must be derated linearly using thermal resistance θ_{JA}: $P_{D(\text{derated})} = \frac{T_{j(\text{max})} - T_A}{\theta_{JA}}$.

Dynamic Q-Point Shift Under Large Signal Overdrive

- Small-Signal Assumption: Linear AC analysis assumes small input amplitudes where operating point variations remain strictly linear along the static AC load line.
- Large-Signal Non-Linearity: BJT exponential transconductance $I_C = I_S e^{V_{BE}/V_T}$ causes positive half-cycles of collector current to expand more than negative half-cycles contract.
- DC Average Shift: Non-symmetrical current peaks create a net DC rectified current component ΔI_{DC}. Total average collector current becomes $I_{C(\text{avg})} = I_{CQ} + \Delta I_{DC}$.
- Dynamic Q-Point Migration: As input signal amplitude increases, the effective average Q-point shifts upward and rightward along the DC load line, altering bias conditions and increasing heat dissipation.

Worked Example: Power Dissipation & Efficiency Calculation

- Problem Statement: A Common-Emitter series-fed Class-A amplifier operates with $V_{CC} = 18$ V, collector resistor $R_C = 1.2$ kΩ, and Q-point set at $V_{CEQ} = 9$ V, $I_{CQ} = 7.5$ mA. 1. Calculate DC supply power P_{dc}. 2. Calculate maximum unclipped AC power output $P_{ac(\max)}$. 3. Calculate amplifier conversion efficiency η. 4. Calculate transistor collector dissipation under zero signal $P_{C(0)}$ and max signal $P_{C(\text{max signal})}$.
- Step 1 (DC Power Input): $P_{dc} = V_{CC} \cdot I_{CQ} = 18 \text{ V} \times 7.5 \text{ mA} = 135 \text{ mW}$.
- Step 2 (Max AC Power Output): $P_{ac(\max)} = \frac{V_{CEQ} \cdot I_{CQ}}{2} = \frac{9 \text{ V} \times 7.5 \text{ mA}}{2} = \frac{67.5}{2} = 33.75 \text{ mW}$.
- Step 3 (Conversion Efficiency): $\eta = \frac{P_{ac(\max)}}{P_{dc}} \times 100\% = \frac{33.75 \text{ mW}}{135 \text{ mW}} \times 100\% = 25.0\%$.
- Step 4 (Transistor Heat Dissipation): - Zero Signal: $P_{C(0)} = V_{CEQ} \cdot I_{CQ} = 9 \text{ V} \times 7.5 \text{ mA} = 67.5 \text{ mW}$. - Max Signal: $P_{C(\text{max signal})} = P_{C(0)} - P_{ac(\max)} = 67.5 \text{ mW} - 33.75 \text{ mW} = 33.75 \text{ mW}$.

Worked Example: Dynamic AC Load Line with External Load R_L

- Circuit Specification: $V_{CC} = 12$ V, $R_C = 2.2$ kΩ, $R_E = 680$ Ω, $R_L = 1.0$ kΩ, Q-point set at $I_{CQ} = 2.5$ mA, $V_{CEQ} = 4.8$ V.
- Step 1 (DC Resistance & DC Load Line Endpoints): $R_{DC} = R_C + R_E = 2.2\ \text{k}\Omega + 0.68\ \text{k}\Omega = 2.88\ \text{k}\Omega$. DC Cutoff: $V_{CE(\text{off})} = 12$ V; DC Saturation: $I_{C(\text{sat})} = \frac{12\ \text{V}}{2.88\ \text{k}\Omega} = 4.167$ mA.
- Step 2 (AC Load Resistance r_c): $r_c = R_C \parallel R_L = \frac{2.2 \times 1.0}{2.2+1.0}\ \text{k}\Omega = \frac{2.2}{3.2}\ \text{k}\Omega = 687.5\ \Omega$.
- Step 3 (AC Load Line Endpoints): AC Saturation Current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c} = 2.5\ \text{mA} + \frac{4.8\ \text{V}}{687.5\ \Omega} = 2.5\ \text{mA} + 6.982\ \text{mA} = 9.482$ mA. AC Cutoff Voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ} r_c = 4.8\ \text{V} + (2.5\ \text{mA} \times 687.5\ \Omega) = 4.8\ \text{V} + 1.719\ \text{V} = 6.519$ V.
- Step 4 (Max AC Power Delivered to Load R_L): Max peak voltage across load: $V_p = \min(V_{CEQ} - V_{CE(\text{sat})}, I_{CQ} r_c) = \min(4.6\ \text{V}, 1.719\ \text{V}) = 1.719$ V. AC Power to R_L: $P_{L(\text{max})} = \frac{V_p^2}{2R_L} = \frac{(1.719)^2}{2 \times 1000} = \frac{2.955}{2000} = 1.478$ mW.

Symmetrical Swing Design Optimization Procedure

- Objective: Given supply voltage V_{CC} and AC load R_L, design R_C and R_E to achieve maximum symmetrical undistorted output voltage swing.
- Design Step 1: Choose emitter resistor drop $V_E \approx 0.1V_{CC}$ for DC thermal stability. Set $R_E = \frac{0.1V_{CC}}{I_{CQ}}$.
- Design Step 2: Set optimum V_{CEQ} condition: $V_{CEQ(\text{opt})} = \frac{V_{CC} \cdot r_c}{r_c + R_{DC}}$.
- Design Step 3: Solve for required collector resistor R_C such that $r_c = R_C \parallel R_L$ satisfies symmetrical swing $I_{CQ} r_c = V_{CEQ} - V_{CE(\text{sat})}$.
- Design Step 4: Verify that peak transistor dissipation $P_{C(0)} = V_{CEQ} I_{CQ}$ stays safely below $P_{D(\text{max})}$ thermal hyperbola with a 50% safety margin.

Summary Table: Power & Load Line Formulas

- Core Formula Summary: 1. DC Load Line: $I_C = -\frac{1}{R_C+R_E}V_{CE} + \frac{V_{CC}}{R_C+R_E}$ 2. AC Load Line: $i_C - I_{CQ} = -\frac{1}{r_c}(v_{CE} - V_{CEQ})$, where $r_c = R_C \parallel R_L$ 3. AC Saturation Current: $i_{C(\text{sat})} = I_{CQ} + \frac{V_{CEQ}}{r_c}$ 4. AC Cutoff Voltage: $v_{ce(\text{off})} = V_{CEQ} + I_{CQ}r_c$ 5. Max Sinusoidal AC Power: $P_{ac(\text{max})} = \frac{V_{ce(peak)}I_{c(peak)}}{2} = \frac{V_{o(p-p)}^2}{8r_c}$ 6. DC Input Power: $P_{dc} = V_{CC}I_{CQ}$ 7. Max Series-Fed Efficiency: $\eta_{\text{max}} = 25\%$ 8. Max Transformer-Coupled Efficiency: $\eta_{\text{max}} = 50\%$

Summary of Lecture 14 & Engineering Principles

- AC Power & Headroom: $P_{ac} = \frac{V_{ce(peak)} I_{c(peak)}}{2}$. AC swing is strictly bounded by load line intercepts $i_{C(\text{sat})}$ and $v_{ce(\text{off})}$.
- Class-A Efficiency Limits: Series-fed topology reaches a maximum of 25% efficiency; transformer coupling elevates efficiency to 50%.
- Worst-Case Thermal Loading: Transistors dissipate maximum heat at ZERO AC input signal ($P_C = V_{CEQ} I_{CQ}$).
- Safe Operating Area: Q-point must remain below the thermal hyperbola $V_{CE} I_C = P_{D(\text{max})}$ under all operating temperatures.
- Next Lecture Preview: Transition to detailed analysis of BJT Biasing Methods (Fixed Bias, Collector Feedback, Emitter Bias, Voltage Divider Bias).

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Plan: Biasing Methods Breakdown

- Overview and Selection Criteria for BJT Biasing Networks
- Method 1: Fixed Bias (Base Bias) — Derivation, Drawbacks, and Instability
- Method 2: Collector-to-Base Feedback Bias — Negative Feedback Mechanism
- Method 3: Emitter-Feedback Bias (Fixed Bias with R_E) — DC Degeneration
- Method 4: Voltage Divider Bias (Self Bias) — Detailed Thevenin Analysis
- Design Protocol for Voltage Divider Bias (R_E, R_{Th}, R_1, R_2 Selection)
- Quantitative Comparison of Stability Factors (S) across Topologies
- Worked Numerical Problem 1: Fixed Bias vs Voltage Divider Bias Drift
- Worked Numerical Problem 2: Designing a Voltage Divider Bias Circuit
- Comparative Matrix & Final Selection Guidelines

Method 1: Fixed Bias Circuit Analysis

- Circuit Configuration: Base resistor R_B connected directly between DC supply V_{CC} and base terminal. Collector resistor R_C connected between V_{CC} and collector. Emitter tied to ground.
- Base Current Equation: Applying KVL around base-emitter loop: $V_{CC} - I_{BQ}R_B - V_{BE} = 0 \implies I_{BQ} = \frac{V_{CC}-V_{BE}}{R_B}$.
- Collector Current & Voltage: $I_{CQ} = \beta_{DC} I_{BQ} = \beta \left(\frac{V_{CC}-V_{BE}}{R_B} \right)$. Collector-emitter voltage: $V_{CEQ} = V_{CC} - I_{CQ}R_C$.
- Stability Factor Derivation: Since I_{BQ} is independent of I_{CQ}, $\frac{\partial I_B}{\partial I_C} = 0$. Substituting into general formula: $S = \frac{1+\beta}{1-\beta(0)} = 1 + \beta$.
- Critical Failure Mode: Maximum possible thermal instability ($S = 1 + \beta$). Any rise in temperature or change in transistor β causes severe Q-point shift directly into saturation.

Method 2: Collector-to-Base Feedback Bias

- Circuit Configuration: Base resistor R_B is connected to the collector terminal instead of V_{CC}, introducing negative feedback.
- Base Loop KVL Equation: $V_{CC} - (I_{CQ} + I_{BQ})R_C - I_{BQ}R_B - V_{BE} = 0$.
- Base Current Formula: Assuming $I_{CQ} \gg I_{BQ}$: $I_{BQ} = \frac{V_{CC}-V_{BE}}{R_B+\beta R_C}$.
- Collector Current Formula: $I_{CQ} = \frac{\beta(V_{CC}-V_{BE})}{R_B+\beta R_C} = \frac{V_{CC}-V_{BE}}{\frac{R_B}{\beta}+R_C}$.
- Stabilization Mechanism: If $T \uparrow \implies I_C \uparrow \implies V_C = (V_{CC} - I_C R_C) \downarrow \implies I_B \downarrow \implies I_C \downarrow$ (restores equilibrium).
- Stability Factor S: Derivative $\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B+R_C} \implies S = \frac{1+\beta}{1+\beta\frac{R_C}{R_B+R_C}}$. Achieves moderate stability ($S < 1 + \beta$).

Method 3: Emitter Bias (Fixed Bias with R_E)

- Circuit Topology: Single base resistor R_B to V_{CC}, collector resistor R_C to V_{CC}, and an emitter resistor R_E connected between emitter and ground.
- Input Loop KVL Equation: $V_{CC} - I_B R_B - V_{BE} - I_E R_E = 0$.
- Base Current Equation: Since $I_E = (1+\beta) I_B$: $I_{BQ} = \frac{V_{CC} - V_{BE}}{R_B + (1+\beta) R_E}$.
- Collector Current Equation: $I_{CQ} = \frac{\beta (V_{CC} - V_{BE})}{R_B + (1+\beta) R_E} \approx \frac{V_{CC} - V_{BE}}{\frac{R_B}{\beta} + R_E}$.
- Stability Factor S: Derivative $\frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_B + R_E} \implies S = \frac{1+\beta}{1+\beta \frac{R_E}{R_B + R_E}}$.
- Condition for β-Independence: If $(1+\beta) R_E \gg R_B$, $I_{CQ} \approx \frac{V_{CC} - V_{BE}}{R_E}$, making collector current nearly independent of transistor β.

Method 4: Voltage Divider Bias (Self-Bias)

- Circuit Topology: Two resistors R_1 and R_2 form a potential divider across V_{CC} to establish a fixed base voltage V_B. Resistors R_C and R_E set collector and emitter currents.
- Thevenin Network Reduction (Base Input): - Thevenin Voltage: $V_{Th} = V_{CC}\left(\frac{R_2}{R_1+R_2}\right)$. - Thevenin Resistance: $R_{Th} = R_1 \parallel R_2 = \frac{R_1 R_2}{R_1+R_2}$.
- Thevenin Base Loop KVL Equation: $V_{Th} - I_{BQ}R_{Th} - V_{BE} - I_{EQ}R_E = 0$.
- Exact Collector Current Equation: $I_{CQ} = \frac{\beta(V_{Th}-V_{BE})}{R_{Th}+(1+\beta)R_E} = \frac{V_{Th}-V_{BE}}{\frac{R_{Th}}{\beta}+\left(\frac{1+\beta}{\beta}\right)R_E}$.
- Approximate Formula (Practical Design Condition): When $(1+\beta)R_E \gg R_{Th}$ (or $R_{Th} \leq 0.1\beta R_E$), $I_B R_{Th} \approx 0$, yielding: $V_B \approx V_{Th} \implies I_{CQ} \approx I_{EQ} = \frac{V_{Th}-V_{BE}}{R_E}$.

Detailed Design Procedure for Voltage Divider Bias

- Step 1 (Select Supply and Q-Point): Choose supply voltage V_{CC} and target quiescent values I_{CQ} and V_{CEQ} (typically $V_{CEQ} \approx 0.5V_{CC}$).
- Step 2 (Select Emitter Resistor R_E): Allocate 10% to 20% of supply voltage across emitter resistor for robust thermal stability: $V_E = I_{EQ}R_E \approx 0.1V_{CC} \implies R_E = \frac{0.1V_{CC}}{I_{CQ}}$.
- Step 3 (Calculate Collector Resistor R_C): Apply output loop KVL: $R_C = \frac{V_{CC} - V_{CEQ} - V_E}{I_{CQ}}$.
- Step 4 (Calculate Base Voltage V_B): $V_B = V_E + V_{BE} = 0.1V_{CC} + 0.7$ V.
- Step 5 (Select Base Divider Resistors R_1, R_2): - Apply stability rule: $R_{Th} \leq 0.1\beta R_E \implies R_1 \parallel R_2 = 0.1\beta R_E$. - Divider current rule: Set divider current $I_{\text{div}} = \frac{V_{CC}}{R_1+R_2} \geq 10I_B$. - Calculate $R_2 = \frac{V_B}{10I_B}$ and $R_1 = \frac{V_{CC}-V_B}{10I_B}$.

Comparative Stability Factor (S) Equations

- Fixed Bias: $S = 1 + \beta$. Maximum instability ($S \approx 100$ to 300). Zero feedback.
- Collector Feedback Bias: $S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}$. Moderate stability ($S \approx 15$ to 40). Voltage feedback.
- Emitter Bias: $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_B+R_E}\right)}$. Good stability if $R_E \gg R_B/\beta$ ($S \approx 10$ to 25). Current feedback.
- Voltage Divider Bias: $S = \frac{1+\beta}{1+\beta\left(\frac{R_E}{R_{Th}+R_E}\right)}$. Excellent stability ($S < 10$). Best performance when $R_{Th} \ll \beta R_E$.
- Asymptotic Limit of Voltage Divider Bias: As $R_{Th}/R_E \to 0$, $S \to 1 + \frac{R_{Th}}{R_E} \approx 1$ (the theoretical minimum ideal stability factor).

Worked Example: Q-Point Drift Comparison

- Problem Statement: Compare the change in I_{CQ} when β increases from 100 to 200 (100% increase) for: 1. Fixed Bias circuit with $V_{CC} = 12$ V, $R_B = 220$ kΩ, $R_C = 2.2$ kΩ. 2. Voltage Divider Bias circuit with $V_{CC} = 12$ V, $R_1 = 39$ kΩ, $R_2 = 10$ kΩ, $R_C = 2.2$ kΩ, $R_E = 1.0$ kΩ.
- Fixed Bias Analysis: - At $\beta = 100$: $I_{BQ} = \frac{12-0.7}{220\ \text{k}\Omega} = 51.36\ \mu\text{A} \implies I_{CQ1} = 100 \times 51.36\ \mu\text{A} = 5.136$ mA. - At $\beta = 200$: $I_{CQ2} = 200 \times 51.36\ \mu\text{A} = 10.272$ mA (100% INCREASE in I_C, driving circuit into saturation!).
- Voltage Divider Bias Analysis: - $V_{Th} = 12 \times \frac{10}{49} = 2.449$ V; $R_{Th} = \frac{39 \times 10}{49}\ \text{k}\Omega = 7.959$ kΩ. - At $\beta = 100$: $I_{CQ1} = \frac{100(2.449-0.7)}{7.959\ \text{k}\Omega + 101(1\ \text{k}\Omega)} = \frac{174.9\ \text{V}}{108.96\ \text{k}\Omega} = 1.605$ mA. - At $\beta = 200$: $I_{CQ2} = \frac{200(2.449-0.7)}{7.959\ \text{k}\Omega + 201(1\ \text{k}\Omega)} = \frac{349.8\ \text{V}}{208.96\ \text{k}\Omega} = 1.674$ mA.
- Comparison Conclusion: - Fixed Bias I_C drift: +100% (5.14 mA → 10.27 mA). - Voltage Divider Bias I_C drift: ONLY +4.3% (1.605 mA → 1.674 mA). Proves total stability!

Worked Example: Designing a Voltage Divider Bias Network

- Design Specification: Design a Voltage Divider Bias circuit for a silicon NPN BJT ($\beta = 120$, $V_{BE} = 0.7$ V) operating from $V_{CC} = 15$ V to set Q-point at $I_{CQ} = 2.0$ mA and $V_{CEQ} = 7.5$ V.
- Step 1 (Select V_E & Calculate R_E): Set $V_E = 0.1 V_{CC} = 0.1 \times 15$ V $= 1.5$ V. $R_E = \frac{V_E}{I_{CQ}} = \frac{1.5 \text{ V}}{2.0 \text{ mA}} = 750\ \Omega$ (Standard value: 750 Ω).
- Step 2 (Calculate R_C): Output loop KVL: $V_{CC} - I_{CQ} R_C - V_{CEQ} - V_E = 0$. $R_C = \frac{V_{CC} - V_{CEQ} - V_E}{I_{CQ}} = \frac{15 \text{ V} - 7.5 \text{ V} - 1.5 \text{ V}}{2.0 \text{ mA}} = \frac{6.0 \text{ V}}{2.0 \text{ mA}} = 3.0$ kΩ (Standard value: 3.0 kΩ).
- Step 3 (Calculate Base Voltage V_B): $V_B = V_E + V_{BE} = 1.5 \text{ V} + 0.7 \text{ V} = 2.2$ V.
- Step 4 (Determine R_1 and R_2): - Base current $I_{BQ} = \frac{I_{CQ}}{\beta} = \frac{2.0 \text{ mA}}{120} = 16.67\ \mu$A. - Set divider current $I_{\text{div}} = 10 I_{BQ} = 166.7\ \mu$A. - $R_2 = \frac{V_B}{I_{\text{div}}} = \frac{2.2 \text{ V}}{166.7\ \mu\text{A}} = 13.2$ kΩ (Standard value: 13 kΩ). - $R_1 = \frac{V_{CC} - V_B}{I_{\text{div}}} = \frac{15 \text{ V} - 2.2 \text{ V}}{166.7\ \mu\text{A}} = \frac{12.8 \text{ V}}{166.7\ \mu\text{A}} = 76.8$ kΩ (Standard value: 75 kΩ).

Input Impedance Trade-Offs Across Biasing Topologies

- Fixed Bias Input Resistance (R_{in}): Base resistor R_B is connected in parallel with transistor input AC resistance $r_\pi = \beta r_e$: $R_{in} = R_B \parallel r_\pi \approx r_\pi$. Offers highest input impedance because R_B is very large (100 kΩ to 1 MΩ).
- Collector Feedback Input Resistance (R_{in}): Miller effect reduces effective base resistance: $R_{in} = \left(\frac{R_B}{1+A_v}\right) \parallel r_\pi$, significantly reducing input impedance.
- Voltage Divider Bias Input Resistance (R_{in}): Parallel combination of base divider resistors and transistor input impedance: $R_{in} = R_1 \parallel R_2 \parallel [r_\pi + (1+\beta)R'_E]$. For unbypassed emitter, R_{in} is high; for bypassed emitter (C_E shorts R_E), $R_{in} = R_1 \parallel R_2 \parallel r_\pi = R_{Th} \parallel r_\pi$.
- Design Trade-Off: High stability requires small R_{Th} ($R_{Th} \leq 0.1\beta R_E$), which lowers input impedance R_{in}. Engineers balance stability against loading effects.

Comprehensive Biasing Topology Comparison Matrix

- Comparison Parameters Across All 4 Methods: 1. Component Count: Fixed (2 resistors), Collector Feedback (2), Emitter Bias (3), Voltage Divider (4 resistors). 2. Stability Factor S: Fixed $(1+\beta)$, Collector Feedback $(\frac{1+\beta}{1+\beta R_C/(R_B+R_C)})$, Emitter Bias $(\frac{1+\beta}{1+\beta R_E/(R_B+R_E)})$, Voltage Divider $(\approx 1+R_{Th}/R_E)$. 3. β-Dependency: Fixed (Extreme), Collector Feedback (Moderate), Emitter Bias (Low if $\beta R_E \gg R_B$), Voltage Divider (Negligible if $R_{Th} \leq 0.1\beta R_E$). 4. Negative Feedback Type: Fixed (None), Collector Feedback (Voltage Feedback), Emitter Bias (Current Feedback), Voltage Divider (Current Feedback via R_E). 5. Industrial Usage: Fixed (Switching only), Collector Feedback (Simple amplifiers), Emitter Bias (Rare), Voltage Divider (Universal standard).

Summary of Lecture 15 & Unit 2 Conclusion

- Biasing Topologies Evaluated: Fixed Bias, Collector Feedback, Emitter Bias, and Voltage Divider Bias.
- Stability Superiority: Voltage Divider Bias achieves minimum stability factor $S \approx 1 + R_{Th}/R_E$, rendering the Q-point immune to thermal drift and transistor β variations.
- Thevenin Analysis: Simplifies voltage divider bias into $V_{Th} = V_{CC}R_2/(R_1 + R_2)$ and $R_{Th} = R_1 \parallel R_2$, yielding $I_{CQ} \approx (V_{Th} - V_{BE})/R_E$.
- Design Rules Mastered: $V_E = 0.1V_{CC}$, $R_{Th} \leq 0.1\beta R_E$, $V_{CEQ} \approx 0.5V_{CC}$.
- Unit 2 Mastery Complete: Established comprehensive understanding of DC biasing, thermal stability, load line mechanics, and circuit design principles.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Blueprint: Stability Factor Analysis

- Physical Mechanisms of Q-Point Instability & Thermal Sensitivity Parameters.
- Total Differential Formulation of Collector Current $I_C = f(I_{CO}, V_{BE}, \beta)$.
- Mathematical Derivation of Primary Stability Factor $S \equiv \frac{\partial I_C}{\partial I_{CO}}$.
- Mathematical Formulations of Secondary Stability Factors $S'(V_{BE})$ and $S''(\beta)$.
- Derivation & Evaluation of S for Fixed Bias, Collector-to-Base Bias, and Voltage Divider Bias Topologies.
- Design Rules for Minimizing Stability Factors ($R_{TH}/R_E \ll \beta$) & Numerical Worked Examples.

Physical Origin of Q-Point Shift & Thermal Sensitivity

- Reverse Leakage Current Drift: I_{CO} doubles approximately every 10°C rise in silicon junction temperature, governed by $I_{CO}(T) = I_{CO}(T_0) \cdot 2^{(T-T_0)/10}$.
- Base-Emitter Voltage Thermal Coefficient: V_{BE} decreases linearly with temperature at approximately $-2.5\,\text{mV}/^{\circ}\text{C}$, expressed mathematically as $\frac{dV_{BE}}{dT} \approx -2.5\,\text{mV}/^{\circ}\text{C}$.
- Common-Emitter Current Gain Sensitivity: $\beta = h_{FE}$ increases with temperature at approximately $+0.5\%$ to $+1\%$ per $^{\circ}$C due to enhanced minority carrier mobility and lifetime.
- Cumulative Shift in Operating Point: Unchecked shifts in I_C push the Q-point toward saturation ($V_{CE} \to 0$) or cutoff ($I_C \to 0$), severely clipping the AC signal.

Fundamental Collector Current Equation & Total Differential

- General BJT Collector Current Equation: $I_C = \beta I_B + (1+\beta) I_{CO}$, accounting for both base injection current and reverse saturation leakage.
- Total Differential Formulation: $dI_C = \left(\frac{\partial I_C}{\partial I_{CO}}\right) dI_{CO} + \left(\frac{\partial I_C}{\partial V_{BE}}\right) dV_{BE} + \left(\frac{\partial I_C}{\partial \beta}\right) d\beta$.
- Definition of Partial Sensitivity Factors: $dI_C = S \cdot dI_{CO} + S' \cdot dV_{BE} + S'' \cdot d\beta$.
- Superposition Assumption: For small temperature excursions, total quiescent current drift ΔI_C is the linear sum of independent contributions from ΔI_{CO}, ΔV_{BE}, and $\Delta \beta$.

Primary Stability Factor $S(I_{CO})$: General Derivation

- Definition of Primary Stability Factor: $S \equiv \left.\frac{\partial I_C}{\partial I_{CO}}\right|_{V_{BE},\beta=\text{const}}$.
- Differentiating $I_C = \beta I_B + (1+\beta) I_{CO}$ with respect to I_C: $1 = \beta \frac{\partial I_B}{\partial I_C} + (1+\beta)\frac{\partial I_{CO}}{\partial I_C}$.
- Rearranging for $\frac{\partial I_C}{\partial I_{CO}}$ yields the Universal Stability Equation: $S = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$.
- Physical Interpretation: $\frac{\partial I_B}{\partial I_C}$ represents the circuit feedback ratio. A negative feedback ratio $\frac{\partial I_B}{\partial I_C} < 0$ increases the denominator, suppressing S toward its ideal minimum value of 1.

Secondary Stability Factors: $S'(V_{BE})$ and $S''(\beta)$

- Definition of $S'(V_{BE})$: $S' \equiv \left.\frac{\partial I_C}{\partial V_{BE}}\right|_{I_{CO},\beta=\text{const}} = \frac{-\beta/R_{TH}}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)} = \frac{-\beta}{R_{TH}+(1+\beta)R_E}$ (for self-bias).
- Definition of $S''(\beta)$: $S'' \equiv \left.\frac{\partial I_C}{\partial \beta}\right|_{I_{CO},V_{BE}=\text{const}} = \frac{\partial}{\partial \beta}\left[\frac{\beta(V_{TH}-V_{BE})}{R_{TH}+(1+\beta)R_E}\right] = \frac{I_{C1}}{\beta_1(1+\beta_2)} \cdot S_2$.
- Interdependence of Stability Factors: High-stability networks (low S) automatically reduce S' and S'' due to shared denominator terms containing R_E feedback.
- Units and Dimensions: S is dimensionless ($1 \leq S \leq 1+\beta$), S' has units of mA/V (Ω^{-1}), and S'' has units of mA per unit change in β.

Stability Factor S Evaluation: Fixed Bias Circuit

- Fixed Bias KVL Equation: $V_{CC} - I_B R_B - V_{BE} = 0 \implies I_B = \frac{V_{CC} - V_{BE}}{R_B}$.
- Feedback Partial Derivative: Since I_B is completely independent of I_C, $\frac{\partial I_B}{\partial I_C} = 0$.
- Substitution into Universal Formula: $S = \frac{1+\beta}{1-\beta(0)} = 1 + \beta$.
- Numerical Impact: For a transistor with $\beta = 100$, $S = 101$. Any increase in leakage current ΔI_{CO} is multiplied by 101 into ΔI_C, making Fixed Bias extremely thermally unstable.

Stability Factor S Evaluation: Collector-to-Base Feedback Bias

- Collector-to-Base Bias KVL Equation: $V_{CC} - (I_C + I_B)R_C - I_B R_B - V_{BE} = 0$.
- Base Current Expression: $I_B = \frac{V_{CC} - V_{BE} - I_C R_C}{R_B + R_C}$.
- Feedback Partial Derivative: $\frac{\partial I_B}{\partial I_C} = -\frac{R_C}{R_B + R_C}$.
- Stability Factor Derivation: $S = \frac{1+\beta}{1-\beta\left(-\frac{R_C}{R_B+R_C}\right)} = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_B+R_C}\right)}$.
- Performance Bounds: As $R_B \to 0$, $S \to 1$. However, small R_B heavily loads the input AC signal, creating a fundamental trade-off between stability and AC voltage gain.

Stability Factor S Evaluation: Self Bias (Voltage Divider with R_E)

- Thévenin Equivalent Network: $V_{TH} = V_{CC}\frac{R_2}{R_1+R_2}$, $R_{TH} = R_1 \parallel R_2 = \frac{R_1R_2}{R_1+R_2}$.
- Thévenin Loop KVL Equation: $V_{TH} - I_B R_{TH} - V_{BE} - (I_C + I_B)R_E = 0$.
- Differentiating KVL with respect to I_C: $0 - \frac{\partial I_B}{\partial I_C}R_{TH} - 0 - R_E - \frac{\partial I_B}{\partial I_C}R_E = 0 \implies \frac{\partial I_B}{\partial I_C} = -\frac{R_E}{R_{TH}+R_E}$.
- Exact Stability Factor Formula: $S = \frac{(1+\beta)\left(1+\frac{R_{TH}}{R_E}\right)}{1+\beta+\frac{R_{TH}}{R_E}}$.
- Asymptotic Analysis: If $R_{TH}/R_E \ll 1$, then $S \to \frac{(1+\beta)(1)}{1+\beta} = 1$ (ideal thermal stability).

Optimization Strategy: Minimizing S via R_{TH}/R_E Trade-offs

- Design Rule of Thumb: To achieve $S \ll 1 + \beta$, enforce $R_{TH} \leq 0.1 \cdot \beta R_E$ or $R_{TH}/R_E \approx 10$.
- Constraint 1 — DC Bias Stability: Lowering R_{TH} reduces S toward 1, maximizing immunity against thermal runaway.
- Constraint 2 — AC Input Impedance: R_{TH} appears in parallel with transistor input impedance $R_{in} = r_p + (1 + \beta)r_e$. Excessively small R_{TH} shunts the AC signal current to ground.
- Constraint 3 — Power Dissipation: Low R_1, R_2 resistor values increase static standing current drawn directly from the V_{CC} power supply.
- Optimal Balance: Choose R_E to drop 1 V to 2 V ($V_E \approx 0.1 V_{CC}$) and set $R_{TH} = 0.1\beta R_E$ to achieve $S \approx 5 - 10$.

Comparative Matrix of Biasing Topologies & Stability Margins

- Fixed Bias: $S = 1 + \beta$. Extremely poor stability; highly sensitive to temperature and β; simplest component count (1 resistor).
- Collector Feedback Bias: $S = \frac{1+\beta}{1+\beta\frac{R_C}{R_B+R_C}}$. Moderate stability; sensitive to AC voltage gain degradation unless bypassed; 2 resistors.
- Voltage Divider Bias (Self Bias): $S = \frac{(1+\beta)(1+R_{TH}/R_E)}{1+\beta+R_{TH}/R_E}$. Superior thermal stability ($S \approx 2-10$); independent of β variations if $R_{TH}/R_E \ll \beta$; standard industrial choice.
- Emitter Bias (Dual Supply $\pm V$): $S = \frac{(1+\beta)(1+R_B/R_E)}{1+\beta+R_B/R_E}$. Excellent stability; allows direct coupling; requires dual power supply rails.

Numerical Example: Calculating S, S', and S'' for Voltage Divider Bias

- Given Parameters: $V_{CC} = 12\,\text{V}$, $R_1 = 33\,\text{k}\Omega$, $R_2 = 4.7\,\text{k}\Omega$, $R_C = 2.2\,\text{k}\Omega$, $R_E = 1\,\text{k}\Omega$, $\beta = 100$, $V_{BE} = 0.7\,\text{V}$.
- Step 1: Calculate Thévenin Equivalent: $V_{TH} = 12 \times \frac{4.7}{33+4.7} = 1.496\,\text{V}$; $R_{TH} = \frac{33 \times 4.7}{33+4.7} = 4.11\,\text{k}\Omega$.
- Step 2: Calculate Ratio R_{TH}/R_E: $\frac{R_{TH}}{R_E} = \frac{4.11\,\text{k}\Omega}{1\,\text{k}\Omega} = 4.11$.
- Step 3: Calculate Primary Stability Factor S: $S = \frac{(1+100)(1+4.11)}{1+100+4.11} = \frac{101 \times 5.11}{105.11} = 4.91$.
- Step 4: Calculate $S'(V_{BE})$: $S' = \frac{-\beta}{R_{TH}+(1+\beta)R_E} = \frac{-100}{4.11\,\text{k}\Omega+101\,\text{k}\Omega} = -0.951\,\text{mA/V}$.
- Conclusion: $S = 4.91 \ll 101$, demonstrating robust thermal stabilization where leakage current multiplication is reduced by over 95%.

Design Problem: Sizing R_E and R_{TH} for Target Stability $S \leq 5$

- Design Problem Statement: Design a Voltage Divider Bias network for $V_{CC} = 15\,\text{V}$, $I_{CQ} = 2\,\text{mA}$, $V_{CEQ} = 7.5\,\text{V}$, $\beta = 120$, requiring $S \leq 5.0$.
- Step 1: Emitter Voltage Selection: Allocate $V_E = 0.1 V_{CC} = 1.5\,\text{V}$. Therefore, $R_E = \frac{V_E}{I_{CQ}} = \frac{1.5\,\text{V}}{2\,\text{mA}} = 750\,\Omega$.
- Step 2: Solve Stability Equation for R_{TH}: $S = 5 = \frac{(1+120)(1+R_{TH}/750)}{1+120+R_{TH}/750} \implies 5(121 + R_{TH}/750) = 121(1 + R_{TH}/750)$.
- Step 3: Algebraic Solution: $605 + 5(R_{TH}/750) = 121 + 121(R_{TH}/750) \implies 484 = 116(R_{TH}/750) \implies R_{TH} = 3129\,\Omega = 3.13\,\text{k}\Omega$.
- Step 4: Calculate Divider Resistors R_1, R_2: $V_{TH} = V_{BE} + V_E = 0.7 + 1.5 = 2.2\,\text{V}$. $R_1 = R_{TH}\frac{V_{CC}}{V_{TH}} = 3.13\,\text{k}\Omega \times \frac{15}{2.2} = 21.34\,\text{k}\Omega$; $R_2 = \frac{R_1 R_{TH}}{R_1 - R_{TH}} = 3.54\,\text{k}\Omega$.

Summary & Engineering Best Practices for Bias Stability

- Stability Factor Definitions: $S = \partial I_C / \partial I_{CO}$, $S' = \partial I_C / \partial V_{BE}$, $S'' = \partial I_C / \partial \beta$.
- Universal Stability Formula: $S = \frac{1+\beta}{1-\beta(\partial I_B / \partial I_C)}$. Stability depends directly on negative feedback factor $\partial I_B / \partial I_C$.
- Topology Hierarchy: Voltage Divider Bias ($S \approx 3-5$) ¿ Collector Feedback ($S \approx 10-20$) ¿¿¿ Fixed Bias ($S = 1+\beta \approx 100+$).
- Golden Rule of Stable Design: Select $R_E \geq 0.1 V_{CC}/I_C$ and enforce $R_{TH} \leq 0.1\beta R_E$ to guarantee small S and prevent thermal runaway.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Blueprint: Bias Compensation Topologies

- Thermal Drift Mechanisms & Mathematical Dependencies of $V_{BE}(T)$ and $I_{CO}(T)$.
- Diode Compensation Circuitry for V_{BE} Variations: Forward-Biased Diode In-Line Topology.
- Diode Compensation Circuitry for Leakage Current I_{CO}: Reverse-Biased Tracking Diode Topology.
- Thermistor (NTC) Compensation Networks: Circuit Analysis & Resistance Characteristics.
- Sensistor (PTC Silicon Resistor) Compensation Networks in Emitter & Base Circuits.
- Active Current Mirror Compensation in Integrated Analog Circuits & Monolithic Design.
- Comparative Analysis of Passive vs. Active Compensation & Numerical Worked Examples.

Thermal Drift Dynamics of V_{BE}, I_{CO}, and β in Transistors

- Temperature Dependence of V_{BE}: $V_{BE}(T) = V_{BE}(T_0) - k_V(T - T_0)$, where $k_V = \left|\frac{dV_{BE}}{dT}\right| \approx 2.5\,\text{mV}/^\circ\text{C}$.
- Temperature Dependence of Leakage Current: $I_{CO}(T) = I_{CO}(T_0) \cdot 2^{(T-T_0)/10}$, causing exponential growth in leakage power.
- Temperature Dependence of β: $\beta(T) = \beta(T_0)\,[1 + c_T(T - T_0)]$, where $c_T \approx 0.005 - 0.01\,/^\circ\text{C}$.
- Uncompensated Impact: In high-power or wide-temperature applications (-40°C to $+125^\circ$C), passive emitter degeneration alone cannot prevent severe Q-point shifting.

Diode Compensation for V_{BE} Variations: Circuit Operation & Analysis

- Circuit Topology: A forward-biased diode D made of the same semiconductor material (silicon) is connected in series with the base resistor R_B or supply V_{CC}.
- Base Current KVL Equation: $I_B = \frac{V_{CC} - V_D - V_{BE}}{R_B}$, where V_D is the forward voltage drop across the diode.
- Thermal Differential Equation: $\frac{dI_B}{dT} = \frac{1}{R_B}\left(-\frac{dV_D}{dT} - \frac{dV_{BE}}{dT}\right)$.
- Cancellation Condition: If the diode is thermally coupled to the transistor, $\frac{dV_D}{dT} = \frac{dV_{BE}}{dT} = -2.5\,\text{mV}/^\circ\text{C}$.
- Resulting Stability: $\frac{dI_B}{dT} = \frac{1}{R_B}\left(-(-2.5\,\text{mV}/^\circ\text{C}) - (-2.5\,\text{mV}/^\circ\text{C})\right) = 0$, holding I_B and I_C constant despite temperature changes.

Diode Compensation for Reverse Leakage Current I_{CO}

- Circuit Topology: A reverse-biased diode D_1 (fabricated on the same substrate) is connected in parallel with the base-emitter junction or base supply.
- Current Equilibrium Equation: $I_B = I_1 - I_R$, where I_1 is the supply bias current and $I_R = I_0(D_1)$ is the reverse saturation current of diode D_1.
- Collector Current Equation with Compensation: $I_C = \beta I_B + (1+\beta)I_{CO} = \beta(I_1 - I_0) + (1+\beta)I_{CO}$.
- Perfect Diode Matching ($I_0 = I_{CO}$): $I_C = \beta I_1 - \beta I_{CO} + (1+\beta)I_{CO} = \beta I_1 + I_{CO}$.
- Stability Factor Reduction: The multiplier for reverse leakage current is reduced from $(1+\beta)$ down to 1, yielding an effective $S \approx 1$.

Thermistor (NTC) Compensation Networks & Mathematical Formulation

- Negative Temperature Coefficient (NTC) Thermistor Law: $R_T(T) = R_0 \exp\left[B\left(\frac{1}{T} - \frac{1}{T_0}\right)\right]$, where B is the thermistor material constant ($3000\text{K} - 4500\text{K}$).
- Base Divider Topology: NTC thermistor R_T is placed in the lower branch (R_2) of the voltage divider network.
- Circuit Mechanism: As temperature rises, R_T drops exponentially $\implies$ $V_{TH} = V_{CC}\frac{R_T}{R_1+R_T}$ decreases $\implies$ V_B decreases.
- Collector Current Stabilization: The reduction in V_B decreases base current I_B, compensating for the rise in I_C caused by increasing β and I_{CO}.
- Design Formula: Select R_0 and B parameter such that $\frac{dV_{TH}}{dT} = \frac{dV_{BE}}{dT} + I_C\frac{dR_E}{dT}$.

Sensistor (PTC Silicon Resistor) Bias Compensation Networks

- Positive Temperature Coefficient (PTC) Sensistor Law: $R_S(T) = R_0\,[1 + \alpha(T - T_0)]$, where $\alpha \approx +0.7\%$ to $+0.8\%\,/^{\circ}\mathrm{C}$ for heavily doped silicon.
- Emitter Degeneration Topology: Sensistor R_S is connected in series with or replaces the emitter resistor R_E.
- Circuit Mechanism: As temperature rises, R_S increases linearly $\implies$ Emitter degeneration voltage $V_E = I_E R_S$ increases dramatically.
- Negative Feedback Action: Higher V_E reduces base-emitter drive voltage $V_{BE,act} = V_B - V_E$, forcing base current I_B down and stabilizing I_C.
- Base Network Variant: Sensistor placed in series with upper divider resistor R_1 increases R_1 with temperature, lowering V_{TH}.

Active Current Mirror Compensation in Integrated Analog Circuits

- Integrated Circuit Limitation: Monolithic ICs cannot easily integrate large electrolytic bypass capacitors or precise thermistors.
- Current Mirror Topology: Two identical transistors (Q_1 reference, Q_2 output) fabricated on the same silicon die in close physical proximity.
- Reference Current Equation: $I_{REF} = \frac{V_{CC} - V_{BE1}}{R_{REF}}$.
- Output Current Scaling: $I_{OUT} = I_{C2} = I_{REF} \cdot \left(\frac{I_{S2}}{I_{S1}}\right) \frac{1}{1+\frac{2}{\beta}}$.
- Thermal Self-Compensation: Since Q_1 and Q_2 share identical temperature T, $V_{BE1}(T) = V_{BE2}(T)$ and $\beta_1(T) = \beta_2(T)$, making output bias current I_{OUT} virtually immune to temperature and β variations.

Comparative Performance Matrix: Passive vs. Active Compensation

- Emitter Resonator (R_E): Passive negative feedback; moderate stability ($S \approx 3 - 10$); causes AC gain reduction (unless bypassed).
- Diode Compensation (V_{BE}): Active element matching; high thermal tracking accuracy; excellent for class B/AB power stages.
- Diode Compensation (I_{CO}): Active leakage diversion; suppresses S to near 1; ideal for high-temperature germanium/silicon legacy systems.
- NTC Thermistor Network: Passive non-linear network; highly customizable temperature slope; slightly higher component tolerance spread.
- Sensistor Network: Passive linear PTC compensation; excellent linearity over $-55°C$ to $+150°C$; higher cost.
- Current Mirror: Active integrated compensation; near-zero temperature drift; ubiquitous in monolithic IC design.

Thermal Tracking and Component Matching Requirements

- Thermal Coupling Necessity: Compensation diodes or sensing elements MUST be mounted on the same heat sink or semiconductor substrate as the power transistor.
- Thermal Resistance Delay: Spatial separation introduces a thermal time constant $\tau_{th} = R_{th}C_{th}$, causing transient Q-point drift during rapid thermal cycling.
- Semiconductor Junction Matching: Diode forward voltage V_D and V_{BE} must match within $\pm 5\,\text{mV}$ across the entire temperature spectrum.
- Isothermal Layout in ICs: Symmetric placement and common-centroid layout techniques are enforced to eliminate thermal gradients across mirror pairs.

Mathematical Sensitivity Analysis of Compensated Bias Networks

- Compensated Sensitivity Equation: $dI_C = S \cdot dI_{CO} + S' \cdot (dV_{BE} - dV_{comp}) + S'' \cdot d\beta$.
- Ideal Cancellation Condition for V_{BE}: Set $dV_{comp} = dV_{BE} \implies S' \cdot (0) = 0$.
- Sensitivity Reduction Factor: $\eta_{comp} = 1 - \frac{\Delta I_{C,\text{compensated}}}{\Delta I_{C,\text{uncompensated}}}$.
- Typical Performance: High-grade diode compensation achieves $\eta_{comp} > 90\%$, restricting Q-point shift to within $\pm 3\%$ over a 100°C temperature span.

Numerical Example: Diode-Compensated Class AB Power Stage

- Given Parameters: Power BJT with $V_{BE} = 0.7\,\text{V}$ at 25°C, $\frac{dV_{BE}}{dT} = -2.2\,\text{mV}/^\circ\text{C}$. Supply $V_{CC} = 20\,\text{V}$, $R_B = 1.8\,\text{k}\Omega$, $\beta = 80$. Temperature rises to 75°C ($\Delta T = 50^\circ\text{C}$).
- Uncompensated Case: $\Delta V_{BE} = -2.2\,\text{mV}/^\circ\text{C} \times 50^\circ\text{C} = -110\,\text{mV} = -0.11\,\text{V}$.
  $\Delta I_B = \frac{0.11\,\text{V}}{1.8\,\text{k}\Omega} = 61.1\,\mu\text{A} \implies \Delta I_C = 80 \times 61.1\,\mu\text{A} = 4.89\,\text{mA}$.
- Compensated Case (Diode in Series): Diode drop changes by
  $\Delta V_D = -2.2\,\text{mV}/^\circ\text{C} \times 50^\circ\text{C} = -0.11\,\text{V}$.
- Net Voltage across R_B:
  $V_{RB} = V_{CC} - V_D - V_{BE} = 20 - (0.7 - 0.11) - (0.7 - 0.11) = 20 - 0.59 - 0.59 = 18.82\,\text{V}$
  (unchanged from 25°C!).
- Result: $\Delta I_B = 0 \implies \Delta I_C = 0\,\text{mA}$ due to V_{BE} drift, completely preventing thermal bias creep.

Design Problem: NTC Thermistor Selection for Temperature Stabilization

- Problem Statement: Select an NTC thermistor for a base divider network ($R_1 = 10\,\text{k}\Omega$) to maintain $V_B = 2.0\,\text{V}$ at 25°C and drop V_B to 1.85 V at 75°C. Supply $V_{CC} = 12\,\text{V}$.
- Step 1: Calculate Thermistor Resistance at 25°C (298.15 K):
  $V_B = 2.0 = 12 \times \frac{R_T(25)}{10\,\text{k}\Omega + R_T(25)} \implies R_T(25) = 2.0\,\text{k}\Omega.$
- Step 2: Calculate Required Thermistor Resistance at 75°C (348.15 K):
  $V_B = 1.85 = 12 \times \frac{R_T(75)}{10\,\text{k}\Omega + R_T(75)} \implies R_T(75) = 1.822\,\text{k}\Omega.$
- Step 3: Calculate Required B Constant:
  $\ln\left(\frac{R_T(75)}{R_T(25)}\right) = B\left(\frac{1}{348.15} - \frac{1}{298.15}\right) \implies \ln(0.911) = B(-0.0004818) \implies B = 193\,\text{K}.$
- Engineering Selection: Pair standard 2.2 kΩ NTC ($B = 3950\,\text{K}$) with parallel fixed resistor to match target slope.

Summary & Selection Criteria for Compensation Networks

- Diode Compensation (V_{BE}): Best for Class A/AB audio & RF power amplifiers; matches linear junction drop $-2.5\,\text{mV}/^{\circ}\text{C}$.
- Diode Compensation (I_{CO}): Best for high-leakage legacy or high-temperature power transistors; suppresses S multiplier to 1.
- NTC/PTC Networks: Highly flexible passive compensation for custom temperature profiling over extended environmental ranges.
- Current Mirrors: Universal standard for monolithic integrated analog circuits (Op-Amps, OTAs, RFICs).
- Golden Design Rule: Always ensure intimate thermal coupling between compensation sensors and power devices to prevent thermal lag.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Blueprint: Thermal Mechanics & Stability

- Physical Mechanism & Positive Feedback Loop of Thermal Runaway.
- Junction Temperature Ratings ($T_{J,\max}$) & Silicon vs Germanium Package Limits.
- Quantitative Definition of Thermal Resistance ($\theta_{JA}, \theta_{JC}, \theta_{CS}, \theta_{SA}$).
- Electrical Circuit Analogy of Thermal Networks (Ohm's Law Analogy).
- Mathematical Derivation of Fundamental Thermal Stability Criterion $\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$.
- Derivation of the $V_{CE} \leq \frac{1}{2} V_{CC}$ Rule for Self-Biased Amplifiers.
- Power Transistor Derating Curves & Numerical Calculation Worked Examples.

Physical Mechanism of Thermal Runaway in BJTs

- Power Dissipation at Collector Junction: $P_D = V_{CE}I_C + V_{BE}I_B \approx V_{CE}I_C$.
- The Self-Reinforcing Positive Feedback Loop: Temperature Rise ($T_J \uparrow$) $\implies$ Leakage Current Increase ($I_{CO} \uparrow$) $\implies$ Collector Current Rise ($I_C \uparrow$) $\implies$ Power Dissipation Increase ($P_D \uparrow$) $\implies$ Further Temperature Rise ($T_J \uparrow\uparrow$).
- Destructive Junction Melting: Unchecked junction temperature exceeding $T_{J,\text{max}}$ ($150^\circ\text{C} - 200^\circ\text{C}$ for Silicon) causes permanent lattice destruction, bond rupturing, and short-circuit failure.
- Dominant Risk Factors: High ambient temperatures, inadequate heat sinking, high collector voltages ($V_{CE} > \frac{1}{2}V_{CC}$), and fixed-bias circuit topologies.

Quantitative Definition of Thermal Resistance (θ)

- Thermal Resistance Definition: $\theta \equiv \frac{\Delta T}{P_D} = \frac{T_1 - T_2}{P_D}$, measured in units of °C/W (degrees Celsius per watt).
- Junction-to-Case Resistance (θ_{JC}): Internal thermal impedance between silicon die junction and package case; fixed by semiconductor manufacturer.
- Case-to-Sink Resistance (θ_{CS}): Contact thermal impedance between transistor case and heat sink surface; dependent on thermal grease / mica washer mounting.
- Sink-to-Ambient Resistance (θ_{SA}): Convective & radiative thermal impedance from heat sink to ambient air; dependent on fin surface area and air flow.
- Total Junction-to-Ambient Resistance: $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA}$.

Electrical Circuit Analogy of Thermal Networks

- Thermal-Electrical Equivalence Parameters:
- • Heat Dissipation Power P_D (Watts) $\equiv$ Electrical Current I (Amperes).
- • Temperature T ($^\circ$C or K) $\equiv$ Electrical Voltage V (Volts).
- • Thermal Resistance θ ($^\circ$C/W) $\equiv$ Electrical Resistance R (Ohms).
- • Thermal Capacitance C_{th} (Joules/$^\circ$C) $\equiv$ Electrical Capacitance C (Farads).
- Fundamental Node Voltage Equation: $T_J - T_A = P_D \cdot \theta_{JA} = P_D \cdot (\theta_{JC} + \theta_{CS} + \theta_{SA})$.
- Equivalent Circuit Schematic: Current source P_D flowing through series resistors θ_{JC}, θ_{CS}, θ_{SA} anchored to ground potential T_A.

Mathematical Derivation of Fundamental Thermal Stability Condition

- Heat Generation Rate: $P_D = f(T_J)$ (power dissipated by the junction as a function of temperature).
- Heat Dissipation Rate (Removal): $P_R = \frac{T_J - T_A}{\theta_{JA}}$ (power transferred to ambient atmosphere).
- Thermal Equilibrium Condition: At steady state, $P_D = P_R \implies T_J = T_A + P_D\theta_{JA}$.
- Stability Criterion against Thermal Perturbation: To prevent runaway, the rate of increase of heat generation must be LESS than the rate of increase of heat removal.
- Mathematical Inequality: $\frac{\partial P_D}{\partial T_J} < \frac{\partial P_R}{\partial T_J} \implies \frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$.
- Physical Meaning: If $\frac{\partial P_D}{\partial T_J} \geq \frac{1}{\theta_{JA}}$, any infinitesimal temperature spike generates more heat than can be radiated, triggering runaway.

Collector Power Dissipation Derivative & Circuit Parameters

- Collector Power Dissipation: $P_D = V_{CE} I_C$.
- Chain Rule Expansion with respect to Junction Temperature T_J: $\frac{\partial P_D}{\partial T_J} = \frac{\partial (V_{CE} I_C)}{\partial T_J} = V_{CE} \frac{\partial I_C}{\partial T_J} + I_C \frac{\partial V_{CE}}{\partial T_J}$.
- Relating V_{CE} to I_C via KVL Loop: In a common emitter stage, $V_{CE} = V_{CC} - I_C(R_C + R_E) \implies \frac{\partial V_{CE}}{\partial I_C} = -(R_C + R_E)$.
- Substituting $\frac{\partial V_{CE}}{\partial T_J} = \frac{\partial V_{CE}}{\partial I_C} \frac{\partial I_C}{\partial T_J} = -(R_C + R_E) \frac{\partial I_C}{\partial T_J}$:
- Simplified Power Derivative: $\frac{\partial P_D}{\partial T_J} = V_{CE} \frac{\partial I_C}{\partial T_J} - I_C(R_C + R_E) \frac{\partial I_C}{\partial T_J} = \frac{\partial I_C}{\partial T_J} [V_{CE} - I_C(R_C + R_E)]$.

Derivation of the Self-Bias Thermal Stability Condition ($V_{CE} \leq \frac{1}{2}V_{CC}$)

- Expressing $I_C(R_C + R_E)$ from DC KVL: $I_C(R_C + R_E) = V_{CC} - V_{CE}$.
- Substitute into Power Derivative: $\frac{\partial P_D}{\partial T_J} = \frac{\partial I_C}{\partial T_J}[V_{CE} - (V_{CC} - V_{CE})] = \frac{\partial I_C}{\partial T_J}[2V_{CE} - V_{CC}]$.
- Evaluating Condition for Negative or Zero Heat Derivative ($\frac{\partial P_D}{\partial T_J} \leq 0$):
- Since $\frac{\partial I_C}{\partial T_J} > 0$, we require $2V_{CE} - V_{CC} \leq 0 \implies V_{CE} \leq \frac{1}{2}V_{CC}$.
- Engineering Consequence: When $V_{CE} < \frac{1}{2}V_{CC}$, any increase in I_C due to temperature causes V_{CE} to decrease so rapidly that total power $P_D = V_{CE}I_C$ ACTUALLY DECREASES! Thermal runaway becomes physically impossible.

Power Transistor Derating Curves & Maximum Dissipation

- Maximum Power Dissipation Rating ($P_{D,\max}$): Datasheet power rating specified at case temperature $T_C = 25^\circ\text{C}$, given by $P_{D,\max}(25^\circ\text{C}) = \frac{T_{J,\max} - 25^\circ\text{C}}{\theta_{JC}}$.
- Thermal Derating Region ($T_C > 25^\circ\text{C}$): As case/ambient temperature increases, allowable power dissipation decreases linearly to zero at $T_{J,\max}$.
- Power Derating Equation: $P_{D,\max}(T_A) = \frac{T_{J,\max} - T_A}{\theta_{JA}} = \frac{T_{J,\max} - T_A}{\theta_{JC} + \theta_{CS} + \theta_{SA}}$.
- Derating Slope Factor: Derating Factor $= \frac{1}{\theta_{JA}}$ (in $\text{W}/^\circ\text{C}$).
- Safe Operating Area (SOA): Enforces simultaneous constraints on maximum voltage $V_{CE,\max}$, peak current $I_{C,\max}$, thermal power dissipation limit $P_{D,\max}$, and secondary breakdown boundary.

Transient Thermal Impedance & Pulse Power Handling

- Thermal Mass & Heat Capacity: Semiconductor die and copper headers possess thermal capacitance $C_{th} = m \cdot c_p$ (Joules/°C).
- Transient Thermal Impedance $Z_{\theta JA}(t)$: For short power pulses ($t_p \ll \tau_{th}$), the effective thermal resistance is significantly lower than steady-state θ_{JA}.
- Thermal Time Constant: $\tau_{th} = \theta_{JA} \cdot C_{th}$. Typical die time constants range from 100 μs to 10 ms, while heat sinks range from 10 s to 100 s.
- Pulsed Power Application: Allows power transistors to handle transient peak power pulses (e.g. 500W for 1ms) far exceeding their continuous DC power rating (e.g. 50W).

Role of Emitter Resistor R_E and Stability Factor S in Preventing Thermal Runaway

- Collector Current Temperature Derivative: $\frac{\partial I_C}{\partial T_J} = S \cdot \frac{\partial I_{CO}}{\partial T_J} + S' \cdot \frac{\partial V_{BE}}{\partial T_J} + S'' \cdot \frac{\partial \beta}{\partial T_J}$.
- Impact of Stability Factor S: Minimizing S directly reduces $\frac{\partial I_C}{\partial T_J}$.
- Evaluating Thermal Runaway Criterion: $\left(S \frac{\partial I_{CO}}{\partial T_J} + S' \frac{\partial V_{BE}}{\partial T_J}\right)(2V_{CE} - V_{CC}) < \frac{1}{\theta_{JA}}$.
- Emitter Resistor Degeneration: Adding R_E increases total loop resistance $(R_C + R_E)$ and reduces S, providing dual protection against thermal runaway.
- Design Summary: Achieving thermal stability requires both appropriate electrical bias design $(S \leq 5)$ and proper physical thermal dissipation design (θ_{SA} sizing).

Numerical Example: Junction Temperature & Power Rating Calculation

- Given Parameters: Silicon power transistor with $T_{J,\max} = 175^\circ\text{C}$, $\theta_{JC} = 1.5^\circ\text{C/W}$. Mounted on heat sink with thermal washer $\theta_{CS} = 0.5^\circ\text{C/W}$ and heat sink rating $\theta_{SA} = 2.0^\circ\text{C/W}$. Ambient temperature $T_A = 40^\circ\text{C}$. Transistor dissipates $P_D = 30\,\text{W}$.
- Step 1: Calculate Total Thermal Resistance θ_{JA}:
  $\theta_{JA} = \theta_{JC} + \theta_{CS} + \theta_{SA} = 1.5 + 0.5 + 2.0 = 4.0^\circ\text{C/W}$.
- Step 2: Calculate Operating Junction Temperature T_J:
  $T_J = T_A + P_D \cdot \theta_{JA} = 40^\circ\text{C} + (30\,\text{W} \times 4.0^\circ\text{C/W}) = 40^\circ\text{C} + 120^\circ\text{C} = 160^\circ\text{C}$.
- Step 3: Evaluate Safety Margin: $T_J = 160^\circ\text{C} < T_{J,\max} = 175^\circ\text{C}$. The design operates safely with a 15°C thermal headroom.
- Step 4: Calculate Maximum Allowable Power at $T_A = 40^\circ\text{C}$: $P_{D,\max} = \frac{175-40}{4.0} = \frac{135}{4.0} = 33.75\,\text{W}$.

Numerical Example: Thermal Runaway Threshold Determination

- Given Circuit: BJT biased at $V_{CC} = 24\,\text{V}$, $V_{CE} = 16\,\text{V}$, $I_C = 1.5\,\text{A}$. $R_C + R_E = 5.33\,\Omega$. Total thermal resistance $\theta_{JA} = 3.0^\circ\text{C/W}$. Measured collector current drift rate $\frac{\partial I_C}{\partial T_J} = 12\,\text{mA}/^\circ\text{C} = 0.012\,\text{A}/^\circ\text{C}$.
- Step 1: Check V_{CE} relative to $\frac{1}{2}V_{CC}$: $\frac{1}{2}V_{CC} = 12\,\text{V}$. Since $V_{CE} = 16\,\text{V} > 12\,\text{V}$, $\frac{\partial P_D}{\partial T_J} > 0$ and thermal runaway is POSSIBLY RISKY.
- Step 2: Calculate Power Dissipation Derivative $\frac{\partial P_D}{\partial T_J}$: $\frac{\partial P_D}{\partial T_J} = \frac{\partial I_C}{\partial T_J}(2V_{CE} - V_{CC}) = 0.012\,\text{A}/^\circ\text{C} \times (2(16) - 24) = 0.012 \times (32 - 24) = 0.096\,\text{W}/^\circ\text{C}$.
- Step 3: Calculate Heat Dissipation Capability $\frac{1}{\theta_{JA}}$: $\frac{1}{\theta_{JA}} = \frac{1}{3.0^\circ\text{C/W}} = 0.333\,\text{W}/^\circ\text{C}$.
- Step 4: Test Thermal Stability Inequality: $\frac{\partial P_D}{\partial T_J} = 0.096\,\text{W}/^\circ\text{C} < \frac{1}{\theta_{JA}} = 0.333\,\text{W}/^\circ\text{C}$.
- Conclusion: The system is THERMALLY STABLE because heat removal capability ($0.333\,\text{W}/^\circ\text{C}$) exceeds internal heat generation growth ($0.096\,\text{W}/^\circ\text{C}$).

Summary & Core Principles of Thermal Design

- Thermal Runaway Mechanism: Uncontrolled thermal feedback loop driven by exponential I_{CO} and V_{BE} thermal drift.
- Thermal Resistance Network: Junction temperature $T_J = T_A + P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$.
- Universal Stability Criterion: Must enforce $\frac{\partial P_D}{\partial T_J} < \frac{1}{\theta_{JA}}$ under all operating conditions.
- Half-Supply Voltage Rule: Biasing at $V_{CE} \leq \frac{1}{2} V_{CC}$ makes $\frac{\partial P_D}{\partial T_J} \leq 0$, rendering thermal runaway physically impossible.
- Integrated Design Strategy: Combine electrical bias stabilization ($S \leq 5$) with properly sized heat sinking (low θ_{SA}) to guarantee lifetime reliability.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Blueprint: Thermal Management & Heat Sink Types

- Fundamentals of Heat Transfer Modes: Conduction, Convection, and Thermal Radiation.
- Thermal Interface Materials (TIM): Greases, Phase-Change Materials, Elastomeric Pads, and Gap Fillers.
- Analysis of Thermal Contact Resistance θ_{CS} & Mounting Torque Effects.
- Classification & Architecture of Heat Sinks: Stamped, Extruded, Pin-Fin, and Skived-Fin.
- Advanced Cooling Topologies: Two-Phase Vapor Chambers, Heat Pipes, and Liquid Cold Plates.
- Natural Convection vs. Forced Air Convection Volumetric Performance.
- Heat Sink Sizing Equation Methodology (θ_{SA} Calculation) & Worked Examples.

Fundamentals of Heat Transfer Mechanisms in Electronics

- Conduction (Solid Material Transfer): Heat flow through solid silicon, copper flange, and aluminum heat sink body, governed by Fourier's Law.
- Convection (Fluid/Air Interface Transfer): Heat dissipation from heat sink fins to surrounding air, governed by Newton's Law of Cooling.
- Radiation (Electromagnetic Waves): Direct infrared radiative heat loss from heat sink surface to surrounding enclosures, governed by Stefan-Boltzmann Law.
- Dominant Mode in Heat Sinks: Convection across fin surface area accounts for $80\% - 90\%$ of total heat dissipation in forced air systems.

Governing Equations of Thermal Dissipation Modes

- Fourier's Law of Conduction: $Q_{cond} = -kA\frac{dT}{dx} = \frac{kA}{L}(T_1 - T_2) \implies \theta_{cond} = \frac{L}{kA}$ (°C/W), where k is thermal conductivity (W/m · K).
- Newton's Law of Convection: $Q_{conv} = hA_{surface}(T_s - T_\infty) \implies \theta_{conv} = \frac{1}{hA_{surface}}$, where h is heat transfer coefficient ($W/m^2 \cdot K$).
- Stefan-Boltzmann Law of Radiation: $Q_{rad} = \epsilon\sigma A_{surface}(T_s^4 - T_{surr}^4)$, where ϵ is surface emissivity ($0.85 - 0.95$ for black anodized aluminum) and $\sigma = 5.67 \times 10^{-8}\,W/m^2K^4$.
- Combined Sink Resistance Equation: $\theta_{SA} = \frac{1}{hA_{fin} + h_{rad}A_{rad}}$.

Thermal Interface Materials (TIM) and Thermal Contact Resistance θ_{CS}

- Microscopic Surface Imperfections: Microscopic air gaps ($k_{air} \approx 0.026\,\mathrm{W/m \cdot K}$) between transistor case and heat sink create high thermal contact resistance.
- Role of Thermal Interface Material: TIM displaces air voids with higher conductivity compounds ($k_{TIM} \approx 1.5 - 8.0\,\mathrm{W/m \cdot K}$).
- Primary Classes of TIM Materials:
- • Thermal Greases / Pastes: Lowest thermal impedance ($0.05 - 0.15^\circ\mathrm{C \cdot in^2/W}$); requires manual application.
- • Phase-Change Materials (PCM): Melts at $45 - 60^\circ\mathrm{C}$ to fill microscopic voids; clean automated application.
- • Elastomeric Silicone Pads: Provides electrical isolation with moderate thermal resistance ($0.5 - 1.5^\circ\mathrm{C/W}$).
- • Graphite / Gap Fillers: Compressible thick pads for bridging large mechanical tolerances.

Mounting Hardware, Torque Controls, and θ_{CS} Optimization

- Impact of Mounting Pressure: Increasing clamping pressure compresses TIM, reducing bond-line thickness (BLT) and lowering θ_{CS}.
- Optimal Torque Specification: Screw-mounted packages (TO-220, TO-247) require $0.5 - 0.8\,\mathrm{N \cdot m}$ mounting torque.
- Over-Torquing Hazard: Excessive torque warps the copper header tab, bowing the contact surface away from the heat sink and INCREASING θ_{CS}.
- Spring Clip Mounting: Provides constant uniform clamping pressure across thermal cycles, compensating for thermal expansion stress.

Extruded & Stamped Heat Sinks: Structure & Performance

- Stamped Heat Sinks: Fabricated by stamping thin aluminum or copper sheets ($0.5 - 1.5\,\text{mA}$ thick). Low cost; suited for low-power board-level components ($P_D < 5\,\text{W}$, $\theta_{SA} \approx 10 - 25^\circ\text{C/W}$).
- Extruded Aluminum Heat Sinks (6063-T5): Fabricated by forcing hot aluminum billets through shaped dies. High thermal conductivity ($k \approx 200\,\text{W/m} \cdot \text{K}$).
- Fin Design Profiles: Straight vertical fins optimize natural convection chimney effects. Aspect ratios (fin height to gap width) typically reach $8:1$ to $10:1$.
- Application Window: Standard choice for medium-to-high power amplifiers ($P_D = 10\,\text{W} - 100\,\text{W}$, $\theta_{SA} \approx 0.5 - 5.0^\circ\text{C/W}$).

High-Density Surface Architectures: Pin-Fin & Skived-Fin

- Pin-Fin Heat Sinks: Array of round, square, or elliptical pins. Omnidirectional air flow capability; disrupts boundary layers to increase convective heat transfer coefficient h.
- Skived-Fin Heat Sinks: Produced by shaving thin, continuous fins directly from a solid copper or aluminum block using a precision blade.
- High Aspect Ratio Advantage: Enables extremely dense fin spacing with aspect ratios up to $25:1$ and zero thermal interface resistance between fins and base plate.
- Material Advantage of Copper: Skived copper heat sinks ($k \approx 390\,\mathrm{W/m \cdot K}$) provide double the thermal conductivity of aluminum, ideal for space-constrained high-flux power density.

Two-Phase Passive Cooling: Heat Pipes & Vapor Chambers

- Phase Change Thermodynamics: Utilizes latent heat of vaporization of working fluid (water/alcohol under vacuum) to transport heat with near-zero temperature drop.
- Operation Cycle: Liquid vaporizes at hot evaporator interface $\rightarrow$ Vapor travels at high speed to cold condenser section $\rightarrow$ Vapor condenses releasing latent heat $\rightarrow$ Liquid returns to evaporator via capillary wick action.
- Effective Thermal Conductivity: Ultra-high equivalent conductivity ($k_{eq} \approx 5,000 - 50,000\,\mathrm{W/m \cdot K}$), $10\times - 100\times$ higher than solid copper.
- Vapor Chamber Application: Planar 2D heat spreader placed directly under high-power density chips to eliminate localized thermal hot spots.

Forced Air Convection vs. Natural Convection Performance Dynamics

- Natural Convection: Driven solely by buoyant forces of heated air ($v_{air} \approx 0.1 - 0.5\,\mathrm{m/s}$). Convective coefficient $h \approx 5 - 15\,\mathrm{W/m^2 \cdot K}$. Requires wide fin spacing ($5 - 10\,\mathrm{mm}$) to prevent boundary layer overlap.
- Forced Air Convection: Driven by fans/blowers ($v_{air} \approx 2.0 - 5.0\,\mathrm{m/s}$). Convective coefficient $h \approx 30 - 150\,\mathrm{W/m^2 \cdot K}$ ($5\times - 10\times$ increase!).
- Thermal Resistance Reduction: Forced airflow reduces θ_{SA} of an extruded heat sink by $60\% - 75\%$ compared to natural convection.
- Pressure Drop Trade-off: Denser fin spacing increases airflow impedance, requiring higher static pressure fans.

Liquid Cooling Cold Plates & Direct Substrate Management

- Liquid Cold Plate Architecture: Internal microchannels machined into copper/aluminum blocks connected to a closed-loop liquid pump, radiator, and reservoir.
- Coolant Properties: Water/glycol mixtures possess $4\times$ higher specific heat capacity ($c_p \approx 4184\,\mathrm{J/kg \cdot K}$) and $25\times$ higher thermal conductivity than air.
- Performance Metric: Achieves extremely low thermal resistances ($\theta_{SA} < 0.05^\circ\mathrm{C/W}$).
- Application Scope: Essential for high-power electronics ($> 500\,\mathrm{W}$ to several kW) such as EV inverters, motor drives, server racks, and high-power RF transmitters.

Numerical Example: Step-by-Step Heat Sink Sizing Calculation (θ_{SA})

- Given Requirements: Transistor TO-247 package dissipating $P_D = 45\,\text{W}$. Maximum junction temperature $T_{J,\text{max}} = 150^\circ\text{C}$. Maximum ambient temperature $T_A = 50^\circ\text{C}$. Transistor datasheet specifies $\theta_{JC} = 0.8^\circ\text{C/W}$. Mounted with thermal grease and mica washer $\theta_{CS} = 0.4^\circ\text{C/W}$.
- Step 1: Calculate Maximum Allowable Total Thermal Resistance $\theta_{JA,\text{max}}$:
- $\theta_{JA,\text{max}} = \frac{T_{J,\text{max}} - T_A}{P_D} = \frac{150^\circ\text{C} - 50^\circ\text{C}}{45\,\text{W}} = \frac{100^\circ\text{C}}{45\,\text{W}} = 2.22^\circ\text{C/W}.$
- Step 2: Solve for Maximum Allowable Heat Sink Thermal Resistance θ_{SA}:
- $\theta_{SA,\text{max}} = \theta_{JA,\text{max}} - \theta_{JC} - \theta_{CS} = 2.22 - 0.8 - 0.4 = 1.02^\circ\text{C/W}.$
- Step 3: Heat Sink Selection: Select a commercial catalog heat sink rating $\theta_{SA} \leq 1.0^\circ\text{C/W}$ under natural convection or $\leq 0.4^\circ\text{C/W}$ under forced air.

Numerical Example: Evaluating TIM Impact on Junction Temperature

- Comparison Scenario: Same 45 W transistor setup with $\theta_{SA} = 1.0^\circ\text{C/W}$, $\theta_{JC} = 0.8^\circ\text{C/W}$, $T_A = 50^\circ\text{C}$.
- Option A — High-Grade Thermal Grease: $\theta_{CS} = 0.2^\circ\text{C/W}$.
- • Total $\theta_{JA} = 0.8 + 0.2 + 1.0 = 2.0^\circ\text{C/W}$.
- • Junction Temp $T_J = 50^\circ\text{C} + (45\,\text{W} \times 2.0^\circ\text{C/W}) = 50 + 90 = 140^\circ\text{C}$ (SAFE!).
- Option B — Dry Joint without TIM: Microscopic air gaps yield $\theta_{CS} = 1.8^\circ\text{C/W}$.
- • Total $\theta_{JA} = 0.8 + 1.8 + 1.0 = 3.6^\circ\text{C/W}$.
- • Junction Temp $T_J = 50^\circ\text{C} + (45\,\text{W} \times 3.6^\circ\text{C/W}) = 50 + 162 = 212^\circ\text{C}$ (DESTRUCTIVE FAILURE!).
- Conclusion: Omitting thermal interface grease increases T_J by 72°C, causing catastrophic thermal destruction.

Summary & Heat Sink Selection Matrix

- Sizing Formula: $\theta_{SA} = \frac{T_{J,\max} - T_A}{P_D} - \theta_{JC} - \theta_{CS}$.
- Low Power ($< 5\,\text{W}$): Stamped sheet metal heat sinks or direct PCB copper pour plane.
- Medium Power ($5\,\text{W} - 100\,\text{W}$): Extruded aluminum heat sinks with natural or forced convection.
- High Power Density ($100\,\text{W} - 300\,\text{W}$): Skived copper pin-fin heat sinks with heat pipe vapor chambers.
- Ultra Power ($> 300\,\text{W}$): Closed-loop liquid cooling cold plates.
- Golden Rule: Always specify high-grade TIM ($k_{TIM} > 2.0\,\text{W/m} \cdot \text{K}$) and apply proper mounting torque to minimize θ_{CS}.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Blueprint: Amplifier Parameters & Frequency Response

- Fundamental Amplifier Gain Definitions: Voltage, Current, Transconductance, Transresistance.
- Decibel (dB) Scale Representation & Logarithmic Bode Plot Curves.
- Low-Frequency Response (f_L): Coupling (C_{C1}, C_{C2}) & Emitter Bypass (C_E) Capacitor Poles.
- High-Frequency Response (f_H): Stray Parasitic & Transistor Junction Capacitances (C_π, C_μ).
- Bandwidth (BW) & Half-Power (-3 dB) Corner Frequency Definitions.
- The Gain-Bandwidth Product (GBP) & High-Frequency Hybrid-\{}pi$ Model.
- Transition Frequency (f_T) Derivation & The Miller Effect Theorem.
- Feedback Effects on Gain-Bandwidth Trade-Offs & Worked Numerical Problems.

Fundamental Amplifier Gain Parameters

- Voltage Gain (A_v): Ratio of AC output voltage to AC input voltage: $A_v = \frac{v_{out}}{v_{in}} = \frac{v_o}{v_i}$ (Dimensionless).
- Current Gain (A_i): Ratio of AC output current to AC input current: $A_i = \frac{i_{out}}{i_{in}} = \frac{i_o}{i_i}$ (Dimensionless).
- Transconductance Gain (G_m): Ratio of AC output current to AC input voltage: $G_m = \frac{i_{out}}{v_{in}}$ (Units: Siemens, S or Ω^{-1}).
- Transresistance Gain (R_m): Ratio of AC output voltage to AC input current: $R_m = \frac{v_{out}}{i_{in}}$ (Units: Ohms, Ω).
- Power Gain (A_p): Ratio of AC output power to AC input power: $A_p = \frac{P_{out}}{P_{in}} = A_v \cdot A_i$.

Decibel (dB) Scale Representation & Logarithmic Bode Curves

- Voltage Gain in Decibels: $A_{v,\text{dB}} = 20\log_{10}|A_v| = 20\log_{10}\left|\frac{v_o}{v_i}\right|$.
- Power Gain in Decibels: $A_{p,\text{dB}} = 10\log_{10}A_p = 10\log_{10}\left(\frac{P_o}{P_i}\right)$.
- Half-Power (-3 dB) Point Definition: Frequency at which output power drops to half its midband value ($P_{out} = 0.5P_{mid}$), corresponding to voltage magnitude dropping to $\frac{1}{\sqrt{2}} \approx 0.707$ of midband voltage gain (A_{mid}).
- Decibel Loss at Cutoff: $20\log_{10}(0.7071) = -3.0103\,\text{dB} \approx -3\,\text{dB}$.
- Bode Plot Slope Rates: Single-pole RC roll-off produces a attenuation slope of $-20\,\text{dB/decade}$ ($-6\,\text{dB/octave}$).

Low-Frequency Cutoff (f_L) Dynamics: Coupling & Bypass Capacitors

- Low-Frequency Attenuation Mechanism: At low frequencies ($f \to 0$), capacitive reactances $X_C = \frac{1}{2\pi f C} \to \infty$, acting as open circuits that attenuate signals.
- Input Coupling Capacitor Pole (C_{C1}): Forms high-pass filter with total input resistance $R'_{in} = R_{sig} + (R_1 \parallel R_2 \parallel r_p)$: $f_{L1} = \frac{1}{2\pi(R_{sig}+R_{in})C_{C1}}$.
- Output Coupling Capacitor Pole (C_{C2}): Forms high-pass filter with load resistance: $f_{L2} = \frac{1}{2\pi(R_C+R_L)C_{C2}}$.
- Emitter Bypass Capacitor Pole (C_E): Bypasses emitter resistor R_E. Resistance looking into emitter is $R'_e = R_E \parallel \left[r_e + \frac{R_{TH} \parallel R_{sig}}{1+\beta}\right]$: $f_{LE} = \frac{1}{2\pi R'_e C_E}$.
- Overall Lower Cutoff Frequency: Dominant pole approximation: $f_L \approx \sqrt{f_{L1}^2 + f_{L2}^2 + f_{LE}^2}$ or $f_L \approx f_{L1} + f_{L2} + f_{LE}$.

High-Frequency Cutoff (f_H) Dynamics: Parasitic Junction Capacitances

- High-Frequency Attenuation Mechanism: At high frequencies ($f \to \infty$), parasitic internal junction reactances $X_C = \frac{1}{2\pi fC} \to 0$, shorting AC signals to ground.
- Base-Emitter Diffusion & Transition Capacitance (C_π or C_{be}): Forward-biased base-emitter junction capacitance ($10\,\text{pF} - 100\,\text{pF}$).
- Base-Collector Depletion Capacitance (C_μ or C_{bc}): Reverse-biased base-collector junction capacitance ($1\,\text{pF} - 5\,\text{pF}$).
- Stray Wiring Capacitance ($C_{w,in}$, $C_{w,out}$): Parasitic PCB trace capacitances ($2\,\text{pF} - 10\,\text{pF}$).
- Overall Upper Cutoff Frequency (f_H): Set by internal low-pass RC network poles: $f_H = \frac{1}{2\pi R_{in,eq} C_{in,total}}$.

Bandwidth (BW) & Midband Operational Range

- Bandwidth Definition: The continuous range of signal frequencies over which amplifier gain remains within 3 dB of its peak midband gain A_{mid}.
- Mathematical Formula: $BW = f_H - f_L$.
- Wideband Approximation ($f_H \gg f_L$): For standard audio and video amplifiers where $f_H \geq 100 f_L$, $BW \approx f_H$.
- Midband Region Characteristics: Frequency range where external capacitors (C_{C1}, C_{C2}, C_E) act as perfect AC short circuits AND internal capacitors (C_π, C_μ) act as perfect AC open circuits, yielding constant gain A_{mid} and zero phase shift distortion.

The Gain-Bandwidth Product (GBP/f_T): Invariance Principle

- Gain-Bandwidth Product Definition: $GBP \equiv |A_{mid}| \times BW \approx |A_{mid}| \times f_H$.
- Fundamental Invariance Principle: For a single-pole amplifier system, the product of midband voltage gain and bandwidth is a CONSTANT parameter dictated by internal transistor physics.
- Gain vs. Bandwidth Trade-Off: Increasing midband gain $|A_{mid}|$ proportionally decreases bandwidth BW; trading gain extends bandwidth.
- Transition Frequency (f_T): Frequency at which short-circuit common-emitter current gain drops to unity ($|h_{fe}(f_T)| = 1$). f_T represents the absolute maximum theoretical GBP of the device.

High-Frequency Hybrid-\{}pi Transistor Model Parameters

- Hybrid-\{}pi Model Components: Replaces low-frequency h-parameter model for high-frequency dynamic AC circuit analysis.
- Base Spreading Resistance ($r_b b'$ or r_x): Ohmic resistance of bulk base semiconductor material between base terminal and active junction ($20\,\Omega - 100\,\Omega$).
- Internal Base-Emitter Resistance ($r'_b e$ or r_π): Dynamic resistance of forward-biased base-emitter junction: $r_\pi = \frac{\beta_0}{g_m} = \frac{\beta_0 V_T}{I_{CQ}}$.
- Transconductance (g_m): $g_m = \frac{I_{CQ}}{V_T} = \frac{I_{CQ}}{26\,\text{mV}}$ at room temperature (25°C).
- Junction Capacitances: $C_{b'e} = C_\pi$ (diffusion + depletion) and $C_{b'c} = C_\mu$ (collector overlap depletion).

Transition Frequency (f_T) Derivation & Hybrid-\{}pi Equation

- Short-Circuit Current Gain Formulation: Output short-circuited ($R_L = 0 \implies v_{ce} = 0$). Output current $i_o = -g_m v_{b'e}$.
- Input Current Equation: $i_i = v_{b'e} \cdot \left[\frac{1}{r_\pi} + j2\pi f(C_\pi + C_\mu)\right]$.
- Short-Circuit Current Gain Expression: $A_{i,sc}(f) = \frac{i_o}{i_i} = \frac{-g_m}{\frac{1}{r_\pi} + j2\pi f(C_\pi + C_\mu)} = \frac{-h_{fe0}}{1+j\frac{f}{f_\beta}}$, where $f_\beta = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)}$ is the β-cutoff frequency.
- Setting $|A_{i,sc}(f_T)| = 1$: At $f = f_T \gg f_\beta$, $|A_{i,sc}| \approx \frac{g_m}{2\pi f_T (C_\pi + C_\mu)} = 1$.
- Transition Frequency Formula: $f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$.

Miller Effect Theorem: Impact of Feedback Capacitance C_μ

- Miller Effect Origin: In an inverting amplifier ($A_v = -|A_v|$), feedback capacitance C_μ connected between base (input) and collector (output) experiences an amplified AC voltage swing across its terminals.
- Input Miller Capacitance Derivation: $C_{M,in} = C_\mu\,(1 - A_v) = C_\mu\,(1 + |A_v|)$.
- Output Miller Capacitance Derivation: $C_{M,out} = C_\mu\left(1 - \frac{1}{A_v}\right) \approx C_\mu$.
- Total High-Frequency Input Capacitance: $C_{in,total} = C_\pi + C_{M,in} = C_\pi + C_\mu(1 + |A_v|)$.
- Bandwidth Impact: The massive equivalent input capacitance $C_{in,total}$ creates a low-frequency dominant pole at the input node, severely reducing high-frequency cutoff f_H.

Feedback Effects on Gain-Bandwidth Product: Desensitivity & Extension

- Closed-Loop Gain with Negative Feedback: $A_f = \frac{A_{mid}}{1+\beta_{fb}A_{mid}}$, where β_{fb} is the feedback factor.
- Closed-Loop Upper Cutoff Frequency: $f_{Hf} = f_H\,(1 + \beta_{fb}A_{mid})$.
- Closed-Loop Lower Cutoff Frequency: $f_{Lf} = \frac{f_L}{1+\beta_{fb}A_{mid}}$.
- Closed-Loop Bandwidth Extension: $BW_f = f_{Hf} - f_{Lf} \approx f_H\,(1 + \beta_{fb}A_{mid})$.
- Conservation of Gain-Bandwidth Product:
  $GBP_f = A_f \times BW_f = \left(\frac{A_{mid}}{1+\beta_{fb}A_{mid}}\right) \times [f_H(1 + \beta_{fb}A_{mid})] = A_{mid} \times f_H = GBP.$

Numerical Example: High-Frequency Hybrid-\{}pi & f_T Calculation

- Given Transistor Parameters: Operating quiescent current $I_{CQ} = 2.6\,\text{mA}$, $\beta_0 = 100$, $V_T = 26\,\text{mV}$. Parasitic junction capacitances $C_\pi = 30\,\text{pF}$, $C_\mu = 2\,\text{pF}$. Inverting voltage gain $|A_v| = 50$. Source resistance $R_{sig} = 600\,\Omega$, $R_{TH} = 10\,\text{k}\Omega$.
- Step 1: Calculate Transconductance g_m: $g_m = \frac{I_{CQ}}{V_T} = \frac{2.6\,\text{mA}}{26\,\text{mV}} = 0.1\,\text{S} = 100\,\text{mS}$.
- Step 2: Calculate Input Resistance r_π: $r_\pi = \frac{\beta_0}{g_m} = \frac{100}{0.1} = 1000\,\Omega = 1.0\,\text{k}\Omega$.
- Step 3: Calculate Transition Frequency f_T: $f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)} = \frac{0.1}{2\pi(30\text{pF}+2\text{pF})} = \frac{0.1}{2\pi \times 32 \times 10^{-12}} = 497.35\,\text{MHz}$.
- Step 4: Calculate Miller Input Capacitance: $C_{M,in} = C_\mu(1 + |A_v|) = 2\,\text{pF} \times (1 + 50) = 102\,\text{pF}$.
- Step 5: Total Input Capacitance: $C_{in,total} = C_\pi + C_{M,in} = 30\,\text{pF} + 102\,\text{pF} = 132\,\text{pF}$.

Summary & Core Amplifier Frequency Response Principles

- Frequency Response Regions: Low-frequency roll-off ($f < f_L$) set by coupling/bypass capacitors; High-frequency roll-off ($f > f_H$) set by junction capacitors (C_π, C_μ).
- Half-Power Cutoff: $-3\,\text{dB}$ point where gain drops to $0.707A_{mid}$ and power drops to 50%.
- Miller Effect: Multiplies feedback capacitance by $(1 + |A_v|)$, creating the dominant high-frequency input pole.
- Gain-Bandwidth Invariance: $GBP = |A_{mid}| \times BW = f_T = \frac{g_m}{2\pi(C_\pi + C_\mu)}$.
- Feedback Extension: Negative feedback trades gain for bandwidth, extending $BW_f = f_H(1 + \beta_{fb}A)$ while conserving overall GBP.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Learning Roadmap

- Voltage, Current, and Power Gain Definitions and Decibel Conversions
- Amplifier Frequency Response: Half-Power (-3 dB) Cutoff Frequencies f_L and f_H
- Bandwidth (BW) and Transfer Function Representation of Single-Pole Amplifiers
- Gain-Bandwidth Product (GBW) and Unity-Gain Frequency (f_T)
- Gain-Bandwidth Trade-Off via Negative Feedback Configuration
- BJT High-Frequency Figures of Merit: Cutoff Frequencies f_α, f_β, and f_T
- Physical Factors Influencing GBW: Transconductance g_m and Parasitic Capacitances
- Op-Amp Closed-Loop Bandwidth Determination and Noise Gain Considerations
- Gain-Bandwidth Shrinkage in Multistage Cascaded Amplifiers
- Step-by-Step Numerical Examples and Comprehensive Summary

Amplifier Gain Metrics: Voltage, Current, and Power Gains in Decibels

- Voltage Gain Definition: Linear ratio $A_v = \frac{V_o}{V_i}$ and decibel representation $A_v(\text{dB}) = 20\log_{10}\left|\frac{V_o}{V_i}\right|$, quantifying signal voltage amplification.
- Current Gain Definition: Linear ratio $A_i = \frac{I_o}{I_i}$ and decibel representation $A_i(\text{dB}) = 20\log_{10}\left|\frac{I_o}{I_i}\right|$, measuring current multiplication across low-impedance nodes.
- Power Gain Relationship: Overall power amplification $A_p = \frac{P_o}{P_i} = A_v \cdot A_i$. In decibels, $A_p(\text{dB}) = 10\log_{10} A_p = A_v(\text{dB}) + A_i(\text{dB})$ when input and output load resistances are equal.
- Source-to-Load System Gain (A_{vs}): Incorporates signal source internal resistance R_S and load resistance R_L: $A_{vs} = \frac{V_o}{V_s} = \left(\frac{R_{in}}{R_S + R_{in}}\right) A_v \left(\frac{R_L}{R_{out} + R_L}\right)$.

Frequency Response Characteristics & Bandwidth (BW)

- Midband Voltage Gain (A_M): The maximum, frequency-independent voltage gain in the intermediate frequency range where coupling/bypass capacitors act as AC short circuits and parasitic capacitances act as open circuits.
- Half-Power (-3 dB) Cutoff Frequencies: Lower cutoff f_L and upper cutoff f_H represent frequencies where the magnitude drops to $|A(f)| = \frac{A_M}{\sqrt{2}} \approx 0.707 A_M$.
- Power Reduction at Cutoff: At f_L and f_H, output power drops to half of midband power ($P_{out} = 0.5 P_{mid}$), corresponding to a -3.01 dB change: $20 \log_{10}(0.707) = -3.01$ dB.
- Bandwidth Definition: $BW = f_H - f_L$. For broadband amplifiers where $f_H \gg f_L$ (e.g., $f_H = 1$ MHz and $f_L = 10$ Hz), the bandwidth is approximated as $BW \approx f_H$.

Single-Pole Transfer Function Analysis & High-Frequency Roll-off

- Single-Pole High-Frequency Transfer Function: $A(s) = \frac{A_M}{1+s/\omega_H}$, where $\omega_H = 2\pi f_H$ is the high-frequency pole.
- Frequency Response Vector Expression: Substituting $s = j\omega$ yields $A(j\omega) = \frac{A_M}{1+j(\omega/\omega_H)} = \frac{A_M}{\sqrt{1+(f/f_H)^2}} \angle -\arctan(f/f_H)$.
- Asymptotic High-Frequency Roll-Off: For frequencies well above cutoff ($f \gg f_H$), the gain magnitude simplifies to $|A(f)| \approx A_M \cdot \frac{f_H}{f}$, giving a roll-off rate of -20 dB/decade (or -6 dB/octave).
- Phase Response Shift: Phase lag at midband ($f \ll f_H$) is 0°, at upper cutoff ($f = f_H$) is -45°, and approaches -90° as $f \to \infty$.

Gain-Bandwidth Product (GBW) and Unity-Gain Frequency (f_T)

- Gain-Bandwidth Product Definition: $GBW = A_M \cdot f_H$, representing the constant product of midband voltage gain magnitude A_M and upper 3-dB bandwidth f_H for a single-pole system.
- Unity-Gain Frequency (f_T): The frequency at which the short-circuit/open-loop voltage gain drops to unity ($|A(f_T)| = 1 = 0$ dB).
- Equivalence of GBW and f_T: Setting $|A(f_T)| = \frac{A_M}{\sqrt{1+(f_T/f_H)^2}} = 1$ yields $f_T \approx A_M \cdot f_H = GBW$ when $A_M \gg 1$.
- Figure of Merit Significance: GBW remains constant across different closed-loop gain configurations, serving as an intrinsic device parameter determined by internal transistor dynamics.

Gain vs. Bandwidth Trade-off via Negative Feedback

- Closed-Loop Gain Derivation: Applying negative feedback with feedback factor β reduces low-frequency gain: $A_{cl}(s) = \frac{A(s)}{1+\beta A(s)}$.
- Closed-Loop Transfer Function Expansion: Substituting $A(s) = \frac{A_0}{1+s/\omega_H}$ yields $A_{cl}(s) = \frac{A_0/(1+A_0\beta)}{1+\frac{s}{\omega_H(1+A_0\beta)}}$.
- Closed-Loop Bandwidth Extension: The new midband gain is $A_{cl,0} = \frac{A_0}{1+A_0\beta}$ and new upper cutoff is $f_{H,cl} = f_H(1 + A_0\beta)$.
- Invariance of Gain-Bandwidth Product: Multiplying closed-loop gain by closed-loop bandwidth gives $GBW_{cl} = A_{cl,0} \cdot f_{H,cl} = \left(\frac{A_0}{1+A_0\beta}\right) \cdot f_H(1 + A_0\beta) = A_0 f_H = GBW$.

Numerical Example 1: BJT Amplifier Bandwidth and GBW Calculation

- Problem Statement: A single-stage BJT amplifier has an open-loop midband voltage gain $A_0 = 80$ dB ($10,000$ V/V) and a unity-gain frequency $f_T = 50$ MHz. (1) Calculate open-loop bandwidth f_H. (2) If negative feedback reduces closed-loop gain to $A_{cl} = 40$ dB (100 V/V), find new bandwidth $f_{H,cl}$.
- Step 1 - Open-Loop Bandwidth f_H: Using $GBW = A_0 \cdot f_H = f_T$, we get $f_H = \frac{f_T}{A_0} = \frac{50 \times 10^6 \text{ Hz}}{10,000} = 5,000 \text{ Hz} = 5 \text{ kHz}$.
- Step 2 - Closed-Loop Bandwidth $f_{H,cl}$: Using constant GBW, $f_{H,cl} = \frac{GBW}{A_{cl}} = \frac{50 \times 10^6 \text{ Hz}}{100} = 500,000 \text{ Hz} = 500 \text{ kHz}$.
- Verification of Feedback Factor β: $1 + A_0\beta = \frac{A_0}{A_{cl}} = \frac{10000}{100} = 100 \implies \beta = \frac{99}{10000} = 0.0099$. Bandwidth expanded 100-fold from 5 kHz to 500 kHz.

Transistor High-Frequency Limits: Cutoff Frequencies f_α, f_β, and f_T

- Common-Base Short-Circuit Cutoff (f_α): Frequency where common-base short-circuit current gain α drops by 3 dB from low-frequency value α_0: $f_\alpha = \frac{1}{2\pi\tau_F}$, where τ_F is base transit time.
- Common-Emitter Short-Circuit Cutoff (f_β): Frequency where common-emitter current gain $\beta(f)$ drops by 3 dB: $f_\beta = \frac{1}{2\pi r_\pi (C_\pi + C_\mu)} = \frac{g_m}{2\pi\beta_0(C_\pi + C_\mu)}$.
- Relationship Between f_T and f_β: Short-circuit current gain relation $\beta(f) = \frac{\beta_0}{1+j(f/f_\beta)}$. Unity gain frequency occurs when $|\beta(f_T)| = 1 \implies f_T = \beta_0 f_\beta = \frac{g_m}{2\pi(C_\pi + C_\mu)}$.
- Alpha-Beta Cutoff Relation: Since $\beta_0 \gg 1$, $f_\beta = \frac{f_T}{\beta_0}$ is substantially lower than f_T and $f_\alpha \approx 1.2 f_T$.

Physical Parameters Governing GBW: g_m, C_π, and C_μ

- Transconductance Dependence: $g_m = \frac{I_C}{V_T}$, where I_C is DC collector current and $V_T \approx 26$ mV at 300 K. Higher bias current I_C elevates g_m and increases f_T.
- Diffusion Capacitance C_{DE}: Proportional to collector current: $C_{DE} = g_m \tau_F = \left(\frac{I_C}{V_T}\right) \tau_F$. Dominates base-emitter junction capacitance $C_\pi = C_{jE} + C_{DE}$ at higher bias currents.
- Depletion Capacitances C_{jE}, C_μ: Voltage-dependent junction capacitances: $C_j(V_R) = \frac{C_{j0}}{(1+V_R/V_0)^m}$. Collector-base capacitance C_μ is minimized by higher reverse-bias collector-base voltage V_{CB}.
- Optimum Bias Current Region: At very high I_C, high-level injection and Kirk effect increase base transit time τ_F, causing f_T and GBW to roll off after reaching a peak value.

Numerical Example 2: Operational Amplifier Closed-Loop Bandwidth

- Problem Statement: An operational amplifier has a specified Gain-Bandwidth Product $GBW = 12$ MHz. It is configured as a non-inverting voltage amplifier with feedback resistors $R_F = 18$ kΩ and $R_1 = 2$ kΩ. Determine: (1) Closed-loop midband voltage gain A_{cl}. (2) Closed-loop 3-dB bandwidth $f_{H,cl}$. (3) Gain at an operating signal frequency of $f = 2.4$ MHz.
- Step 1 - Closed-Loop Gain A_{cl}: $A_{cl} = 1 + \frac{R_F}{R_1} = 1 + \frac{18\ \text{k}\Omega}{2\ \text{k}\Omega} = 1 + 9 = 10$ V/V (20 dB).
- Step 2 - Closed-Loop Bandwidth $f_{H,cl}$: $f_{H,cl} = \frac{GBW}{A_{cl}} = \frac{12 \times 10^6\ \text{Hz}}{10} = 1.2$ MHz.
- Step 3 - Gain Magnitude at $f = 2.4$ MHz: $|A(f)| = \frac{A_{cl}}{\sqrt{1+(f/f_{H,cl})^2}} = \frac{10}{\sqrt{1+(2.4/1.2)^2}} = \frac{10}{\sqrt{1+4}} = \frac{10}{\sqrt{5}} \approx 4.47$ V/V (13.01 dB).

Gain-Bandwidth Considerations in Multistage Amplifiers

- Multistage Bandwidth Shrinkage Effect: Cascading N identical non-interacting single-pole stages increases overall low-frequency gain to $A_{M,sys} = (A_M)^N$, but shrinks upper 3-dB bandwidth.
- Upper Cutoff Formula for N Cascaded Stages: $f_{H,sys} = f_H \cdot \sqrt{2^{1/N} - 1}$, where f_H is the upper cutoff of an individual stage.
- Bandwidth Reduction Factors: For $N = 2$, $f_{H,sys} = 0.643 f_H$. For $N = 3$, $f_{H,sys} = 0.510 f_H$. For $N = 4$, $f_{H,sys} = 0.435 f_H$.
- Overall GBW Non-Constancy: Because overall gain grows exponentially $(A_M)^N$ while bandwidth shrinks moderately, the total multi-stage GBW is not equal to single-stage GBW, requiring careful stage-by-stage optimization.

Summary & Key Engineering Formulas for Amplifier Parameters

- Gain Relationships: Voltage Gain $A_v(\text{dB}) = 20\log_{10}|A_v|$, Power Gain $A_p(\text{dB}) = 10\log_{10}A_p = A_v(\text{dB}) + A_i(\text{dB})$.
- Bandwidth & Cutoff Limits: Half-power (-3 dB) frequencies f_L, f_H; Bandwidth $BW = f_H - f_L \approx f_H$ for broadband systems.
- Gain-Bandwidth Invariance: $GBW = A_M \cdot f_H = f_T$. Negative feedback scales gain down by $(1 + A_0\beta)$ and expands upper bandwidth by $(1 + A_0\beta)$, keeping GBW constant.
- Transistor Frequency Parameters: Unity-gain frequency $f_T = \beta_0 f_\beta = \frac{g_m}{2\pi(C_\pi + C_\mu)}$, driven by bias current I_C and internal capacitances.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Learning Roadmap

- Low-Frequency Limitations and High-Pass RC Filter Action in Amplifiers
- Input Coupling Capacitor (C_{C1}) Network & Cutoff Frequency (f_{L1}) Derivation
- Output Coupling Capacitor (C_{C2}) Network & Cutoff Frequency (f_{L2}) Derivation
- Emitter Bypass Capacitor (C_E) AC Impedance & Cutoff Frequency (f_{LE}) Derivation
- Pole-Zero Analysis of the Emitter Bypass Impedance Network $Z_E(s)$
- Dominant Pole Approximation & Low-Frequency Asymptotic Bode Plotting
- Detailed Step-by-Step Numerical Calculation of f_{L1}, f_{L2}, f_{LE}, and Overall f_L
- Low-Frequency Phase Lead Response and Pulse Distortion (Sag/Tilt)
- Engineering Design Guidelines for Low-Frequency Capacitor Selection
- Design Calculation Example for Target Lower Cutoff Frequency $f_L = 50$ Hz
- Comprehensive Summary and Design Rules

Low-Frequency Signal Attenuation Mechanisms in BJT Amplifiers

- Capacitive Reactance Frequency Dependency: AC reactance $X_C(f) = \frac{1}{2\pi fC}$ approaches infinity as frequency $f \to 0$ Hz, acting as a open circuit to DC and attenuating low-frequency AC signals.
- High-Pass Filter Topology: Coupling capacitors C_{C1} and C_{C2} are in series with the signal path, forming high-pass RC filter sections with circuit resistances.
- Bypass Capacitor Degeneration: Emitter bypass capacitor C_E is in parallel with emitter resistor R_E. At low frequencies where X_{CE} is large, negative feedback across R_E reduces AC voltage gain.
- Midband Transition: As frequency increases above f_L, $X_C \to 0$, capacitors act as AC short circuits, and amplifier gain stabilizes at midband value A_M.

Input Coupling Capacitor (C_{C1}) Network & Cutoff Frequency (f_{L1})

- Equivalent Input Resistance ($R_{in,C1}$): Seen looking into the nodes connected to C_{C1}: $R_{in,C1} = R_S + R_{in,stage} = R_S + (R_1 \parallel R_2 \parallel R_{in,base})$, where $R_{in,base} = r_\pi + (1+\beta_0)R_E$ if unbypassed at DC.
- Transfer Function Contribution: $T_1(s) = \frac{V_b(s)}{V_s(s)} = \left(\frac{R_{in,stage}}{R_S+R_{in,stage}}\right)\frac{s}{s+\omega_{L1}}$, where $\omega_{L1} = \frac{1}{C_{C1}R_{in,C1}}$.
- Lower Cutoff Pole Frequency (f_{L1}): $f_{L1} = \frac{1}{2\pi C_{C1}R_{in,C1}} = \frac{1}{2\pi C_{C1}[R_S+(R_1\|R_2\|R_{in,base})]}$.
- Low-Frequency Roll-Off & Phase Shift: Below f_{L1}, voltage transfer drops at $+20$ dB/decade with frequency decrease, and introduces a phase lead of $+45^\circ$ at $f = f_{L1}$.

Output Coupling Capacitor (C_{C2}) Network & Cutoff Frequency (f_{L2})

- Equivalent Output Resistance ($R_{out,C2}$): Seen looking from the terminals of C_{C2}: $R_{out,C2} = R_{out,stage} + R_L = R_C + R_L$ (assuming transistor output resistance $r_o \gg R_C$).
- Output Transfer Function Expression: $T_2(s) = \frac{V_o(s)}{V_c(s)} = \left(\frac{R_L}{R_C+R_L}\right) \frac{s}{s+\omega_{L2}}$, where $\omega_{L2} = \frac{1}{C_{C2}(R_C+R_L)}$.
- Output Cutoff Pole Frequency (f_{L2}): $f_{L2} = \frac{1}{2\pi C_{C2}(R_C+R_L)}$.
- Loading Effect Impact: Larger load resistance R_L increases $R_{out,C2}$, which lowers the required capacitance C_{C2} for a given low-frequency cutoff target f_{L2}.

Emitter Bypass Capacitor (C_E) AC Impedance & Cutoff Frequency (f_{LE})

- Equivalent Resistance Seen by C_E ($R_{eq,E}$): Seen looking into the emitter terminal: $R_{eq,E} = R_E \parallel R_{emitter,in} = R_E \parallel \left[r_e + \frac{R_S \parallel R_1 \parallel R_2}{\beta_0 + 1}\right]$, where small-signal emitter resistance $r_e = \frac{V_T}{I_C} = \frac{r_\pi}{\beta_0 + 1}$.
- Emitter Pole Frequency Formula (f_{LE}): $f_{LE} = \frac{1}{2\pi C_E R_{eq,E}} = \frac{1}{2\pi C_E \left(R_E \parallel \left[r_e + \frac{R_S \parallel R_1 \parallel R_2}{\beta_0 + 1}\right]\right)}$.
- Small Equivalent Resistance Implication: Because r_e is small (typically $10 - 30\ \Omega$), $R_{eq,E}$ is very small ($15 - 50\ \Omega$). Thus, f_{LE} is much higher than f_{L1} and f_{L2} for equal capacitor values.
- Dominant Pole Role: To keep f_{LE} down near audio frequencies, C_E must be significantly larger ($47 - 220\ \mu$F) than C_{C1} or C_{C2} ($1 - 10\ \mu$F).

Pole-Zero Derivation of the Emitter Bypass Impedance Network $Z_E(s)$

- Impedance Expression for $R_E \parallel C_E$: $Z_E(s) = R_E \parallel \frac{1}{sC_E} = \frac{R_E}{1+sR_E C_E}$.
- Unbypassed Gain Equation: Incorporating $Z_E(s)$ into CE amplifier voltage gain: $A_v(s) = -\frac{\beta_0(R_C \| R_L)}{r_\pi + (\beta_0+1)Z_E(s)} = -g_m(R_C \parallel R_L)\frac{1+sR_E C_E}{1+sR_E C_E + g_m R_E}$.
- Zero Frequency Location (ω_z): The numerator zero occurs at $\omega_z = \frac{1}{R_E C_E} \implies f_z = \frac{1}{2\pi R_E C_E}$.
- Pole Frequency Location (ω_p): The denominator pole occurs at $\omega_p = \frac{1+g_m R_E}{R_E C_E} = \frac{1}{C_E R_{eq,E}} \implies f_{LE} = \frac{1}{2\pi C_E R_{eq,E}}$.
- Gain Transition: At frequencies below f_z, gain drops to unbypassed value $A_{v,unbypassed} = -\frac{R_C \| R_L}{R_E}$. Above f_{LE}, gain rises to full midband bypassed gain $A_M = -g_m(R_C \parallel R_L)$.

Dominant Pole Approximation & Low-Frequency Asymptotic Response

- Overall Low-Frequency Transfer Function: $A_L(s) = A_M \cdot \left(\frac{s}{s+\omega_{L1}}\right)\left(\frac{s}{s+\omega_{L2}}\right)\left(\frac{s+\omega_z}{s+\omega_{LE}}\right)$.
- Dominant Pole Condition: If one pole frequency is significantly higher than all other low-frequency poles (e.g., $f_{LE} \geq 4f_{L1}$ and $f_{LE} \geq 4f_{L2}$), f_{LE} dominates the lower 3-dB cutoff: $f_L \approx f_{LE}$.
- Non-Dominant Pole Combination Formula: When poles are closely spaced, overall lower cutoff f_L is estimated using short-circuit sum or root-square approximation: $f_L \approx \sqrt{f_{L1}^2 + f_{L2}^2 + f_{LE}^2}$ or $f_L \approx f_{L1} + f_{L2} + f_{LE}$.
- Asymptotic Bode Slope Progression: Gain magnitude slope increases from $+20$ dB/decade below f_{LE}, to $+40$ dB/decade below f_{L1}, to $+60$ dB/decade below f_{L2}.

Numerical Example 1: Determining f_{L1}, f_{L2}, f_{LE} and Overall f_L

- Circuit Parameters: $V_{CC} = 12$ V, $R_1 = 40$ kΩ, $R_2 = 10$ kΩ, $R_C = 4$ kΩ, $R_E = 2$ kΩ, $R_S = 600$ Ω, $R_L = 10$ kΩ, $\beta_0 = 100$, $I_C = 1$ mA. Capacitors: $C_{C1} = 10$ μF, $C_{C2} = 4.7$ μF, $C_E = 47$ μF. Small-signal parameters: $V_T = 26$ mV $\implies r_e = 26\ \Omega, g_m = 38.46$ mS, $r_\pi = 2.6$ kΩ.
- Step 1 - Calculate f_{L1}: $R_B = 40\text{ k} \parallel 10\text{ k} = 8$ kΩ. $R_{in,stage} = R_B \parallel r_\pi = 8\text{ k} \parallel 2.6\text{ k} = 1.962$ kΩ. $R_{in,C1} = 600 + 1962 = 2.562$ kΩ. $f_{L1} = \frac{1}{2\pi \times 10\mu\text{F} \times 2562} = 6.21$ Hz.
- Step 2 - Calculate f_{L2}: $R_{out,C2} = R_C + R_L = 4\text{ k} + 10\text{ k} = 14$ kΩ. $f_{L2} = \frac{1}{2\pi \times 4.7\mu\text{F} \times 14000} = 2.42$ Hz.
- Step 3 - Calculate f_{LE}: $R_{base,eq} = R_S \parallel R_1 \parallel R_2 = 600 \parallel 8000 = 558\ \Omega$. $R_{emitter,in} = r_e + \frac{558}{101} = 26 + 5.52 = 31.52\ \Omega$. $R_{eq,E} = 2000 \parallel 31.52 = 31.03\ \Omega$. $f_{LE} = \frac{1}{2\pi \times 47\mu\text{F} \times 31.03} = 109.13$ Hz.
- Step 4 - Overall f_L: Dominant pole $f_{LE} = 109.13$ Hz. Root-square estimate $f_L = \sqrt{6.21^2 + 2.42^2 + 109.13^2} = 109.33$ Hz.

Low-Frequency Phase Lead & Signal Distortion

- Total Low-Frequency Phase Lead Equation:
  $\theta(f) = +\arctan\left(\frac{f_{L1}}{f}\right) + \arctan\left(\frac{f_{L2}}{f}\right) + \arctan\left(\frac{f_{LE}}{f}\right) - \arctan\left(\frac{f_z}{f}\right)$.
- Midband vs Low-Frequency Phase: At midband ($f \gg f_L$), $\theta(f) \approx 0^\circ$ relative to the 180° inversion of Common-Emitter configuration.
- Pulse Response Distortion (Square Wave Sag/Tilt): Passing a pulse of width T_W through high-pass cutoff f_L causes exponential rooftop decay.
- Percentage Sag Formula: Fractional voltage droop $S = \frac{\Delta V}{V_{peak}} \approx \pi \frac{f_L}{f_{pulse}} \times 100\%$. Keeping sag under 5% requires $f_L \leq 0.016 f_{pulse}$.

Capacitor Selection Strategies for Target Lower Cutoff Frequency

- Design Budgeting Strategy: When designing for a target lower 3-dB cutoff f_L, allocate contributions across capacitors to minimize physical component sizes and costs.
- Optimal Pole Budget Rule of Thumb: Set the emitter bypass pole $f_{LE} = 0.8f_L$, and input/output coupling poles $f_{L1} = 0.1f_L$, $f_{L2} = 0.1f_L$.
- Minimizing Bypass Capacitor Size: Since $C_E = \frac{1}{2\pi f_{LE} R_{eq,E}}$, allocating 80% of f_L to f_{LE} maximizes f_{LE}, reducing required physical capacitance C_E.
- Practical Considerations: Electrolytic capacitors used for C_E have wide tolerances ($\pm 20\%$) and Equivalent Series Resistance (ESR) that must be factored into high-precision designs.

Numerical Example 2: Designing Capacitors for a Specified $f_L = 50$ Hz

- Design Requirement: Size capacitors C_{C1}, C_{C2}, C_E for a CE stage with $R_{in,C1} = 3$ kΩ, $R_{out,C2} = 12$ kΩ, $R_{eq,E} = 25$ Ω to achieve a lower 3-dB cutoff $f_L = 50$ Hz.
- Step 1 - Allocate Pole Budgets: Target $f_{LE} = 0.8 \times 50$ Hz $= 40$ Hz, $f_{L1} = 0.1 \times 50$ Hz $= 5$ Hz, $f_{L2} = 0.1 \times 50$ Hz $= 5$ Hz.
- Step 2 - Calculate Input Coupling Capacitor C_{C1}: $C_{C1} = \frac{1}{2\pi \times 5 \text{ Hz} \times 3000 \ \Omega} = 10.61 \ \mu\text{F} \implies$ Select standard 15 μF.
- Step 3 - Calculate Output Coupling Capacitor C_{C2}: $C_{C2} = \frac{1}{2\pi \times 5 \text{ Hz} \times 12000 \ \Omega} = 2.65 \ \mu\text{F} \implies$ Select standard 3.3 μF.
- Step 4 - Calculate Emitter Bypass Capacitor C_E: $C_E = \frac{1}{2\pi \times 40 \text{ Hz} \times 25 \ \Omega} = 159.15 \ \mu\text{F} \implies$ Select standard 220 μF.

Summary of Bypass and Coupling Capacitor Effects on Frequency Response

- Coupling Capacitors (C_{C1}, C_{C2}): Determine high-pass cutoffs $f_{L1} = \frac{1}{2\pi C_{C1} R_{in,C1}}$ and $f_{L2} = \frac{1}{2\pi C_{C2} R_{out,C2}}$.
- Bypass Capacitor (C_E): Determines cutoff $f_{LE} = \frac{1}{2\pi C_E R_{eq,E}}$. Requires largest capacitance because $R_{eq,E} = R_E \parallel \left[r_e + \frac{R_{base}}{\beta_0 + 1} \right]$ is very small.
- Pole-Zero Behavior: Bypass network creates a zero $f_z = \frac{1}{2\pi R_E C_E}$ and pole f_{LE}. Gain transitions from unbypassed value below f_z to bypassed midband value above f_{LE}.
- Dominant Pole Approximation: Lower 3-dB cutoff $f_L \approx \sqrt{f_{L1}^2 + f_{L2}^2 + f_{LE}^2} \approx f_{LE}$ when f_{LE} is dominant.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Learning Roadmap

- Overview of the Three Frequency Response Regions (Low, Midband, High)
- Midband Voltage Gain Derivation using Small-Signal Hybrid-π Model
- BJT High-Frequency Hybrid-π Model & Junction Capacitances (C_π, C_μ)
- Miller's Theorem Derivation and Equivalent Input/Output Capacitances
- High-Frequency Input and Output Cutoff Frequencies ($f_{H,in}$, $f_{H,out}$)
- Construction of Complete Bode Magnitude and Phase Response Curves
- Comprehensive Numerical Example: Full Frequency Response Calculation
- High-Frequency Performance Comparison Across Configurations (CE, CB, CC)
- MOSFET Common-Source (CS) High-Frequency Analysis
- Design Problem: Bandwidth Extension Techniques for CE Amplifiers
- Comprehensive Summary and Key Takeaways

Overview of the Complete Frequency Response Curve

- Low-Frequency Region ($f < f_L$): Gain attenuates at $+20$ dB/decade per pole due to increasing reactance of coupling (C_{C1}, C_{C2}) and bypass (C_E) capacitors.
- Midband Frequency Region ($f_L \leq f \leq f_H$): Voltage gain magnitude is constant at maximum value A_M. External capacitors act as ideal AC short circuits, while internal parasitic capacitances act as open circuits.
- High-Frequency Region ($f > f_H$): Gain rolls off at -20 dB/decade per pole due to decreasing reactance of internal junction capacitances C_π (base-emitter) and C_μ (base-collector).
- Bandwidth & Half-Power Points: Operating bandwidth $BW = f_H - f_L$. Gain magnitude at f_L and f_H is $|A(f)| = \frac{A_M}{\sqrt{2}} = A_M - 3.01$ dB.

Midband Small-Signal Voltage Gain Derivation

- Midband Hybrid-π Circuit: External capacitors are replaced by AC short circuits. Transistor replaced by small-signal parameters r_π and $g_m v_b e$.
- Input Voltage Divider: Base-emitter signal voltage $V_{be} = V_s \left(\frac{R_{in}}{R_S + R_{in}} \right)$, where $R_{in} = R_1 \parallel R_2 \parallel r_\pi$.
- Output Voltage Expression: Output voltage $V_o = -g_m V_{be}(R_C \parallel R_L)$ (negative sign indicates 180° phase inversion).
- Overall Midband System Gain ($A_{v,mid}$): $A_{v,mid} = \frac{V_o}{V_s} = -\left(\frac{R_1 \| R_2 \| r_\pi}{R_S + R_1 \| R_2 \| r_\pi} \right) g_m (R_C \parallel R_L)$, where $g_m = \frac{I_C}{V_T}$ and $r_\pi = \frac{\beta_0}{g_m}$.

High-Frequency BJT Hybrid-π Model & Parasitic Capacitances

- Base-Emitter Junction Capacitance (C_π): Sum of forward-bias depletion capacitance C_{jE} and diffusion capacitance $C_{DE} = g_m \tau_F$: $C_\pi = C_{jE} + g_m \tau_F$ (typically $20 - 100$ pF).
- Base-Collector Junction Capacitance (C_μ): Reverse-bias depletion capacitance $C_{jC} = \frac{C_{j0}}{(1+V_{CB}/V_0)^m}$ (typically $1 - 5$ pF). Crosses the base and collector terminals.
- Collector-Substrate Capacitance (C_{cs}): Parasitic capacitance to substrate in integrated circuits (typically $1 - 3$ pF).
- Wiring & Layout Parasitics: Wiring capacitances $C_{w,in}$ and $C_{w,out}$ added in parallel with input and output nodes.

Miller's Theorem & High-Frequency Input/Output Capacitance Derivation

- Miller's Theorem Concept: An impedance Z connected between input node (1) and output node (2) with voltage gain $K = \frac{V_2}{V_1}$ can be replaced by two equivalent shunting impedances: $Z_1 = \frac{Z}{1-K}$ and $Z_2 = \frac{Z}{1-1/K}$.
- Miller Input Capacitance ($C_{M,in}$): For bridging feedback capacitance C_μ with stage inverting gain $K = A_{v,stage} = -g_m(R_C \parallel R_L)$: $C_{M,in} = C_\mu(1 - A_{v,stage}) = C_\mu(1 + |A_{v,stage}|)$.
- Miller Output Capacitance ($C_{M,out}$): $C_{M,out} = C_\mu \left(1 - \frac{1}{A_{v,stage}}\right) \approx C_\mu$ since $|A_{v,stage}| \gg 1$.
- Total High-Frequency Input Capacitance (C'_{in}):
  $C'_{in} = C_\pi + C_{M,in} + C_{w,in} = C_\pi + C_\mu(1 + |A_{v,stage}|) + C_{w,in}$.
- Impact of Miller Multiplication: Even a small $C_\mu = 4$ pF with gain $A_{v,stage} = -100$ creates $C_{M,in} = 4$ pF $\times$ 101 $= 404$ pF, completely dominating input capacitance!

High-Frequency Cutoff Calculation ($f_{H,in}$, $f_{H,out}$ and Overall f_H)

- Input High-Frequency Pole ($f_{H,in}$): Equivalent resistance $R'_{in} = R_S \parallel R_1 \parallel R_2 \parallel r_\pi$. Input cutoff: $f_{H,in} = \frac{1}{2\pi R'_{in} C'_{in}} = \frac{1}{2\pi (R_S \| R_1 \| R_2 \| r_\pi)[C_\pi + C_\mu(1+|A_{v,stage}|)+C_{w,in}]}$.
- Output High-Frequency Pole ($f_{H,out}$): Equivalent resistance $R'_{out} = R_C \parallel R_L \parallel r_o \approx R_C \parallel R_L$. Output cutoff: $f_{H,out} = \frac{1}{2\pi R'_{out} C'_{out}} = \frac{1}{2\pi (R_C \| R_L)[C_\mu + C_{cs} + C_{w,out}]}$.
- Dominant High-Frequency Pole: Because $C'_{in} \gg C'_{out}$ due to Miller multiplication, $f_{H,in}$ is substantially smaller than $f_{H,out}$, making $f_{H,in}$ the dominant upper pole.
- Overall Upper 3-dB Cutoff Frequency (f_H): $f_H \approx f_{H,in}$ or using root-square combination: $f_H = \frac{1}{\sqrt{(1/f_{H,in})^2 + (1/f_{H,out})^2}}$.

Bode Magnitude and Phase Plots of Single-Stage Amplifier

- Complete Transfer Function: $A(s) = A_{v,mid} \cdot \left(\frac{s}{s+\omega_L}\right) \cdot \left(\frac{1}{1+s/\omega_H}\right)$.
- Bode Magnitude Asymptotes: Flat response at $A_{v,mid}$(dB) in midband ($f_L < f < f_H$). $+20$ dB/decade roll-off for $f < f_L$, -20 dB/decade roll-off for $f > f_H$.
- Corner Frequencies: At $f = f_L$ and $f = f_H$, actual gain magnitude is -3 dB below asymptotic lines.
- Bode Phase Plot Progression: At $f \ll f_L$, phase is $+270^\circ$ ($+90^\circ$ lead over midband 180°). At $f = f_L$, phase is $+225^\circ$. At midband, phase is 180°. At $f = f_H$, phase is 135° (45° lag). At $f \gg f_H$, phase approaches $+90^\circ$ (90° lag).

Comprehensive Numerical Example: Complete Frequency Response of CE Amplifier

- Given Circuit & Transistor Parameters: $V_{CC} = 15$ V, $R_1 = 33$ kΩ, $R_2 = 10$ kΩ, $R_C = 3.3$ kΩ, $R_E = 1$ kΩ, $R_S = 500$ Ω, $R_L = 10$ kΩ, $\beta_0 = 150$, $I_C = 1.5$ mA. Parasitics: $C_\pi = 30$ pF, $C_\mu = 4$ pF, $C_{w,in} = 5$ pF, $C_{w,out} = 3$ pF. External: $C_{C1} = 10$ μF, $C_{C2} = 10$ μF, $C_E = 100$ μF. Small-signal parameters: $V_T = 26$ mV $\implies$ $r_e = 17.33$ Ω, $g_m = 57.69$ mS, $r_\pi = 2.6$ kΩ.
- Step 1 - Midband Gain ($A_{v,mid}$): $R_{in} = 33$ k $\parallel$ 10 k $\parallel$ 2.6 k $= 1.954$ kΩ. Loaded collector resistance $R'_L = R_C \parallel R_L = 3.3$ k $\parallel$ 10 k $= 2.481$ kΩ. Internal stage gain $A_{v,stage} = -g_m R'_L = -57.69$ mS $\times$ 2481 $= -143.13$ V/V. Overall gain $A_{v,mid} = -\left(\frac{1954}{500+1954}\right) \times 143.13 = -113.97$ V/V (41.14 dB).
- Step 2 - Miller Input Capacitance ($C_{M,in}$): $C_{M,in} = C_\mu(1 + |A_{v,stage}|) = 4$ pF $\times (1 + 143.13) = 576.52$ pF. Total input capacitance $C'_{in} = C_\pi + C_{M,in} + C_{w,in} = 30 + 576.52 + 5 = 611.52$ pF.
- Step 3 - High-Frequency Input Pole ($f_{H,in}$): Equivalent resistance $R'_{in} = R_S \parallel R_{in} = 500 \parallel 1954 = 398.1$ Ω. $f_{H,in} = \frac{1}{2\pi \times 398.1\ \Omega \times 611.52\ \text{pF}} = 653.8$ kHz.
- Step 4 - High-Frequency Output Pole ($f_{H,out}$): $C'_{out} = C_\mu + C_{w,out} = 4 + 3 = 7$ pF. $R'_{out} = 2.481$ kΩ. $f_{H,out} = \frac{1}{2\pi \times 2481 \times 7\ \text{pF}} = 9.16$ MHz. Upper cutoff $f_H \approx f_{H,in} = 653.8$ kHz.

High-Frequency Response Comparison: CE, CB, and CC Configurations

- Common-Emitter (CE): Provides high voltage and current gain, but suffers from strong Miller effect $C_{M,in} = C_\mu(1 + |A_v|)$, resulting in moderate upper cutoff frequency f_H.
- Common-Base (CB): Low input impedance ($R_{in} \approx r_e$), unit current gain, but ZERO Miller effect because collector is AC grounded relative to input. Achieves extremely high upper cutoff $f_H \approx f_T$, making it ideal for RF amplifiers.
- Common-Collector (CC / Emitter Follower): Voltage gain $A_v \approx 1 \implies C_{M,in} = C_\mu(1 - 1) = 0$. Low Miller multiplication, high input impedance, wide bandwidth, ideal as high-speed output buffers.
- Summary Comparison: CB configuration provides the widest bandwidth for voltage amplification due to elimination of Miller effect.

MOSFET Common-Source (CS) High-Frequency Response

- MOSFET High-Frequency Parasitics: Gate-source capacitance C_{gs}, gate-drain capacitance C_{gd}, and drain-source capacitance C_{ds}.
- Midband Gain: $A_{v,mid} = -g_m(R_D \parallel R_L)$, where $g_m = 2\sqrt{K_n I_D} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D}$.
- Miller Gate-Drain Capacitance: Gate-drain capacitance C_{gd} bridges input and output: $C_{M,in} = C_{gd}(1 + g_m(R_D \parallel R_L))$.
- CS High-Frequency Pole ($f_{H,in}$): $f_{H,in} = \frac{1}{2\pi(R_S \| R_G)[C_{gs} + C_{gd}(1 + g_m(R_D \| R_L))]}$. Very high input resistance R_G makes CS amplifiers sensitive to signal source resistance R_S.

Design Problem: Bandwidth Extension of a CE Stage

- Problem Challenge: An engineer needs to extend the upper 3-dB bandwidth f_H of a Common-Emitter stage from 500 kHz to 2 MHz. Evaluate design options.
- Option 1 - Emitter Degeneration (R_e): Adding an unbypassed emitter resistor R_e reduces stage gain to $A'_{v,stage} \approx -\frac{R_C \| R_L}{r_e + R_e}$. Lower gain reduces $C_{M,in} = C_\mu(1 + |A'_{v,stage}|)$, extending upper cutoff f_H proportionally.
- Option 2 - Source Impedance Reduction (R_S): Lowering signal source resistance R_S using an upstream Emitter Follower buffer reduces $R'_{in} = R_S \parallel R_{in}$, boosting $f_{H,in} = \frac{1}{2\pi R'_{in} C'_{in}}$.
- Option 3 - Device Selection: Replacing BJT with a high-f_T microwave transistor having smaller C_μ (0.5 pF vs 4 pF).
- Quantitative Trade-off: Adding R_e to trade gain for bandwidth preserves the constant Gain-Bandwidth Product (GBW).

Summary of Single-Stage Amplifier Frequency Characteristics

- Complete Transfer Function: $A(s) = A_{v,mid}\left(\frac{s}{s+\omega_L}\right)\left(\frac{1}{1+s/\omega_H}\right)$.
- Midband Gain: $A_{v,mid} = -\left(\frac{R_{in}}{R_S+R_{in}}\right) g_m(R_C \parallel R_L)$.
- Low-Frequency Dominant Pole: Set by external capacitors C_{C1}, C_{C2}, C_E, dominated by C_E due to small $R_{eq,E}$.
- High-Frequency Dominant Pole: Set by internal parasitics C_π, C_μ, dominated by Miller input capacitance $C_{M,in} = C_\mu(1 + |A_{v,stage}|)$.
- Configuration Comparison: Common-Base provides superior high-frequency performance by eliminating Miller effect.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Learning Roadmap

- Necessity and Structural Architecture of Multi-Stage Cascaded Amplifiers
- Total Voltage Gain Derivation in Linear and Decibel Scales
- Inter-Stage Loading Effects on Individual Stage Gain Calculations
- Complete Source-to-Load System Gain (A_{vs}) Derivation
- Detailed Step-by-Step Numerical Example: Two-Stage CE-CE Amplifier
- Cascode Configuration (CE-CB Pair): High Gain & Miller Effect Elimination
- Darlington Pair Configuration for Ultra-High Current Gain ($A_i \approx \beta^2$)
- Effect of Cascading on System Bandwidth (Bandwidth Shrinkage Phenomenon)
- Detailed Step-by-Step Numerical Example: 3-Stage Bandwidth Reduction
- Noise Figure Cascading & Friis Formula for Multi-Stage Signal Chains
- Comprehensive Summary and Key Design Formulas

Necessity and Architecture of Multi-Stage Cascaded Amplifiers

- Limitations of Single-Stage Amplifiers: Single stages cannot provide simultaneously high voltage gain (> 60 dB), high input impedance (> 1 MΩ), and low output impedance (< 50 Ω).
- Cascade Principle: Output signal of Stage 1 (V_{o1}) is fed as input to Stage 2 (V_{i2}), whose output (V_{o2}) drives Stage 3 (V_{i3}), up to Stage N.
- Functional Stage Specialization: (1) Input Stage: High input impedance, low noise. (2) Intermediate Stages: High voltage amplification. (3) Output Stage: Low output impedance, high power drive.
- Overall System Gains: Overall Voltage Gain $A_v = \frac{V_{oN}}{V_{i1}}$, Current Gain $A_i = \frac{I_{oN}}{I_{i1}}$, Power Gain $A_p = A_v A_i$.

Total Voltage Gain Calculation in Linear and Decibel Scales

- Linear Multiplication Rule: For N cascaded stages, overall voltage gain is the product of individual LOADED stage voltage gains: $A_v = \frac{V_{o1}}{V_{i1}} \cdot \frac{V_{o2}}{V_{i2}} \cdot \cdots \cdot \frac{V_{oN}}{V_{iN}} = \prod_{k=1}^{N} A_{vk}$.
- Decibel Addition Rule: Converting to decibels simplifies gain calculations into simple additions: $A_{v(\text{dB})} = 20 \log_{10} \left| \prod_{k=1}^{N} A_{vk} \right| = \sum_{k=1}^{N} 20 \log_{10} |A_{vk}| = \sum_{k=1}^{N} A_{vk(\text{dB})}$.
- Current Gain Product: Total system current gain $A_i = A_{i1} \cdot A_{i2} \ldots A_{iN} = \prod_{k=1}^{N} A_{ik}$.
- Power Gain Product: Total power gain $A_p = A_{p1} \cdot A_{p2} \ldots A_{pN}$. In decibels, $A_{p(\text{dB})} = A_{p1(\text{dB})} + A_{p2(\text{dB})} + \cdots + A_{pN(\text{dB})}$.

Inter-Stage Loading Effects on Individual Stage Gain Calculations

- Inter-Stage Loading Phenomenon: The input impedance $R_{in(k+1)}$ of stage $k+1$ appears in parallel with collector/drain resistor R_{Ck} of stage k.
- Loaded Gain Formula for Stage k: $A_{vk,\text{loaded}} = -g_{mk}\left(R_{Ck} \parallel R_{in(k+1)}\right)$.
- Input Impedance of BJT Stage $k+1$: $R_{in(k+1)} = R_{1(k+1)} \parallel R_{2(k+1)} \parallel r_{\pi(k+1)}$ for a fully bypassed Common-Emitter stage.
- Open-Circuit vs Loaded Gain Warning: Calculating stage k gain as $A_{vk} = -g_{mk}R_{Ck}$ ignoring $R_{in(k+1)}$ leads to severe overestimation of overall system gain!

Complete Source-to-Load System Gain (A_{vs}) Derivation

- System Signal Chain Model: Source V_s with resistance $R_S \rightarrow$ Input Stage 1 $\rightarrow$ Intermediate Stages $\rightarrow$ Output Stage $N \rightarrow$ Load R_L.
- Input Attenuation Factor: $V_{i1} = V_s \left(\frac{R_{in1}}{R_S + R_{in1}} \right)$, where $R_{in1} = R_{11} \parallel R_{21} \parallel r_{\pi 1}$.
- Output Divider Factor: $V_o = V_{oN} \left(\frac{R_L}{R_{outN} + R_L} \right)$, where $R_{outN} \approx R_{CN}$.
- Complete System Voltage Gain Equation:
  $A_{vs} = \frac{V_o}{V_s} = \left(\frac{R_{in1}}{R_S + R_{in1}} \right) \cdot A_{v1,\text{loaded}} \cdot A_{v2,\text{loaded}} \ldots A_{vN,\text{loaded}} \cdot \left(\frac{R_L}{R_{outN} + R_L} \right)$.

Numerical Example 1: Two-Stage RC-Coupled CE-CE Voltage Gain Analysis

- Given Circuit Parameters: $V_{CC} = 12$ V, $R_S = 600\ \Omega$, $R_L = 10$ kΩ. Stage 1: $R_{11} = 40$ kΩ, $R_{21} = 10$ kΩ, $R_{C1} = 4.7$ kΩ, $I_{C1} = 1$ mA, $\beta_1 = 100$. Stage 2: $R_{12} = 33$ kΩ, $R_{22} = 10$ kΩ, $R_{C2} = 2.2$ kΩ, $I_{C2} = 2$ mA, $\beta_2 = 150$. Small-signal params: $g_{m1} = 38.46$ mS, $r_{\pi 1} = 2.6$ kΩ; $g_{m2} = 76.92$ mS, $r_{\pi 2} = 1.95$ kΩ.
- Step 1 - Stage 2 Input Impedance (R_{in2}): $R_{in2} = R_{12} \parallel R_{22} \parallel r_{\pi 2} = 33\ \text{k} \parallel 10\ \text{k} \parallel 1.95\ \text{k} = 1.554$ kΩ.
- Step 2 - Stage 1 Loaded Gain (A_{v1}): Effective collector load $R'_{L1} = R_{C1} \parallel R_{in2} = 4.7\ \text{k} \parallel 1.554\ \text{k} = 1.167$ kΩ. $A_{v1} = -g_{m1} R'_{L1} = -38.46\ \text{mS} \times 1167 = -44.88$ V/V.
- Step 3 - Stage 2 Loaded Gain (A_{v2}): Effective collector load $R'_{L2} = R_{C2} \parallel R_L = 2.2\ \text{k} \parallel 10\ \text{k} = 1.803$ kΩ. $A_{v2} = -g_{m2} R'_{L2} = -76.92\ \text{mS} \times 1803 = -138.69$ V/V.
- Step 4 - Overall System Gain (A_{vs}): $R_{in1} = 40\ \text{k} \parallel 10\ \text{k} \parallel 2.6\ \text{k} = 1.962$ kΩ. $A_{vs} = \left(\frac{1962}{600+1962}\right) \times (-44.88) \times (-138.69) = 0.7658 \times 6224.4 = 4766.6$ V/V (73.56 dB).

Cascode Configuration (CE-CB Pair): High Gain & Miller Effect Elimination

- Cascode Architecture: Common-Emitter stage (Q1) driving a Common-Base stage (Q2) connected in series.
- Stage 1 Load Impedance: Collector load of Q1 is the low input impedance of CB stage Q2: $R_{L1} = R_{in,CB2} = r_{e2} = \frac{V_T}{I_C}$.
- Stage 1 Voltage Gain (A_{v1}): $A_{v1} = -g_{m1} r_{e2} = -\left(\frac{I_C}{V_T}\right)\left(\frac{V_T}{I_C}\right) = -1$ V/V.
- Elimination of Miller Effect: Because $|A_{v1}| = 1$, Miller input capacitance is $C_{M,in} = C_{\mu 1}(1+1) = 2C_{\mu 1}$, completely eliminating Miller multiplication!
- Stage 2 Voltage Gain & Total Gain: Stage 2 (CB) provides high voltage gain $A_{v2} = +g_{m2}(R_C \parallel R_L)$. Overall Cascode gain $A_v = A_{v1}A_{v2} = -g_{m1}(R_C \parallel R_L)$ with wide bandwidth.

Darlington Pair Configuration for Ultra-High Current Gain ($A_i \approx \beta^2$)

- Darlington Structure: Two BJTs connected such that collector terminals are tied together and the emitter of Q1 directly drives the base of Q2.
- Composite Current Gain (β_D): $\beta_D = \beta_1 + \beta_2 + \beta_1\beta_2 \approx \beta_1\beta_2$ (e.g., $100 \times 100 = 10,000$).
- Input Impedance ($r_{\pi,D}$): $r_{\pi,D} = r_{\pi 1} + (1 + \beta_1) r_{\pi 2} \approx 2\beta_1\beta_2 r_{e2}$, providing very high input impedance.
- Base-Emitter Voltage Drop: $V_{BE,D} = V_{BE1} + V_{BE2} \approx 1.4$ V (requires higher turn-on voltage).
- Applications: High-current output drivers, power amplifiers, and high input impedance buffer stages.

Effect of Cascading on System Bandwidth (Bandwidth Shrinkage Phenomenon)

- Bandwidth Shrinkage Phenomenon: Cascading N identical non-interacting amplifier stages increases overall midband gain $(A_M)^N$, but shrinks net system bandwidth.
- System Upper Cutoff Formula ($f_{H,sys}$): $f_{H,sys} = f_H\sqrt{2^{1/N} - 1}$, where f_H is the upper cutoff of an individual stage.
- System Lower Cutoff Formula ($f_{L,sys}$): $f_{L,sys} = \frac{f_L}{\sqrt{2^{1/N}-1}}$, where f_L is the lower cutoff of an individual stage.
- Shrinkage Multiplier Factors: For $N = 1 : 1.00$; $N = 2 : 0.643$; $N = 3 : 0.510$; $N = 4 : 0.435$.
- Net Bandwidth Impact: Lower cutoff $f_{L,sys}$ increases (worsens) while upper cutoff $f_{H,sys}$ decreases (worsens), causing significant bandwidth compression.

Numerical Example 2: 3-Stage Cascaded Amplifier Bandwidth Reduction

- Problem Statement: An amplifier consists of $N = 3$ identical cascaded stages. Each individual stage has a lower cutoff frequency $f_L = 20$ Hz and an upper cutoff frequency $f_H = 500$ kHz. Determine: (1) Single stage bandwidth BW_{single}. (2) Overall 3-stage system lower cutoff $f_{L,sys}$. (3) Overall 3-stage system upper cutoff $f_{H,sys}$. (4) Net system bandwidth BW_{sys}.
- Step 1 - Shrinkage Factor Calculation: Factor $S_N = \sqrt{2^{1/3} - 1} = \sqrt{1.2599 - 1} = \sqrt{0.2599} \approx 0.5098$.
- Step 2 - System Lower Cutoff ($f_{L,sys}$): $f_{L,sys} = \frac{f_L}{S_N} = \frac{20 \text{ Hz}}{0.5098} = 39.23$ Hz.
- Step 3 - System Upper Cutoff ($f_{H,sys}$): $f_{H,sys} = f_H \times S_N = 500 \text{ kHz} \times 0.5098 = 254.91$ kHz.
- Step 4 - Net System Bandwidth (BW_{sys}): Single stage $BW = 500 \text{ kHz} - 20 \text{ Hz} \approx 499.98$ kHz. System $BW_{sys} = 254.91 \text{ kHz} - 39.23 \text{ Hz} = 254.87$ kHz (a 49% bandwidth loss).

Noise Figure Cascading & Friis Formula for Multi-Stage Systems

- Noise Figure Definition (F): Ratio of input SNR to output SNR: $F = \frac{SNR_{in}}{SNR_{out}} \geq 1$. In decibels, $NF(\text{dB}) = 10 \log_{10} F$.
- Friis Formula for Cascaded Noise Figure: $F_{total} = F_1 + \frac{F_2 - 1}{A_{p1}} + \frac{F_3 - 1}{A_{p1} A_{p2}} + \cdots + \frac{F_N - 1}{\prod_{k=1}^{N-1} A_{pk}}$, where F_k is stage noise factor and A_{pk} is stage linear power gain.
- Critical Design Insight: The noise factor of the overall multi-stage system is dominated almost entirely by the FIRST stage (F_1).
- Low-Noise Amplifier (LNA) Requirement: The first stage must combine a very low Noise Figure ($F_1 \approx 1$) with high power gain ($A_{p1} \gg 1$) to suppress noise contributions from subsequent stages.

Summary & Engineering Principles for Multi-Stage Amplifier Gain

- Gain Aggregation: Overall gain is product of loaded stage gains $A_v = \prod A_{vk}$. In decibels, stage gains add: $A_{v(\text{dB})} = \sum A_{vk(\text{dB})}$.
- Inter-Stage Loading: Must include input impedance $R_{in(k+1)}$ when calculating collector load $R'_{Ck} = R_{Ck} \parallel R_{in(k+1)}$.
- High-Performance Topologies: Cascode (CE-CB) eliminates Miller effect for wide bandwidth. Darlington pair provides super-beta current gain $\beta_D \approx \beta^2$.
- Bandwidth Shrinkage: Cascading N identical stages narrows system bandwidth ($f_{H,sys} = f_H\sqrt{2^{1/N} - 1}$, $f_{L,sys} = f_L/\sqrt{2^{1/N} - 1}$).
- Noise Cascading: Friis formula dictates that first-stage LNA gain and low noise figure dominate system SNR.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Learning Roadmap

- Core Roles and Functions of Inter-Stage Coupling Networks
- RC Coupling Technique: Topology, Biasing Isolation, and Audio Range Characteristics
- RC Coupling Limitations: Low-Frequency Attenuation and Inter-Stage Loading
- Direct Coupling Technique: Topologies, DC Response (0 Hz), and DC Level Shifting
- Transformer Coupling Technique: Principles, Electrical Isolation, and Impedance Matching
- Transformer Coupling Limitations: Frequency Non-Linearities, Bulk, and Parasitics
- LC (Tuned) Coupling Technique: High-Frequency RF Tank Circuits and Selectivity
- Detailed Comparative Matrix: Evaluating All Four Coupling Schemes
- Numerical Calculation Example 1: Transformer Impedance Matching for Output Driver
- Numerical Calculation Example 2: LC Tuned Coupling Bandwidth and Q-Factor Design
- Comprehensive Summary and Selection Flowchart

Role and Functions of Inter-Stage Coupling Networks

- Primary Function 1 - AC Signal Transfer: Pass AC output signal from stage k to input of stage $k+1$ with minimal attenuation and phase distortion.
- Primary Function 2 - DC Bias Isolation: Prevent high DC collector voltage V_{Ck} of stage k from overriding or disturbing the DC base bias voltage $V_{B(k+1)}$ of stage $k+1$.
- Primary Function 3 - Impedance Matching: Transform source/stage output impedance to match load/next-stage input impedance for maximum power transfer ($Z_{out} = Z_{in}^*$).
- Coupling Network Selection Factors: Operating frequency range (DC, Audio, RF), power transfer requirements, physical size, component cost, and monolithic IC compatibility.

RC Coupling Technique: Topology, Biasing Isolation, and Characteristics

- Circuit Topology: Coupling capacitor C_C placed in series between collector of Stage 1 and base of Stage 2. Collector resistor R_{C1} acts as AC load and DC bias path.
- DC Bias Isolation Principle: C_C acts as an ideal open circuit to DC ($X_C = \infty$ at $f = 0$), completely blocking DC voltage V_{C1} from affecting Stage 2 base bias V_{B2}.
- AC Signal Passband: At audio frequencies (20 Hz – 20 kHz), C_C impedance $X_C = \frac{1}{2\pi f C_C}$ is negligible, passing AC signals virtually unattenuated.
- Key Advantages: Excellent gain flatness across audio spectrum, low component cost, lightweight, compact discrete implementation.

RC Coupling Frequency Limitations and Inter-Stage Loading

- Low-Frequency Attenuation: At low frequencies ($f < f_L$), reactance $X_C = \frac{1}{2\pi f C_C}$ rises, forming a high-pass filter with Stage 2 input impedance R_{in2} and dropping gain at $+20$ dB/decade.
- High-Frequency Attenuation: At high frequencies ($f > f_H$), internal parasitic capacitances (C_π, C_μ) shunt signal current to ground, causing gain to roll off at -20 dB/decade.
- Inter-Stage Loading Reduction: Collector resistor R_{C1} dissipates DC power and loads Stage 1, reducing loaded voltage gain: $A_{v1} = -g_{m1}(R_{C1} \parallel R_{in2})$.
- Inability to Amplify DC Signals: Impossible to use in bio-medical instrumentation, DC sensors, or direct-coupled operational amplifiers where 0 Hz response is mandatory.

Direct Coupling Technique: Topologies and DC Level-Shifting

- Circuit Topology: Direct electrical connection (wire or resistor) from collector/emitter of Stage 1 directly to base of Stage 2 without capacitors or transformers.
- DC to High-Frequency Response: Operates from DC (0 Hz) up to high frequencies f_H. Essential for operational amplifiers (op-amps), analog ICs, bio-medical sensors, and DC power supplies.
- Cumulative DC Bias Shift Challenge: Collector voltage of Stage 1 becomes base voltage of Stage 2 ($V_{B2} = V_{C1}$). In multi-stage cascades, DC bias voltages climb progressively higher, risking transistor saturation.
- DC Level-Shifting Solutions: (1) Alternating NPN and PNP transistor stages. (2) Zener diode voltage shifters in series. (3) Active current-mirror level shifters in integrated circuits.

Transformer Coupling Technique: Principles and Impedance Matching

- Circuit Topology: Primary winding of an inter-stage transformer acts as collector load for Stage 1; secondary winding connects across base-emitter nodes of Stage 2.
- DC Isolation & Zero DC Load Resistance: Primary winding DC resistance is near zero ($R_{DC} \approx 0\ \Omega$), eliminating DC voltage drop across collector load and maximizing V_{CE} headroom.
- Impedance Transformation Property: A transformer with turns ratio $n = \frac{N_p}{N_s} = \frac{N_1}{N_2}$ reflects secondary load impedance Z_L to primary side as $Z_p = n^2 Z_L = \left(\frac{N_1}{N_2}\right)^2 Z_L$.
- Maximum Power Transfer Application: Transforms low load impedance (e.g. 8 Ω loudspeaker) to match high transistor output impedance (e.g. 2 kΩ), maximizing power transfer efficiency.

Transformer Coupling Frequency Limitations and Practical Drawbacks

- Low-Frequency Degradation: Primary magnetizing inductance L_m causes low-frequency attenuation as $X_{Lm} = 2\pi f L_m$ drops, creating core saturation and frequency distortion below 50 Hz.
- High-Frequency Degradation: Transformer leakage inductance L_l and inter-winding parasitic capacitance C_w cause high-frequency attenuation and self-resonance peaks.
- Poor Frequency Response Uniformity: Non-flat frequency response curve makes transformer coupling unsuitable for high-fidelity (Hi-Fi) audio amplification.
- Physical Constraints: Transformers are bulky, heavy, expensive, introduce magnetic hum pickup, and CANNOT be integrated onto monolithic silicon IC chips.

LC (Tuned) Coupling Technique: High-Frequency RF Bandpass Cascades

- Circuit Topology: A parallel LC resonant tank circuit (L in parallel with C) serves as the collector load for Stage 1, coupled to Stage 2 via a small coupling capacitor.
- Resonant Frequency (f_0): Implements a narrow bandpass filter centered at $f_0 = \frac{1}{2\pi\sqrt{LC}}$. Tank impedance peaks sharply to $R_p = Q\omega_0 L$ at resonance.
- Quality Factor (Q) & Selectivity: Tank $Q = \frac{R_p}{\omega_0 L} = \omega_0 R_p C$. High Q provides steep selectivity, suppressing adjacent channel interference in radio receivers.
- Passband Bandwidth (BW): 3-dB bandpass bandwidth $BW = \frac{f_0}{Q}$. Ideal for RF receivers, IF amplifiers (455 kHz, 10.7 MHz), and wireless transmitters.

Comprehensive Comparative Analysis of Coupling Techniques

- Direct Coupling: Frequency Range = 0 Hz (DC) to $>$ 100 MHz; DC Isolation = None; Impedance Matching = Poor; IC Integrability = Excellent (Preferred in ICs); Cost = Very Low.
- RC Coupling: Frequency Range = 20 Hz – 20 kHz (Audio); DC Isolation = Excellent (via C_C); Impedance Matching = Poor; IC Integrability = Poor ($C_C > 10$ pF too large); Cost = Low.
- Transformer Coupling: Frequency Range = Narrow audio/RF; DC Isolation = Excellent (magnetic); Impedance Matching = EXCELLENT (n^2 ratio); IC Integrability = Impossible; Cost = High.
- LC (Tuned) Coupling: Frequency Range = High RF (100 kHz – GHz); DC Isolation = Good (via C); Impedance Matching = Moderate; IC Integrability = Moderate (RF-IC spirals); Cost = Moderate.

Design Calculation Example 1: Transformer Matching for Output Driver

- Problem Statement: A BJT power stage has an output internal resistance $R_{out} = 1.8$ kΩ. It must drive a low-impedance loudspeaker $R_L = 8$ Ω. (1) Calculate required transformer turns ratio $n = N_p/N_s$ for maximum power transfer. (2) Compare power delivered to load with transformer vs direct RC connection.
- Step 1 - Turns Ratio Calculation: For maximum power transfer, primary reflected impedance $R_p = R_{out} = 1800$ Ω. Using $R_p = n^2 R_L \implies n = \sqrt{\frac{R_p}{R_L}} = \sqrt{\frac{1800}{8}} = \sqrt{225} = 15:1$.
- Step 2 - Power Comparison: AC signal voltage source $V_{oc} = 12\ V_{rms}$.
- With Transformer Matching: Load power $P_L = \frac{(V_{oc}/2)^2}{R_p} = \frac{6^2}{1800} = \frac{36}{1800} = 20$ mW.
- Without Transformer (Direct Connection): $I_L = \frac{12}{1800+8} = 6.637\ mA_{rms}$. Load power $P_{L,\text{direct}} = I_L^2 R_L = (6.637\ \text{mA})^2 \times 8\ \Omega = 0.352$ mW. Transformer matching increases output power by over 56 times (56.8×)!

Design Calculation Example 2: LC Tuned Coupling Bandwidth and Q-Factor Design

- Problem Statement: An IF amplifier in an AM radio receiver operates at a center frequency $f_0 = 455$ kHz using LC tuned coupling with inductance $L = 1$ mH. The parallel tank resistance is $R_p = 50$ kΩ. Calculate: (1) Required tuning capacitance C. (2) Tank Quality Factor Q. (3) 3-dB passband bandwidth BW.
- Step 1 - Calculate Tuning Capacitance C: Using $f_0 = \frac{1}{2\pi\sqrt{LC}} \implies C = \frac{1}{4\pi^2 f_0^2 L} = \frac{1}{4\pi^2(455\times10^3)^2\times10^{-3}} = 122.2$ pF.
- Step 2 - Calculate Tank Reactance X_L: $X_L = 2\pi f_0 L = 2\pi \times 455 \times 10^3 \times 10^{-3} = 2858.8\ \Omega$.
- Step 3 - Calculate Quality Factor Q: $Q = \frac{R_p}{X_L} = \frac{50{,}000\ \Omega}{2858.8\ \Omega} = 17.49$.
- Step 4 - Calculate 3-dB Bandwidth BW: $BW = \frac{f_0}{Q} = \frac{455\text{ kHz}}{17.49} = 26.01$ kHz (ideal for selecting 10 kHz AM audio channels while suppressing adjacent stations).

Summary & Selection Criteria for Multi-Stage Coupling Networks

- Direct Coupling: Extends response down to DC (0 Hz). Mandatory for IC fabrication; requires level shifters to manage DC bias buildup.
- RC Coupling: Standard for discrete audio amplifiers (20 Hz – 20 kHz). Blocks DC bias using C_C; inexpensive but causes inter-stage loading.
- Transformer Coupling: Provides maximum power transfer via turns ratio $n = \sqrt{R_p/R_s}$ and electrical isolation, but is bulky and non-linear.
- LC Tuned Coupling: Provides narrow-band high-frequency RF selectivity ($f_0 = \frac{1}{2\pi\sqrt{LC}}$, $BW = f_0/Q$). Ideal for wireless receiver IF stages.
- Selection Strategy: Match coupling topology to operational frequency range, integration constraints, and power efficiency requirements.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Outline

- 1. Multi-Stage Architecture: Cascaded BJT RC Coupling and DC Biasing Isolation
- 2. Midband Voltage Gain Derivation: Small-Signal AC Equivalent & Stage-to-Stage Interstage Loading
- 3. Low-Frequency Response: Coupling Capacitors (C_C1, C_C2, C_C3) and Emitter Bypass Capacitors (C_E1, C_E2) Pole Calculations
- 4. High-Frequency Response: Hybrid-pi Model, Parasitic Capacitances (C_pi, C_mu), and Miller Effect Transformation
- 5. Multistage Frequency Response Metrics: Dominant Pole Approximations, Bandwidth Shrinkage, and Gain-Bandwidth Product
- 6. Step-by-Step Comprehensive Numerical Design Example and Performance Trade-offs

Two-Stage RC Coupled Amplifier Circuit Architecture & Biasing

- Circuit Configuration: Two cascaded Common-Emitter (CE) BJT stages connected via an interstage coupling capacitor C_C2, with input coupling capacitor C_C1 and output coupling capacitor C_C3.
- DC Biasing Isolation: Coupling capacitors block DC voltage components, allowing independent Q-point biasing (V_CEQ1, I_CQ1 and V_CEQ2, I_CQ2) for each stage via voltage dividers (R_11, R_12 and R_21, R_22).
- AC Signal Coupling: Coupling capacitors present low reactive impedance (X_C = 1 / (2 *pi* f * C) approx 0) in the midband frequency range, allowing AC signal transmission with minimal attenuation between stages.
- Emitter Bypass Networks: Resistors R_E1 and R_E2 provide thermal Q-point stabilization against beta variations, while parallel capacitors C_E1 and C_E2 bypass AC signals to ground to prevent degenerative AC gain reduction.
- Interstage Loading Interaction: The input impedance of the second stage R_in2 = R_21 —— R_22 —— r_pi2 acts as a parallel AC load on the collector resistor R_C1 of the first stage, reducing the effective first-stage gain.

Midband Voltage Gain Derivation & Interstage Loading

- Small-Signal Parameters: Hybrid-pi parameters for stage i: transconductance g_mi = I_CQi / V_T (where V_T approx 26 mV at 300K) and base input resistance r_pi_i = beta_0i / g_mi.
- Stage 2 Voltage Gain (A_v2): The load seen by stage 2 collector is R_L2' = R_C2 —— R_L. Gain A_v2 = V_o / V_i2 = -g_m2 * (R_C2 —— R_L).
- Stage 1 Voltage Gain (A_v1): Stage 1 collector sees AC load R_L1' = R_C1 —— R_B2 —— r_pi2, where R_B2 = R_21 —— R_22. Gain A_v1 = V_i2 / V_i1 = -g_m1 * (R_C1 —— R_B2 —— r_pi2).
- Total Midband System Voltage Gain (A_v0): Calculated as the product of individual voltage gains: A_v0 = A_v1 *A_v2 = g_m1* g_m2 *(R_C1 —— R_B2 —— r_pi2)* (R_C2 —— R_L).
- Overall Voltage Gain from Signal Source (A_vs0): Incorporating source resistance R_s: A_vs0 = (V_o / V_s) = A_v0 * (R_in1 / (R_s + R_in1)), where R_in1 = R_B1 —— r_pi1.
- Decibel Representation: Overall gain in dB is A_v0,dB = 20 * log10(—A_v0—) = A_v1,dB + A_v2,dB.

Low-Frequency Response: Coupling Capacitor Poles Analysis

- Low-Frequency Attenuation Mechanisms: At low frequencies, capacitive reactance X_C = 1 / (2 *pi* f * C) increases, causing potential divider action with circuit resistances and rolling off gain at 20 dB/decade per capacitor.
- Input Coupling Capacitor Pole (f_L,C1): Sees resistance R_eq,C1 = R_s + R_in1 = R_s + (R_11 —— R_12 —— r_pi1). Cutoff frequency f_L,C1 = 1 / (2 *pi* (R_s + R_in1) * C_C1).
- Interstage Coupling Capacitor Pole (f_L,C2): Sees output resistance of stage 1 in series with input resistance of stage 2: R_eq,C2 = (R_C1 —— r_o1) + (R_B2 —— r_pi2). Cutoff frequency f_L,C2 = 1 / (2 *pi* (R_C1 + R_in2) * C_C2).
- Output Coupling Capacitor Pole (f_L,C3): Sees output resistance of stage 2 in series with load resistance: R_eq,C3 = R_C2 + R_L. Cutoff frequency f_L,C3 = 1 / (2 *pi* (R_C2 + R_L) * C_C3).
- High-Pass Transfer Function Formulation: Each coupling capacitor contributes a first-order high-pass transfer factor s / (s + omega_Li), where omega_Li = 2 *pi* f_Li.

Low-Frequency Response: Emitter Bypass Capacitor Poles

- Bypass Capacitor Action: Capacitor C_E in parallel with R_E creates a pole-zero pair in the low-frequency transfer function. At low frequencies, incomplete AC bypassing introduces emitter degeneration.
- Equivalent Resistance Seen by C_E1: Reflected source and base resistance looking into the emitter of Stage 1: R_eq,E1 = R_E1 —— ((r_pi1 + (R_s —— R_B1)) / (1 + beta_0)).
- Stage 1 Emitter Cutoff Frequency (f_L,E1): Derived as f_L,E1 = 1 / (2 *pi* R_eq,E1 * C_E1). Because R_eq,E1 is typically small (tens of ohms), f_L,E1 requires large capacitance (e.g., 10 uF - 100 uF) to keep the pole low.
- Stage 2 Emitter Cutoff Frequency (f_L,E2): Equivalent resistance R_eq,E2 = R_E2 —— ((r_pi2 + (R_C1 —— R_B2)) / (1 + beta_0)), giving cutoff f_L,E2 = 1 / (2 *pi* R_eq,E2 * C_E2).
- Zero Frequency of Emitter Network: The zero occurs at lower frequency f_Z,Ei = 1 / (2 *pi* R_Ei * C_Ei), below which gain flattens out to unbypassed gain A_v,unbypassed approx -R_C / R_E.

Low-Frequency Bode Plot & Dominant Pole Determination

- Overall Low-Frequency System Transfer Function: A_v(s) = A_v0 * product_{i=1}^{5} (s / (s + omega_Li)) (assuming 3 coupling and 2 bypass poles).
- Asymmetrical Low-Frequency Slope: For frequencies omega ¡¡ omega_L,min, the asymptotic slope rolls off at +100 dB/decade (+5 x 20 dB/dec) with a phase lead approaching +450 degrees.
- Dominant Pole Approximation: If one low-frequency pole omega_L,dom is significantly higher than all other low-frequency poles (by a factor of ¿= 4), then lower 3-dB cutoff frequency f_L approx f_L,dom.
- Non-Dominant Pole Interaction Formula: When multiple low-frequency poles are close to each other, the overall lower 3-dB cutoff frequency is approximated by: f_L approx sqrt(f_L1^2 + f_L2^2 + f_L3^2 + f_L,E1^2 + f_L,E2^2).
- Design Rule for Dominant Pole Placement: Design rules typically set f_L,E1 and f_L,E2 as the dominant lower cutoff poles to minimize required physical capacitor sizes.

High-Frequency Response: Hybrid-pi Model Parasitic Capacitances

- BJT Internal Parasitic Capacitances: High-frequency roll-off is dictated by internal junction capacitances: base-emitter junction capacitance C_pi = C_b'e (diffusion + depletion) and base-collector junction capacitance C_mu = C_b'c (depletion capacitance).
- Transistor Gain-Bandwidth Product (f_T): The unity-current-gain frequency f_T = g_m / (2 *pi* (C_pi + C_mu)). Typical values for RF/small-signal BJTs range from 300 MHz to several GHz.
- Diffusion Capacitance Dynamics: C_de = g_m * tau_F, where tau_F is the forward transit time of minority carriers across the base (typically 10 - 500 ps). C_de dominates C_pi at higher collector currents.
- Depletion Capacitance Dependence: C_mu = C_mu0 / (1 + V_CB / V_0)^m, where m approx 0.33 - 0.5 depending on junction grading.
- Stray Wiring Capacitances (C_W): PCB traces, interconnects, and socket capacitances add parasitic shunt capacitance C_W1, C_W2 (typically 2 - 10 pF) to ground at each node.

High-Frequency Response: Miller Effect Transformation

- Miller Theorem Statement: A feedback impedance Z_F connected between input and output nodes with inverted voltage gain A_v = V_o / V_i can be decoupled into equivalent input and output shunt impedances to ground.
- Miller Input Capacitance (C_M,in): C_M,in = C_mu *(1 - A_v). For an inverting stage where A_v = -—A_v—, C_M,in = C_mu* (1 + —A_v—).
- Miller Output Capacitance (C_M,out): C_M,out = C_mu * (1 - 1 / A_v) approx C_mu (since —A_v— ¿¿ 1).
- Stage 1 Total High-Frequency Input Capacitance (C_in1,hi): C_in1,hi = C_pi1 + C_mu1 * (1 + —A_v1—) + C_W1. Because —A_v1— is large, C_M,in1 completely dominates the input node capacitance!
- Stage 2 Total High-Frequency Input Capacitance (C_in2,hi): C_in2,hi = C_pi2 + C_mu2 * (1 + —A_v2—) + C_W2.

High-Frequency Cutoff Frequency f_H & Dominant Pole Analysis

- Stage 1 Input High-Frequency Pole (f_H1): Equivalent Thevenin resistance seen by C_in1,hi: R_th1 = R_s —— R_B1 —— r_pi1. Cutoff frequency f_H1 = 1 / (2 *pi* R_th1 * C_in1,hi).
- Interstage High-Frequency Pole (f_H2): Equivalent Thevenin resistance seen by C_in2,hi: R_th2 = R_C1 —— R_B2 —— r_pi2 —— r_o1. Cutoff frequency f_H2 = 1 / (2 *pi* R_th2 * C_in2,hi).
- Output High-Frequency Pole (f_H3): Total output capacitance C_out2 = C_mu2 + C_W3 seeing resistance R_th3 = R_C2 —— R_L —— r_o2. Cutoff frequency f_H3 = 1 / (2 *pi* R_th3 * C_out2).
- Overall Upper 3-dB Frequency Estimate (f_H): Combining non-dominant high-frequency poles using the reciprocal square-root approximation: 1 / f_H approx 1.1 * sqrt(1/f_H1^2 + 1/f_H2^2 + 1/f_H3^2).
- Open-Circuit Time Constant (OCT) Method: Alternative robust estimation f_H approx 1 / (2 *pi* sum(tau_Hi_0)), where tau_Hi_0 = R_i0 * C_i.

Multistage Bandwidth Shrinkage & Gain-Bandwidth Product

- Identical Cascaded Stage Bandwidth Reduction: For N identical non-interacting amplifier stages each with upper cutoff f_H1 and lower cutoff f_L1:
- System Upper Cutoff Formula: f_H,sys = f_H1 *sqrt(2^(1/N) - 1). For N = 2 stages, sqrt(2^(1/2)-1) = sqrt(sqrt(2)-1) approx 0.643 =¿ f_H,sys = 0.643* f_H1.
- System Lower Cutoff Formula: f_L,sys = f_L1 / sqrt(2^(1/N) - 1). For N = 2 stages, f_L,sys = f_L1 / 0.643 = 1.56 * f_L1.
- System Bandwidth Shrinkage: Overall system bandwidth BW_sys = f_H,sys - f_L,sys approx 0.643 *f_H1 - 1.56* f_L1. Cascading stages narrows overall passband bandwidth!
- Gain-Bandwidth Product (GBP) Trade-Off: While cascading boosts midband voltage gain (A_v0 = A_v1^N), the overall bandwidth reduces, demanding careful pole management in high-frequency communications.

Comprehensive Worked Numerical Design Example

- Circuit Parameters: Two identical BJT stages with g_m = 40 mS, r_pi = 2.5 kOhm, R_C1 = R_C2 = 4 kOhm, R_B1 = R_B2 = 50 kOhm, R_s = 1 kOhm, R_L = 10 kOhm.
- Capacitor Values: C_C1 = C_C2 = C_C3 = 10 uF, C_E1 = C_E2 = 100 uF, C_pi = 30 pF, C_mu = 2 pF.
- Step 1: Calculate Stage Gains: R_L2' = 4k —— 10k = 2.86 kOhm =¿ A_v2 = -40 mS * 2.86 kOhm = -114.4.
- Stage 1 Load: R_L1' = 4k —— 50k —— 2.5k = 1.488 kOhm =¿ A_v1 = -40 mS * 1.488 kOhm = -59.5.
- Total Midband Gain: A_v0 = A_v1 *A_v2 = (-59.5)* (-114.4) = +6807 (76.66 dB).
- Step 2: Miller Capacitance: C_M,in1 = 2 pF * (1 + 59.5) = 121 pF =¿ C_in1,hi = 30 + 121 = 151 pF.
- C_M,in2 = 2 pF * (1 + 114.4) = 230.8 pF =¿ C_in2,hi = 30 + 230.8 = 260.8 pF.
- Step 3: High-Frequency Cutoffs: R_th1 = 1k —— 50k —— 2.5k = 704 Ohm =¿ f_H1 = 1 / (2 *pi* 704 * 151pF) = 1.497 MHz.
- R_th2 = 1.488 kOhm =¿ f_H2 = 1 / (2 *pi* 1488 * 260.8pF) = 410.2 kHz.
- Overall Upper Cutoff: f_H approx 1 / sqrt(1/(1.497M)^2 + 1/(410.2k)^2) = 395.7 kHz.

Frequency Response Comparison: Single-Stage vs Two-Stage RC Coupled

- Midband Voltage Gain Comparison: Single-stage CE provides A_v approx 50-100, whereas two-stage RC coupled provides A_v0 approx 2,000-10,000 (34 dB - 80 dB gain range).
- Bandwidth Comparison: Single-stage features wider bandwidth (BW approx 2 - 5 MHz), whereas two-stage suffers bandwidth compression (BW approx 300 kHz - 800 kHz).
- Phase Response Comparison: Single-stage exhibits 180-degree phase shift in midband (-90 deg at f_L, -270 deg at f_H). Two-stage exhibits 0-degree (360 deg) midband phase shift.
- Noise & Distortion Trade-Offs: Two-stage amplifies first-stage thermal and shot noise; cumulative phase shifts at high frequencies increase susceptibility to parasitic oscillation if stray feedback exists.
- Practical Design Applications: Audio preamplifiers, sensor signal conditioning blocks, intermediate frequency (IF) gain stages in radio receivers.

Summary & Key Engineering Takeaways

- Midband Gain Equation: A_v0 = A_v1 $A_{v2} = [-g_{m1}$ (R_C1 —— R_B2 —— r_pi2)] $[-g_{m2}$ (R_C2 —— R_L)].
- Low-Frequency Roll-Off: Dictated by external coupling capacitors (C_C1, C_C2, C_C3) and emitter bypass capacitors (C_E1, C_E2). Dominant pole sets lower cutoff f_L.
- High-Frequency Roll-Off: Dictated by BJT parasitic capacitances (C_pi, C_mu) and Miller multiplication C_M,in = C_mu * (1 + —A_v—), setting upper cutoff f_H.
- Multistage Bandwidth Shrinkage: For 2 identical stages, f_H,sys = 0.643 f_{H1} and $f_{L,sys} = 1.56$ f_L1, narrowing net passband.
- Design Guideline: Select large emitter bypass capacitors to prevent dominant low-frequency gain degradation, and use low source/load resistances to maximize high-frequency bandwidth.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Outline

- 1. Universal Feedback Architecture: Open-Loop Amplifier, Feedback Network, and Summing Junctions
- 2. Closed-Loop Gain Derivation: Mathematical Formulation of A_f = A / (1 + A * beta) and Loop Gain T
- 3. Negative Feedback Desensitization: Immunity to Parameter Variations, Temperature Drift, and Aging
- 4. Performance Modifications: Bandwidth Extension, Gain-Bandwidth Invariance, and Harmonic Distortion Reduction
- 5. Positive Feedback Mechanics: Regenerative Action, Latching, and Barkhausen Stability Criterion (—A * beta— = 1, phase = 0 deg)
- 6. Quantitative Engineering Design Examples and Comparative Performance Analysis Matrix

General Feedback System Model & Block Diagram Topology

- System Components: A feedback amplifier consists of a basic open-loop forward amplifier with transfer function A(s), a feedback network with transfer function beta(s), a sampling network, and a mixing/summing junction.
- Signal Variables: Input signal x_s (voltage or current), feedback signal x_f = beta * x_o, net input signal x_i = x_s - x_f (for negative feedback) or x_i = x_s + x_f (for positive feedback).
- Forward Path Amplifier (A): Idealized open-loop gain A = x_o / x_i. Internal parameters are sensitive to temperature, DC bias shifts, and manufacturing tolerances.
- Feedback Network (beta): Passive resistive/reactive attenuation network beta = x_f / x_o (typically beta ¡= 1). Designed with precise, temperature-stable passive components (resistors/capacitors).
- Mixer/Summing Node: Combines source signal x_s and feedback signal x_f to generate error/effective drive signal x_i.

Derivation of Closed-Loop Gain A_f & Loop Gain Dynamics

- Algebraic Derivation for Negative Feedback: Output equation x_o = A *x_i. Substituting net input x_i = x_s - x_f gives x_o = A* (x_s - beta * x_o).
- Rearranging Terms: x_o + A *beta* x_o = A *x_s =¿ x_o* (1 + A *beta) = A* x_s.
- Closed-Loop Gain Formula: A_f = x_o / x_s = A / (1 + A * beta).
- Loop Gain (T): The product T = A * beta represents the total gain around the feedback loop (from mixer through forward path and feedback network back to mixer).
- Amount of Feedback (F): Defined as F = 1 + A *beta = 1 + T. Expressed in decibels as F_dB = 20* log10(—1 + A * beta—).
- Asymptotic Gain Limit: Under heavy negative feedback (where A *beta ¿¿ 1): A_f approx A / (A* beta) = 1 / beta! Closed-loop gain becomes virtually independent of open-loop gain A.

Mechanisms of Negative Feedback: Desensitization of Gain

- Sensitivity Definition: Fractional change in closed-loop gain A_f relative to fractional change in open-loop gain A: S_A^{A_f} = (dA_f / A_f) / (dA / A).
- Derivation of Sensitivity Reduction: Differentiating A_f with respect to A gives dA_f / dA = d/dA [A / (1 + A *beta)] = 1 / (1 + A* beta)^2.
- Sensitivity Equation: dA_f / A_f = (1 / (1 + A *beta)) (dA / A). Fractional gain variation is reduced by the factor (1 + A * beta).
- Thermal & Aging Immunity: Temperature-induced variations in BJT beta_0 or MOSFET g_m (which cause 50% - 100% drift in open-loop gain A) cause negligible drift (¡ 1%) in closed-loop gain A_f.
- Nonlinear Stabilization: Linearizes overall amplifier transfer characteristics, even when transistor open-loop gain A fluctuates across large signal swings.

Bandwidth Extension via Negative Feedback

- High-Frequency Response with Feedback: Single-pole open-loop amplifier A(s) = A_0 / (1 + s / omega_H), where A_0 is open-loop midband gain and omega_H = 2 *pi* f_H is upper cutoff frequency.
- Closed-Loop Frequency Transfer Function: A_f(s) = [A_0 / (1 + s / omega_H)] / [1 + beta *A_0 / (1 + s / omega_H)] = A_0 / (1 + A_0* beta + s / omega_H).
- Dividing by (1 + A_0 *beta): A_f(s) = [A_0 / (1 + A_0* beta)] / [1 + s / (omega_H *(1 + A_0* beta))].
- Closed-Loop Cutoff Frequency: New upper 3-dB frequency omega_Hf = omega_H *(1 + A_0* beta) =¿ f_Hf = f_H *(1 + A_0* beta). Upper cutoff frequency is extended by (1 + A_0 * beta)!
- Closed-Loop Lower Cutoff Frequency: Lower 3-dB frequency is lowered: f_Lf = f_L / (1 + A_0 * beta).
- Gain-Bandwidth Product Invariance: A_f0 *f_Hf = [A_0 / (1 + A_0* beta)] *[f_H* (1 + A_0 *beta)] = A_0* f_H = Constant (GBP).

Nonlinear Distortion & Noise Reduction Dynamics

- Harmonic Distortion Reduction: Transistor non-linear transfer functions generate output harmonic distortion D. Applying negative feedback reduces output harmonic distortion to D_f = D / (1 + A * beta).
- Linearity Enhancement: By suppressing second and third harmonic amplitudes, negative feedback transforms non-linear amplifiers into high-fidelity linear stages.
- Signal-to-Noise Ratio (SNR) Analysis: Consider noise voltage V_n injected inside an amplifier stage: V_o = A_1 *A_2* V_s + A_2 * V_n.
- Closed-Loop Output with Noise: V_of = (A_1 *A_2* V_s) / (1 + A_1 *A_2* beta) + (A_2 *V_n) / (1 + A_1* A_2 * beta).
- Noise Limitation: Negative feedback reduces output noise generated WITHIN the feedback loop, but CANNOT improve SNR for noise present at the primary input source (V_ni)!

Mechanisms of Positive Feedback & Regenerative Action

- Positive Feedback Transfer Function: Feedback signal x_f is added in-phase at the mixer: x_i = x_s + x_f = x_s + beta * x_o.
- Closed-Loop Gain Formulation: A_f = A / (1 - A * beta).
- Regenerative Gain Enhancement: For 0 ¡ A *beta ¡ 1, the denominator (1 - A* beta) ¡ 1, causing closed-loop gain A_f to EXCEED open-loop gain A (gain enhancement).
- Instability & Saturation Region: As loop gain A * beta approaches +1, closed-loop gain A_f -¿ infinity. The system becomes unstable; any microscopic noise pulse triggers exponential growth until circuit supply rails latch.
- Applications of Positive Feedback: Controlled positive feedback is utilized in oscillators (sinusoidal/waveform generation), Schmitt triggers (bistable multivibrators with hysteresis), and regenerative receivers.

Barkhausen Criterion for Sustained Oscillations

- Oscillator Definition: An electronic circuit that converts DC power into a periodic AC output signal without requiring any external AC input (x_s = 0).
- Barkhausen Condition 1 (Loop Gain Magnitude): The magnitude of the loop transmission around the feedback loop must equal unity at the desired frequency of oscillation f_0: —T(j *omega_0)— = —A(j* omega_0) *beta(j* omega_0)— = 1.
- Barkhausen Condition 2 (Loop Phase Shift): The total phase shift around the feedback loop must equal zero degrees or an integer multiple of 360 degrees: angle(A *beta) = 2* n * pi (where n = 0, 1, 2...).
- Practical Oscillation Build-Up: To guarantee initial startup from thermal noise, practical designs set initial loop gain magnitude slightly higher: —A * beta— approx 1.05 - 1.1.
- Amplitude Stabilization: Non-linear amplitude limiting (such as FET AGC circuits, thermistors, or diode clamps) reduces effective gain to —A * beta— = 1 precisely at steady state to prevent signal clipping.

Frequency Response & Stability Margins (Gain & Phase Margins)

- Potential Instability in Negative Feedback Amplifiers: At high frequencies, internal amplifier poles introduce phase lag. If phase lag reaches 180 degrees while —A * beta— ¿= 1, negative feedback turns into positive feedback!
- Gain Crossover Frequency (f_c): The frequency at which loop gain magnitude equals unity (0 dB): —A(j *omega_c)* beta(j * omega_c)— = 1 (0 dB).
- Phase Crossover Frequency (f_180): The frequency at which loop phase shift equals -180 degrees: angle(A(j *omega_180)* beta(j * omega_180)) = -180 deg.
- Phase Margin (PM): PM = 180 deg + angle(A(j *omega_c)* beta(j * omega_c)). For stable operation without ringing, PM ¿= 45 deg (60 deg optimal).
- Gain Margin (GM): GM = -20 *log10(—A(j* omega_180) *beta(j* omega_180)—). Indicates how much loop gain can increase before instability occurs (typically GM ¿= 6 dB - 10 dB).

Quantitative Analysis of Negative Feedback Amplifier

- Problem Statement: An open-loop amplifier has midband voltage gain A_0 = 10,000 (80 dB), upper 3-dB frequency f_H = 1 kHz, and second-harmonic distortion D = 10%. Calculate negative feedback properties with beta = 0.009.
- Step 1: Calculate Loop Gain & Feedback Factor: Loop gain T = A_0 *beta = 10,000* 0.009 = 90. Amount of feedback F = 1 + A_0 * beta = 1 + 90 = 91 (39.18 dB).
- Step 2: Calculate Closed-Loop Gain (A_f): A_f = A_0 / (1 + A_0 * beta) = 10,000 / 91 = 109.89 (40.82 dB). Note: 1 / beta = 1 / 0.009 = 111.11.
- Step 3: Calculate Gain Sensitivity Reduction: If open-loop gain A drops by 20% (dA/A = -0.20), closed-loop gain variation is dA_f / A_f = (-0.20) / 91 = -0.0022 = -0.22%!
- Step 4: Calculate Closed-Loop Bandwidth: f_Hf = f_H *(1 + A_0* beta) = 1 kHz * 91 = 91 kHz.
- Step 5: Calculate Reduced Distortion: D_f = D / (1 + A_0 * beta) = 10% / 91 = 0.11%.

Quantitative Oscillator Design using Barkhausen Criterion

- Problem Statement: Design an RC Phase-Shift Oscillator core using a 3-stage RC ladder network in the feedback path. Determine the required open-loop amplifier gain A and frequency of oscillation f_0.
- RC Ladder Feedback Transfer Function: beta(s) = (s *R* C)^3 / [(s *R* C)^3 + 6 *(s* R *C)^2 + 5* (s *R* C) + 1].
- Step 1: Setting Imaginary Part to Zero for Phase Shift: Setting s = j *omega and equating imaginary terms to zero gives: -omega^3* R^3 *C^3 + 5* omega *R* C = 0.
- Oscillation Frequency Derivation: omega_0^2 *R^2* C^2 = 6 =¿ omega_0 = 1 / (sqrt(6) *R* C) =¿ f_0 = 1 / (2 *pi* sqrt(6) *R* C).
- Step 2: Evaluating Feedback Factor at f_0: Substituting omega_0 into beta(j *omega_0) yields beta(j* omega_0) = -1 / 29.
- Step 3: Applying Barkhausen Gain Condition: For sustained oscillations, —A *beta— = 1 =¿ A* (-1 / 29) = -1 =¿ A = +29.
- Conclusion: The forward amplifier must provide an inverting gain of at least A = -29 (or non-inverting gain +29 with net 180 deg ladder phase shift) to sustain oscillations.

Comparative Performance Matrix: Negative vs. Positive Feedback

- Voltage Gain: Negative feedback reduces gain [A_f = A / (1 + A *beta)]; Positive feedback increases gain [A_f = A / (1 - A* beta)].
- Gain Stability: Negative feedback increases stability [dA_f/A_f = (dA/A)/(1 + A * beta)]; Positive feedback decreases stability (leads to saturation/latching).
- System Bandwidth: Negative feedback expands bandwidth [f_Hf = f_H *(1 + A* beta)]; Positive feedback narrows bandwidth.
- Nonlinear Distortion: Negative feedback suppresses distortion [D_f = D / (1 + A * beta)]; Positive feedback increases distortion.
- Terminal Noise (Internal): Negative feedback reduces internal noise; Positive feedback amplifies noise.
- Primary Applications: Negative feedback is used in audio/RF linear amplifiers and operational amplifiers; Positive feedback is used in sinusoidal oscillators, relaxation oscillators, and Schmitt triggers.

Summary & Core Takeaways of Feedback Concepts

- Closed-Loop Transfer Function: A_f = A / (1 +/- A * beta). Negative feedback uses '+', Positive feedback uses '-'.
- Desensitization & Independence: Under heavy negative feedback (A * beta ¿¿ 1), closed-loop gain depends solely on passive components: A_f approx 1 / beta.
- Performance Enhancements: Negative feedback increases upper cutoff frequency (f_Hf = f_H *(1 + A* beta)), maintains constant Gain-Bandwidth Product, and lowers distortion (D_f = D / (1 + A * beta)).
- Barkhausen Criteria: Sustained oscillation requires —A *beta— = 1 and loop phase shift angle(A* beta) = 0 deg or 360 deg.
- Stability Margin Requirements: Amplifier stability requires positive Phase Margin (PM ¿= 45 deg) and Gain Margin (GM ¿= 6 dB) to prevent unwanted oscillations.

Electronics Circuit and Application (ECA)

Complete Course Presentation

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Lecture Agenda & Outline

- 1. Output Signal Sampling: Voltage (Node/Shunt) vs. Current (Loop/Series) Sampling Mechanics
- 2. Input Signal Summing: Series (Voltage Comparison) vs. Shunt (Current Comparison) Mixing Mechanics
- 3. Two-Port Parameter Matrices: Selection of h, g, y, and z Parameters for Feedback Networks
- 4. Feedback Loading Analysis: Derivation of Input/Output Loading Resistances (r_11 and r_22)
- 5. The Systematic 5-Step Feedback Analysis Algorithm for Discrete Transistor Circuits
- 6. Step-by-Step Circuit Calculations: Voltage-Series and Current-Series Transistor Amplifier Case Studies

Output Signal Sampling: Voltage (Shunt) vs. Current (Series)

- Voltage (Shunt) Sampling Mechanism: The feedback network is connected in PARALLEL across output load terminals to sense output voltage V_o.
- Ideal Voltage Sampler Properties: To avoid loading the output, an ideal voltage sampler presents infinite input impedance looking into the feedback network (R_in,beta -¿ infinity).
- Effect on Output Impedance: Voltage sampling stabilizes output voltage V_o, resulting in a DRAMATIC REDUCTION of closed-loop output resistance: R_of = R_o / (1 + A * beta).
- Current (Series) Sampling Mechanism: The feedback network is connected in SERIES with output load loop to sense output current I_o.
- Ideal Current Sampler Properties: To avoid loading the output loop, an ideal current sampler presents zero insertion impedance looking into the feedback network (R_in,beta -¿ 0).
- Effect on Output Impedance: Current sampling stabilizes output current I_o, resulting in a DRAMATIC INCREASE of closed-loop output resistance: R_of = R_o *(1 + A* beta).

Input Signal Summing: Series (Voltage) vs. Shunt (Current)

- Series (Voltage Comparison) Summing: The feedback signal V_f is connected in SERIES with signal source V_s at input: V_i = V_s - V_f.
- Ideal Series Summer Properties: Series mixing requires high input impedance for voltage sensing. Closed-loop input resistance INCREASES: R_inf = R_in *(1 + A* beta).
- Voltage Source Matching: Ideal for signal sources with low source resistance R_s (Thevenin equivalent voltage sources).
- Shunt (Current Comparison) Summing: The feedback signal I_f is connected in PARALLEL (shunt) with signal source I_s at input node: I_i = I_s - I_f.
- Ideal Shunt Summer Properties: Shunt mixing draws current from input node. Closed-loop input resistance DECREASES: R_inf = R_in / (1 + A * beta).
- Current Source Matching: Ideal for signal sources with high source resistance R_s (Norton equivalent current sources).

The Four Basic Feedback Topologies & Ideal Amplifier Models

- 1. Voltage-Series (Series-Shunt) Topology: Samples V_o, sums V_f in series. Ideal Voltage Amplifier (V_o / V_s). High R_inf, Low R_of.
- 2. Current-Series (Series-Series) Topology: Samples I_o, sums V_f in series. Ideal Transconductance Amplifier (I_o / V_s). High R_inf, High R_of.
- 3. Voltage-Shunt (Shunt-Shunt) Topology: Samples V_o, sums I_f in shunt. Ideal Transresistance Amplifier (V_o / I_s). Low R_inf, Low R_of.
- 4. Current-Shunt (Shunt-Series) Topology: Samples I_o, sums I_f in shunt. Ideal Current Amplifier (I_o / I_s). Low R_inf, High R_of.
- System Design Selection: Choice of topology depends entirely on source impedance R_s and load impedance R_L requirements.

Two-Port Network Representations of Feedback Networks

- Purpose of Two-Port Formulation: Practical feedback networks are 2-port resistive networks. Two-port analysis decouples forward transfer from feedback loading effects.
- Voltage-Series (h-parameters): Hybrid matrix where V_1 = h_11 *I_1 + h_12* V_2 and I_2 = h_21 *I_1 + h_22* V_2. Feedback factor beta = h_12 = (V_1 / V_2) —_{I_1=0}.
- Current-Series (z-parameters): Impedance matrix V_1 = z_11 *I_1 + z_12* I_2 and V_2 = z_21 *I_1 + z_22* I_2. Feedback factor beta = z_12 = (V_1 / I_2) —_{I_1=0}.
- Voltage-Shunt (y-parameters): Admittance matrix I_1 = y_11 *V_1 + y_12* V_2 and I_2 = y_21 *V_1 + y_22* V_2. Feedback factor beta = y_12 = (I_1 / V_2) —_{V_1=0}.
- Current-Shunt (g-parameters): Inverse hybrid matrix I_1 = g_11 *V_1 + g_12* I_2 and V_2 = g_21 *V_1 + g_22* I_2. Feedback factor beta = g_12 = (I_1 / I_2) —_{V_1=0}.

Feedback Network Loading Analysis: r_11 and r_22 Resistances

- Concept of Loaded Open-Loop Circuit: Real feedback networks load both the amplifier input and output nodes. We construct a basic amplifier WITHOUT feedback (A') by incorporating loading resistances r_11 and r_22.
- Input Loading Resistance (r_11): Resistance looking into port 1 of feedback network with port 2 properly terminated:
- For Voltage Output (V_o sampled): Port 2 is SHORT-CIRCUITED (V_2 = 0). r_11 = Input resistance looking into feedback network with output shorted.
- For Current Output (I_o sampled): Port 2 is OPEN-CIRCUITED (I_2 = 0). r_11 = Input resistance looking into feedback network with output open.
- Output Loading Resistance (r_22): Resistance looking into port 2 of feedback network with port 1 properly terminated:
- For Series Input (V_f mixed): Port 1 is OPEN-CIRCUITED (I_1 = 0). r_22 = Output resistance looking into feedback network with input open.
- For Shunt Input (I_f mixed): Port 1 is SHORT-CIRCUITED (V_1 = 0). r_22 = Output resistance looking into feedback network with input shorted.

Systematic 5-Step Algorithm for Analyzing Feedback Amplifiers

- Step 1 (Identify Topology): Determine if output sampling is Voltage or Current, and if input mixing is Series or Shunt. Identify the 4 basic topologies.
- Step 2 (Determine Feedback Factor beta): Find beta = Signal_fed_back / Output_signal (e.g., V_f / V_o, V_f / I_o, I_f / V_o, or I_f / I_o) with input signal set to zero.
- Step 3 (Construct Loaded Open-Loop Circuit A'): Draw basic amplifier without feedback. Include source resistance R_s, load R_L, input loading r_11, and output loading r_22.
- Step 4 (Calculate Open-Loop Gain A and Loop Gain T): Compute open-loop gain A = Output / Input of the loaded circuit. Compute loop gain T = A * beta.
- Step 5 (Compute Closed-Loop Parameters): Calculate closed-loop gain A_f = A / (1 + A * beta), closed-loop input resistance R_inf, and closed-loop output resistance R_of.

Voltage-Series (Series-Shunt) Topology Formulation

- Signal Variables: Source voltage V_s, feedback voltage V_f, error voltage V_i = V_s - V_f, output voltage V_o.
- Feedback Factor: beta_v = (V_f / V_o) —_{I_1=0} (dimensionless ratio).
- Loading Resistances: r_11 = h_11 = (V_1 / I_1) —_{V_2=0} (Port 2 shorted); r_22 = 1 / h_22 = (V_2 / I_2) —_{I_1=0} (Port 1 open).
- Loaded Open-Loop Circuit (A_v): Basic amplifier voltage gain including loading: A_v = (V_o / V_i)—_{loaded}. Input resistance R_in = R_s + r_11 + r_pi; Output resistance R_o = R_C —— r_22 —— R_L.
- Closed-Loop Gain: A_vf = V_o / V_s = A_v / (1 + A_v * beta_v).
- Closed-Loop Resistances: Input resistance R_inf = R_in *(1 + A_v* beta_v); Output resistance R_of = R_o / (1 + A_v * beta_v).

Current-Series (Series-Series) Topology Formulation

- Signal Variables: Source voltage V_s, feedback voltage V_f, error voltage V_i = V_s - V_f, output current I_o.
- Feedback Factor: beta_z = (V_f / I_o) —_{I_1=0} (has units of Ohms, Ohms = V / A).
- Loading Resistances: r_11 = z_11 = (V_1 / I_1) —_{I_2=0} (Port 2 open); r_22 = z_22 = (V_2 / I_2) —_{I_1=0} (Port 1 open).
- Loaded Open-Loop Transconductance Gain (A_m): A_m = (I_o / V_i)—_{loaded} (has units of Siemens, A / V).
- Loop Gain Product: T = A_m * beta_z (dimensionless, Siemens x Ohms = 1).
- Closed-Loop Parameters: Transconductance A_mf = A_m / (1 + A_m *beta_z). Voltage gain A_vf = V_o / V_s = -A_mf* R_L.
- Closed-Loop Resistances: Input resistance R_inf = R_in *(1 + A_m* beta_z); Output resistance R_of = R_o *(1 + A_m* beta_z).

Voltage-Shunt & Current-Shunt Formulations

- Voltage-Shunt Topology (Shunt-Shunt):
- Feedback factor beta_g = I_f / V_o (Siemens, A/V). Open-loop transresistance A_r = V_o / I_i (Ohms, V/A). Loop gain T = A_r * beta_g.
- Closed-Loop Gain: A_rf = A_r / (1 + A_r * beta_g). Voltage gain A_vf = V_o / V_s = -A_rf / R_s.
- Resistances: BOTH input and output resistances DECREASE: R_inf = R_in / (1 + A_r *beta_g)*, *R_of = R_o / (1 + A_r* beta_g).
- Current-Shunt Topology (Shunt-Series):
- Feedback factor beta_i = I_f / I_o (dimensionless current ratio). Open-loop current gain A_i = I_o / I_i (dimensionless).
- Closed-Loop Current Gain: A_if = A_i / (1 + A_i * beta_i).
- Resistances: Input resistance DECREASES, Output resistance INCREASES: R_inf = R_in / (1 + A_i *beta_i)*, *R_of = R_o* (1 + A_i * beta_i).

Step-by-Step Analysis: Voltage-Series BJT Feedback Stage

- Circuit Parameters: Two-stage BJT amplifier with feedback resistor R_F = 10 kOhm from Stage 2 emitter to Stage 1 emitter. R_E1 = 100 Ohm, R_C1 = 4 kOhm, R_C2 = 2 kOhm, r_pi1 = r_pi2 = 1 kOhm, h_fe1 = h_fe2 = 100.
- Step 1 (Topology): Output voltage V_o is sampled at Stage 2 collector/emitter node; feedback voltage V_f across R_E1 is in series with Stage 1 base-emitter input =¿ Voltage-Series Feedback.
- Step 2 (Feedback Factor beta_v): beta_v = V_f / V_o = R_E1 / (R_E1 + R_F) = 100 / (100 + 10,000) = 0.0099 approx 0.01.
- Step 3 (Loading Resistances): r_11 (output shorted) = R_E1 —— R_F = 100 —— 10,000 approx 99 Ohm.
- r_22 (input open) = R_E1 + R_F = 100 + 10,000 = 10.1 kOhm.
- Step 4 (Open-Loop Gain A_v): Loaded first stage gain A_v1 = -h_fe1 *R_C1 / (r_pi1 + (1+h_fe1)*r_11) = -100 *4k / (1k + 101*99) = -36.3.
- Loaded second stage gain A_v2 = -h_fe2 *(R_C2 —— r_22) / r_pi2 = -100* (2k —— 10.1k) / 1k = -165.3.
- Total Open-Loop Gain A_v = A_v1 *A_v2 = (-36.3)* (-165.3) = +6000 (75.56 dB).
- Step 5 (Closed-Loop Gain A_vf): A_vf = A_v / (1 + A_v *beta_v) = 6000 / (1 + 6000* 0.01) = 6000 / 61 = 98.36 (39.85 dB).

Step-by-Step Analysis: Current-Series Transconductance Stage

- Circuit Parameters: Single-stage BJT Common-Emitter amplifier with unbypassed emitter resistor R_E = 500 Ohm. Transistor parameters: g_m = 40 mS, r_pi = 2.5 kOhm, R_C = 5 kOhm, R_s = 1 kOhm.
- Step 1 (Topology): Output current I_c is sampled through emitter loop; feedback voltage V_f = I_e * R_E is in series with base input =¿ Current-Series Feedback.
- Step 2 (Feedback Impedance beta_z): V_f = I_o * R_E =¿ beta_z = V_f / I_o = R_E = 500 Ohm.
- Step 3 (Loading Resistances): Output open (I_o = 0) =¿ r_11 = R_E = 500 Ohm; Input open (I_i = 0) =¿ r_22 = R_E = 500 Ohm.
- Step 4 (Open-Loop Transconductance A_m): Loaded open-loop transconductance (without feedback loop): A_m = I_o / V_i = g_m = 40 mS.
- Loop Gain T: T = A_m *beta_z = 40 mS* 500 Ohm = 20.
- Step 5 (Closed-Loop Parameters): Closed-loop transconductance A_mf = A_m / (1 + T) = 40 mS / (1 + 20) = 1.905 mS.
- Closed-Loop Voltage Gain: A_vf = -A_mf *R_C = -1.905 mS* 5 kOhm = -9.525. (Note: -R_C / R_E = -5000 / 500 = -10!).
- Input Resistance Transformation: R_inf = (R_s + r_pi) *(1 + T) = (1k + 2.5k)* (1 + 20) = 3.5 kOhm * 21 = 73.5 kOhm!

Comprehensive Summary & Two-Port Matrix Overview

- Feedback Topologies Summary:
- 1. Voltage-Series: beta_v = V_f / V_o, R_inf = R_in *(1 + A_v* beta_v), R_of = R_o / (1 + A_v * beta_v) [Voltage Amp].
- 2. Current-Series: beta_z = V_f / I_o, R_inf = R_in *(1 + A_m* beta_z), R_of = R_o *(1 + A_m* beta_z) [Transconductance Amp].
- 3. Voltage-Shunt: beta_g = I_f / V_o, R_inf = R_in / (1 + A_r *beta_g), R_of = R_o / (1 + A_r* beta_g) [Transresistance Amp].
- 4. Current-Shunt: beta_i = I_f / I_o, R_inf = R_in / (1 + A_i *beta_i), R_of = R_o* (1 + A_i * beta_i) [Current Amp].
- Two-Port Rule: Input series mixing INCREASES R_in; Input shunt mixing DECREASES R_in. Voltage output sampling DECREASES R_out; Current output sampling INCREASES R_out.
- Methodology: Always execute the systematic 5-step algorithm incorporating r_11 and r_22 loading resistances.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Outline

- 1. Topological Taxonomy: Classification by Output Sampling (Voltage/Current) and Input Mixing (Series/Shunt)
- 2. Voltage-Series (Series-Shunt) Feedback: BJT Two-Stage Feedback Pair Schematics and Op-Amp Non-Inverting Stage
- 3. Current-Series (Series-Series) Feedback: Single-Stage CE/CS Unbypassed Emitter/Source Resistor Stage
- 4. Voltage-Shunt (Shunt-Shunt) Feedback: BJT Collector-to-Base Feedback Resistor and Op-Amp Inverting Amplifier
- 5. Current-Shunt (Shunt-Series) Feedback: Two-Stage BJT Current Amplifier Circuit Configuration
- 6. Step-by-Step Worked Engineering Examples and Comprehensive Topological Comparison Matrix

Formal Taxonomy of the Four Feedback Topologies

- Classification Basis: Feedback circuits are classified according to the physical quantity sampled at the output node (Voltage or Current) and the physical quantity summed at the input node (Series Voltage or Shunt Current).
- 1. Voltage-Series (Series-Shunt): Output Voltage V_o sampled in parallel; Feedback Voltage V_f summed in series with input source V_s.
- 2. Current-Series (Series-Series): Output Current I_o sampled in series; Feedback Voltage V_f summed in series with input source V_s.
- 3. Voltage-Shunt (Shunt-Shunt): Output Voltage V_o sampled in parallel; Feedback Current I_f summed in parallel (shunt) with input source I_s.
- 4. Current-Shunt (Shunt-Series): Output Current I_o sampled in series; Feedback Current I_f summed in parallel (shunt) with input source I_s.
- Source & Load Characterization: Series input requires voltage source (low R_s); Shunt input requires current source (high R_s). Voltage output drives high load R_L; Current output drives low load R_L.

Voltage-Series (Series-Shunt) Topology & Impedance Effects

- Circuit Mechanics: Voltage sampler measures output voltage V_o across load R_L; Feedback network presents attenuation beta_v = V_f / V_o; Series summer subtracts feedback voltage V_f from input voltage V_s.
- Ideal Amplifier Equivalent: Acts as an ideal Voltage Amplifier (Voltage-Controlled Voltage Source, VCVS).
- Transfer Gain Metric: Closed-loop voltage gain A_vf = V_o / V_s = A_v / (1 + A_v * beta_v).
- Asymptotic Limit: When open-loop loop gain A_v * beta_v ¿¿ 1, closed-loop gain A_vf approx 1 / beta_v.
- Input Impedance Transformation: Series input mixing boosts input resistance: R_inf = R_in *(1 + A_v* beta_v)*. Prevents loading on high-impedance voltage sources.
- Output Impedance Transformation: Voltage output sampling lowers output resistance: R_of = R_o / (1 + A_v * beta_v). Delivers stiff, load-independent output voltage.

Discrete BJT Voltage-Series Feedback Pair Circuit Analysis

- Circuit Configuration: Two-stage cascaded Common-Emitter (CE) BJT amplifier. Feedback resistor R_F is connected from Stage 2 emitter node to Stage 1 emitter node.
- AC Signal Flow: Output voltage V_o at Stage 2 collector causes AC current through R_F into Stage 1 emitter resistor R_E1, producing feedback voltage V_f = V_o * [R_E1 / (R_E1 + R_F)] across R_E1.
- Input Summer Operation: Input voltage V_s is applied to Stage 1 base. Base-emitter signal voltage is V_be1 = V_s - V_f (Series Voltage Summing).
- Feedback Ratio Formulation: beta_v = V_f / V_o = R_E1 / (R_E1 + R_F).
- Loading Resistances Incorporation: r_11 = R_E1 —— R_F added in series with Stage 1 emitter; r_22 = R_E1 + R_F added in parallel with Stage 2 collector load.
- Closed-Loop Voltage Gain: A_vf = V_o / V_s approx (R_E1 + R_F) / R_E1 = 1 + R_F / R_E1.

Current-Series (Series-Series) Topology & Transconductance

- Circuit Mechanics: Current sampler senses output current I_o flowing through load R_L; Feedback network generates feedback voltage V_f = beta_z * I_o; Series summer subtracts V_f from input V_s.
- Ideal Amplifier Equivalent: Acts as an ideal Transconductance Amplifier (Voltage-Controlled Current Source, VCCS).
- Transfer Gain Metric: Open-loop transconductance A_m = I_o / V_i (Siemens); Feedback factor beta_z = V_f / I_o (Ohms). Loop gain T = A_m * beta_z.
- Closed-Loop Transconductance: A_mf = I_o / V_s = A_m / (1 + A_m *beta_z). Closed-loop voltage gain A_vf = V_o / V_s = -A_mf* R_L.
- Input Impedance Transformation: Series input mixing boosts input resistance: R_inf = R_in *(1 + A_m* beta_z).
- Output Impedance Transformation: Current output sampling boosts output resistance: R_of = R_o *(1 + A_m* beta_z). Delivers stiff, load-independent output current.

Discrete Current-Series Circuit: Unbypassed Emitter/Source Resistor

- Single-Stage CE Circuit Configuration: BJT Common-Emitter amplifier with emitter resistor R_E left UNBYPASSED (no parallel bypass capacitor C_E).
- AC Signal Mechanics: Collector current I_c approx I_e flows through unbypassed resistor R_E, generating feedback voltage V_f = I_o * R_E directly in series with base input voltage V_s.
- Feedback Impedance Value: beta_z = V_f / I_o = R_E (Ohms).
- Loaded Transconductance (A_m): For basic CE transistor without feedback, A_m = g_m. Loop gain T = g_m * R_E.
- Closed-Loop Transconductance: A_mf = g_m / (1 + g_m * R_E).
- Closed-Loop Voltage Gain Derivation: A_vf = -A_mf R_C = -[g_m / (1 + g_m R_E)] R_C. If g_m R_E ¿¿ 1, then A_vf approx -R_C / R_E!
- FET Source Follower Variant: CS MOSFET with unbypassed source resistor R_S yields feedback factor beta_z = R_S and A_vf approx -R_D / R_S.

Voltage-Shunt (Shunt-Shunt) Topology & Transresistance

- Circuit Mechanics: Voltage sampler measures output voltage V_o across load R_L; Feedback network generates feedback current I_f = beta_g * V_o; Shunt summer subtracts I_f from input current source I_s.
- Ideal Amplifier Equivalent: Acts as an ideal Transresistance Amplifier (Current-Controlled Voltage Source, CCVS).
- Transfer Gain Metric: Open-loop transresistance A_r = V_o / I_i (Ohms); Feedback factor beta_g = I_f / V_o (Siemens). Loop gain T = A_r * beta_g.
- Closed-Loop Transresistance: A_rf = V_o / I_s = A_r / (1 + A_r * beta_g). Closed-loop voltage gain from source V_s (via R_s): A_vf = V_o / V_s = -A_rf / R_s.
- Input Impedance Transformation: Shunt input mixing lowers input resistance: R_inf = R_in / (1 + A_r * beta_g). Creates virtual ground at input node.
- Output Impedance Transformation: Voltage output sampling lowers output resistance: R_of = R_o / (1 + A_r * beta_g).

Discrete Voltage-Shunt Circuit: Collector-to-Base Feedback Resistor

- Circuit Configuration: Single-stage Common-Emitter BJT amplifier with a feedback resistor R_F connected directly between collector (output node) and base (input node).
- AC Signal Mechanics: Output voltage V_o at collector drives AC feedback current I_f = (V_o - V_b) / R_F approx V_o / R_F into base input node, subtracting from signal current I_s.
- Feedback Admittance Value: beta_g = I_f / V_o = -1 / R_F (Siemens).
- Loaded Open-Loop Transresistance (A_r): A_r = V_o / I_i = -g_m *(R_C —— r_pi —— R_F)* r_pi.
- Closed-Loop Transresistance Asymptote: When loop gain —A_r * beta_g— ¿¿ 1, closed-loop transresistance A_rf = V_o / I_s approx 1 / beta_g = -R_F!
- Closed-Loop Voltage Gain (from Voltage Source V_s with R_s): A_vf = V_o / V_s = (V_o / I_s) / R_s = -R_F / R_s.
- Miller Effect Perspective: Resistor R_F appears at input as equivalent parallel resistance R_in,M = R_F / (1 + —A_v—), explaining the drastic drop in R_inf.

Current-Shunt (Shunt-Series) Topology & Current Amplification

- Circuit Mechanics: Current sampler senses output current I_o flowing through load; Feedback network generates feedback current I_f = beta_i * I_o; Shunt summer subtracts I_f from input current I_s.
- Ideal Amplifier Equivalent: Acts as an ideal Current Amplifier (Current-Controlled Current Source, CCCS).
- Transfer Gain Metric: Open-loop current gain A_i = I_o / I_i (dimensionless); Feedback factor beta_i = I_f / I_o (dimensionless). Loop gain T = A_i * beta_i.
- Closed-Loop Current Gain: A_if = I_o / I_s = A_i / (1 + A_i * beta_i). Asymptote for large loop gain: A_if approx 1 / beta_i.
- Input Impedance Transformation: Shunt input mixing lowers input resistance: R_inf = R_in / (1 + A_i * beta_i). Ideal for low-impedance current inputs.
- Output Impedance Transformation: Current output sampling boosts output resistance: R_of = R_o *(1 + A_i* beta_i). Ideal for driving low-impedance current loads.

Discrete BJT Current-Shunt Circuit: Two-Stage Current Pair

- Circuit Configuration: Two-stage BJT amplifier. Feedback resistor R_F is connected from Stage 2 emitter to Stage 1 base input node. Emitter resistor R_E2 is unbypassed.
- AC Signal Flow: Stage 2 AC emitter current I_e2 approx I_o flows through R_E2, generating AC voltage V_e2 = I_o * R_E2. This drives feedback current I_f = V_e2 / R_F into Stage 1 base node.
- Feedback Ratio Formulation: beta_i = I_f / I_o = [I_o * R_E2 / (R_E2 + R_F)] / I_o = R_E2 / (R_E2 + R_F).
- Closed-Loop Current Gain Asymptote: A_if = I_o / I_s approx 1 / beta_i = (R_E2 + R_F) / R_E2 = 1 + R_F / R_E2.
- Application in Photodiode Preamps: Used to amplify low-level photocurrents from sensors while maintaining low input impedance to prevent RC speed degradation.

Comprehensive Op-Amp Non-Inverting Voltage-Series Analysis

- Circuit Configuration: Op-amp with input signal V_s applied to non-inverting (+) terminal. Feedback voltage divider (R_1, R_2) connected from output V_o to inverting (-) terminal.
- Step 1 (Topology Identification): Output voltage V_o is sampled; feedback voltage V_f = V_o * [R_1 / (R_1 + R_2)] is subtracted at differential input (V_+ - V_-) =¿ Voltage-Series Feedback.
- Step 2 (Feedback Factor beta_v): beta_v = V_f / V_o = R_1 / (R_1 + R_2).
- Step 3 (Open-Loop Parameters): Ideal op-amp has open-loop voltage gain A_OL = 10^5 (100 dB), differential input resistance R_in = 2 M-Ohm, output resistance R_o = 75 Ohm.
- Step 4 (Closed-Loop Gain A_vf): Given R_1 = 1 k-Ohm, R_2 = 9 k-Ohm =¿ beta_v = 1k / (1k + 9k) = 0.1.
- Loop Gain T = A_OL *beta_v = 10^5* 0.1 = 10,000 (80 dB).
- A_vf = A_OL / (1 + T) = 10^5 / 10,001 = 9.999 (exact 1 / beta_v = 10!).
- Step 5 (Transformed Impedances): Closed-loop input resistance R_inf = 2 M-Ohm * (1 + 10,000) = 20.002 Giga-Ohms!
- Closed-loop output resistance R_of = 75 Ohm / (1 + 10,000) = 0.0075 Ohms (7.5 milli-Ohms)!

Comprehensive Op-Amp Inverting Voltage-Shunt Analysis

- Circuit Configuration: Op-amp with non-inverting (+) terminal grounded. Input source V_s connected through R_1 to inverting (-) terminal. Feedback resistor R_F connected from output V_o to (-) terminal.
- Step 1 (Topology Identification): Output voltage V_o sampled; feedback current I_f = (V_o - V_-) / R_F summed in parallel with input current I_in = (V_s - V_-) / R_1 at inverting node =¿ Voltage-Shunt Feedback.
- Step 2 (Virtual Ground Concept): High loop gain forces differential voltage (V_+ - V_-) -¿ 0. Since V_+ = 0V, inverting terminal V_- is held at Virtual Ground (0V).
- Step 3 (Nodal Current Equilibrium): Summing AC currents at inverting node: I_in + I_f = 0 =¿ (V_s - 0) / R_1 + (V_o - 0) / R_F = 0.
- Step 4 (Closed-Loop Voltage Gain Derivation): V_o / R_F = -V_s / R_1 =¿ A_vf = V_o / V_s = -R_F / R_1.
- Step 5 (Closed-Loop Input Impedance): Looking into input terminal past R_1: Resistance at inverting node R_in,node = R_in / (1 + A_OL * beta_g) approx 0 Ohm. Therefore, total input resistance seen by source is R_inf = R_1 + 0 = R_1.

Summary & Topological Comparison Matrix

- Comprehensive Feedback Comparison Matrix:
- 1. Voltage-Series: Samples V_o, Sums V_f Series — A_vf approx 1 / beta_v — R_inf = R_in(1+T) [HIGH] — R_of = R_o/(1+T) [LOW]. Circuit: Op-Amp Non-Inverting, BJT 2-stage voltage pair.
- 2. Current-Series: Samples I_o, Sums V_f Series — A_mf approx 1 / beta_z — R_inf = R_in(1+T) [HIGH] — R_of = R_o(1+T) [HIGH]. Circuit: Unbypassed R_E / R_S stage.
- 3. Voltage-Shunt: Samples V_o, Sums I_f Shunt — A_rf approx 1 / beta_g — R_inf = R_in/(1+T) [LOW] — R_of = R_o/(1+T) [LOW]. Circuit: Op-Amp Inverting, Collector-Base R_F.
- 4. Current-Shunt: Samples I_o, Sums I_f Shunt — A_if approx 1 / beta_i — R_inf = R_in/(1+T) [LOW] — R_of = R_o(1+T) [HIGH]. Circuit: BJT 2-stage current pair.
- Design Rule: Select Voltage sampling to deliver stable voltage; Current sampling for stable current. Select Series mixing for high input impedance; Shunt mixing for low input impedance.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Outline

- 1. Mathematical Proofs: Derivation of Input Impedance for Series (KVL) and Shunt (KCL) Mixing
- 2. Mathematical Proofs: Derivation of Output Impedance for Voltage and Current Sampling using Test Sources
- 3. High-Frequency Pole Movement: Root-Locus and Q-factor Dynamics in Multi-Pole Feedback Amplifiers
- 4. Stability Metrics: Gain Margin (GM) and Phase Margin (PM) Criteria on Nyquist and Bode Plots
- 5. Frequency Compensation: Dominant Pole Placement, Lag Compensation, and Miller Pole-Splitting Mechanics
- 6. Engineering Design Examples: Multi-Stage Feedback Calculations and Miller Compensation Design

Mathematical Proof of Input Impedance Transformation

- Proof 1: Series Input Mixing (Voltage Comparison):
- Input Circuit Equations: Apply Kirchhoff's Voltage Law at input loop: V_s = V_i + V_f. Substitute V_f = beta $V_o = beta$ (A * V_i).
- Substituting V_f: V_s = V_i + A $beta$ V_i = V_i $(1 + A$ beta).
- Input Current Equation: I_i = V_i / R_in (where R_in is open-loop input resistance).
- Closed-Loop Resistance Derivation: R_inf = V_s / I_i = [V_i $(1 + A$ beta)] / (V_i / R_in) = R_in $(1 + A$ beta). PROVED!
- Proof 2: Shunt Input Mixing (Current Comparison):
- Apply Kirchhoff's Current Law at input node: I_s = I_i + I_f. Substitute I_f = beta $I_o = beta$ (A * I_i).
- Substituting I_f: I_s = I_i + A $beta$ I_i = I_i $(1 + A$ beta).
- Input Voltage Equation: V_i = I_i * R_in.
- Closed-Loop Resistance Derivation: R_inf = V_i / I_s = (I_i $R_in) / [I_i$ (1 + A $beta)] = R_in /$ $(1 + A$ beta). PROVED!

Mathematical Proof of Output Impedance Transformation

- Proof Method: Deactivate input signal source (set V_s = 0 or I_s = 0), apply an external test voltage V_x at output terminals, measure resulting current I_x. R_of = V_x / I_x.
- Proof 1: Voltage Output Sampling (Shunt Output):
- For set V_s = 0 and applied V_x: Feedback voltage V_f = beta *V_x. Series input gives error V_i = 0 - V_f = -beta* V_x.
- Internal Amplifier Current: Dependent source generates current g_m *V_i = -A* V_x / R_o.
- KCL at Output Node: I_x = (V_x / R_o) - (internal source current) = (V_x / R_o) - (-A *beta* V_x / R_o) = (V_x / R_o) *(1 + A* beta).
- Closed-Loop Output Resistance: R_of = V_x / I_x = R_o / (1 + A * beta). PROVED!
- Proof 2: Current Output Sampling (Series Output):
- Applying test current I_x through output loop with V_s = 0 gives V_f = beta *I_x =¿ V_i = -beta* I_x.
- KVL around Output Loop: V_x = I_x *R_o - A* V_i = I_x *R_o - A* (-beta *I_x) = I_x* R_o *(1 + A* beta).
- Closed-Loop Output Resistance: R_of = V_x / I_x = R_o *(1 + A* beta). PROVED!

Summary & Matrix of Impedance Transformation Rules

- Master Impedance Matrix:
- Topology 1 (Voltage-Series): Series Input -¿ R_inf = R_in *(1 + A_v* beta_v); Voltage Output -¿ R_of = R_o / (1 + A_v * beta_v).
- Topology 2 (Current-Series): Series Input -¿ R_inf = R_in *(1 + A_m* beta_z); Current Output -¿ R_of = R_o *(1 + A_m* beta_z).
- Topology 3 (Voltage-Shunt): Shunt Input -¿ R_inf = R_in / (1 + A_r *beta_g); Voltage Output -¿ R_of = R_o / (1 + A_r* beta_g).
- Topology 4 (Current-Shunt): Shunt Input -¿ R_inf = R_in / (1 + A_i *beta_i); Current Output -¿ R_of = R_o* (1 + A_i * beta_i).
- Signal Conditioning Matching:
- Voltage Source -¿ Requires Voltage-Series or Current-Series (High R_in).
- Current Source -¿ Requires Voltage-Shunt or Current-Shunt (Low R_in).
- Voltage Load -¿ Requires Voltage-Series or Voltage-Shunt (Low R_out).
- Current Load -¿ Requires Current-Series or Current-Shunt (High R_out).

Frequency Response Dynamics & Pole Movement under Feedback

- Single-Pole System Root Locus: Open-loop transfer function A(s) = A_0 / (1 + s / omega_p).
- Closed-Loop Transfer Function: A_f(s) = [A_0 / (1 + s / omega_p)] / [1 + beta *A_0 / (1 + s / omega_p)] = [A_0 / (1 + A_0* beta)] / [1 + s / (omega_p *(1 + A_0* beta))].
- Pole Trajectory: The real pole moves along the negative real axis from s = -omega_p to s = -omega_pf = -omega_p *(1 + A_0* beta). System remains UNCONDITIONALLY STABLE for any amount of feedback!
- Two-Pole System Dynamics: Open-loop transfer function A(s) = A_0 / [(1 + s / omega_p1) * (1 + s / omega_p2)].
- Complex Conjugate Pole Pair: As feedback factor beta increases, the two real poles move toward each other, collide on the real axis, and break out into complex conjugate poles: s_1,2 = -sigma +/- j * omega_d.
- Peaking & Over-Shoot: Complex poles induce high-frequency gain peaking in frequency response and transient ringing in step response if quality factor Q = sqrt(1 + A_0 * beta) / (1 + omega_p1 / omega_p2) ¿ 0.707.

Multi-Pole Instability & High-Frequency Phase Shift Mechanics

- Three-Pole System Instability: Open-loop transfer function A(s) = A_0 / [(1 + s / omega_p1) *(1 + s / omega_p2)* (1 + s / omega_p3)].
- Phase Accumulation: Each pole contributes up to -90 degrees of phase shift at high frequencies. A 3-pole system accumulates up to -270 degrees of phase lag.
- Phase Crossover Frequency (omega_180): Frequency where total phase shift reaches -180 degrees: angle(A(j *omega_180)* beta) = -180 deg.
- Positive Feedback Transformation: At omega_180, e^(-j *180 deg) = -1. The denominator (1 + A* beta) becomes (1 - —A * beta—). Negative feedback transforms into POSITIVE FEEDBACK!
- Barkhausen Runaway Condition: If loop gain magnitude —A(j *omega_180)* beta— ¿= 1 (0 dB), the system undergoes self-sustained spontaneous oscillation.

Gain Margin (GM) and Phase Margin (PM) Stability Criteria

- Bode Plot Stability Evaluation: Plot 20 *log10(—A* beta—) and phase angle(A * beta) versus logarithmic frequency.
- Gain Crossover Frequency (f_c): Defined where —A(j *2* pi *f_c)* beta— = 1 (0 dB).
- Phase Crossover Frequency (f_180): Defined where angle(A(j *2* pi *f_180)* beta) = -180 deg.
- Phase Margin Formula: PM = 180 deg + angle(A(j *2* pi *f_c)* beta).
- PM Target Values: PM ¿ 0 deg for stability; PM ¿= 45 deg for acceptable transient response; PM = 60 deg for maximally flat Butterworth response (zero peaking).
- Gain Margin Formula: GM = -20 *log10(—A(j* 2 *pi* f_180) * beta—). Target: GM ¿= 6 dB - 10 dB.

Frequency Compensation: Dominant Pole & Miller Pole Splitting

- Need for Frequency Compensation: High-gain multistage op-amps have multiple poles, leading to PM ¡ 0 (unstable). Frequency compensation alters loop response to force —A * beta— ¡ 1 before phase reaches -180 degrees.
- Dominant Pole Compensation: Adding a large capacitor C_D across an internal high-resistance node pulls the first pole down to a very low frequency f_p1' ¡¡ f_p1.
- Drawback of Simple Dominant Pole: Drastically reduces open-loop bandwidth and limits amplifier Slew Rate (SR = dV/dt).
- Miller Compensation (Pole Splitting): Connecting a small compensation capacitor C_C across the high-gain inverting stage (Stage 2).
- Miller Pole-Splitting Action:
- 1. Dominant pole f_p1 is pulled LOW to f_p1' approx 1 / [2 *pi* (g_m2 *R_1* R_2 * C_C)] via Miller input capacitance multiplication.
- 2. Non-dominant pole f_p2 is pushed HIGH to f_p2' approx g_m2 / [2 *pi* (C_1 + C_2)] via negative feedback around Stage 2!
- Result: Widely separates poles, ensuring 20 dB/decade roll-off through gain crossover frequency and achieving PM approx 60 - 90 degrees!

Effect of Feedback on Noise & Internal Interference

- Noise Source Classification: Input-referred noise V_ni (from sensors/first stage) vs Internal stage noise V_n2 (from power supply ripple, second stage drivers).
- Signal-to-Noise Ratio (SNR) Equation: Output signal V_o = A_1 *A_2* V_s; Output noise from stage 2 V_on = A_2 * V_n2.
- Closed-Loop SNR Transformation: With feedback factor beta applied around overall system:
- V_of = (A_1 *A_2* V_s) / (1 + A_1 *A_2* beta), and V_onf = (A_2 *V_n2) / (1 + A_1* A_2 * beta).
- System SNR with Feedback: SNR_f = V_of / V_onf = (A_1 *A_2* V_s) / (A_2 *V_n2) = A_1* (V_s / V_n2).
- Noise Suppression Conclusion: Negative feedback dramatically suppresses internal noise V_n2 injected AFTER high-gain stage A_1. However, noise V_ni present at the primary input is amplified along with the signal!

Design Example 1: Multi-Stage Feedback Impedance Analysis

- Problem Statement: A two-stage BJT Series-Shunt (Voltage-Series) feedback amplifier has open-loop voltage gain A_v = 2,000 (66 dB), open-loop input resistance R_in = 4 k-Ohm, open-loop output resistance R_o = 8 k-Ohm. The feedback factor is beta_v = 0.025.
- Step 1: Calculate Loop Gain T: T = A_v $\times$ *beta_v = 2,000* $\times$ 0.025 = 50 (33.98 dB).
- Step 2: Calculate Amount of Feedback F: F = 1 + T = 1 + 50 = 51 (34.15 dB).
- Step 3: Calculate Closed-Loop Gain A_vf: A_vf = A_v / (1 + T) = 2,000 / 51 = 39.215 (31.87 dB). (Note: Asymptotic 1 / beta_v = 1 / 0.025 = 40!).
- Step 4: Calculate Closed-Loop Input Resistance R_inf: Series input mixing boosts input resistance: R_inf = R_in $\times$ *(1 + T) = 4 k-Ohm* $\times$ 51 = 204 k-Ohm!
- Step 5: Calculate Closed-Loop Output Resistance R_of: Voltage output sampling lowers output resistance: R_of = R_o / (1 + T) = 8,000 Ohm / 51 = 156.86 Ohms!
- Conclusion: Feedback boosted input resistance from 4 k-Ohm to 204 k-Ohm, and dropped output resistance from 8 k-Ohm to 156.86 Ohms.

Design Example 2: Miller Compensation & Phase Margin Calculation

- Problem Statement: An uncompensated op-amp has open-loop gain A_0 = 10^5, primary pole f_p1 = 100 Hz, secondary pole f_p2 = 1 MHz, and tertiary pole f_p3 = 10 MHz. Calculate Phase Margin with beta = 0.1, and design Miller capacitor C_C for PM = 60 deg.
- Step 1: Uncompensated Phase Margin at Gain Crossover: Loop gain T(0) = 10^5 *0.1 = 10^4 (80 dB). Uncompensated crossover frequency f_c approx 100 Hz* 10^4 = 1 MHz.
- At f_c = 1 MHz: Phase lag angle(T) = -arctan(1M / 100) - arctan(1M / 1M) - arctan(1M / 10M) = -90 deg - 45 deg - 5.7 deg = -140.7 deg.
- Uncompensated Phase Margin: PM = 180 deg - 140.7 deg = 39.3 deg (Inadequate! Target PM ¿= 60 deg).
- Step 2: Miller Pole-Splitting Design for PM = 60 deg: For PM = 60 deg, new gain crossover f_c' must equal non-dominant pole f_p2' = 1 MHz.
- Required New Dominant Pole f_p1': f_c' = f_p1' *T(0) =¿ 1 MHz = f_p1'* 10^4 =¿ f_p1' = 100 Hz / 10 = 10 Hz.
- Step 3: Calculating Miller Capacitor C_C: Given stage 1 output resistance R_1 = 1 M-Ohm and stage 2 transconductance g_m2 = 5 mS:
- f_p1' = 1 / [2 *pi* g_m2 *R_1* R_2 *C_C] =¿ C_C = 1 / [2* pi *5mS* 1M-Ohm *10k-Ohm* 10Hz] = 3.18 pF.

Multi-Variable Design Trade-offs: Gain vs Bandwidth vs Stability

- 1. Voltage Gain vs Bandwidth Trade-Off: Increasing feedback factor beta lowers closed-loop voltage gain A_f, but expands system bandwidth f_Hf = f_H *(1 + A_0* beta) proportionally.
- 2. Gain Margin / Phase Margin vs Loop Gain Trade-Off: High loop gain T = A * beta provides superior gain desensitization and distortion reduction, but pushes multi-pole systems toward phase crossover, degrading Phase Margin.
- 3. Input/Output Impedance Matching: Series input boosts R_in (ideal for voltage sensing); Shunt input lowers R_in (ideal for current sensing). Voltage sampling lowers R_out; Current sampling boosts R_out.
- 4. Power & Area Overhead: Miller compensation requires silicon area for capacitor C_C and increases high-frequency power dissipation during large-signal slewing.
- Engineering Synthesis: Active circuit design demands balancing gain requirements, load impedance matching, noise figure, and Phase Margin ¿= 60 degrees.

Unit 4 Comprehensive Summary & Master Takeaways

- Closed-Loop Fundamental Formula: A_f = A / (1 + A *beta). Under heavy feedback (A* beta ¿¿ 1), A_f approx 1 / beta.
- Universal Impedance Modification: All input and output impedances are transformed by factor (1 + Loop Gain) = (1 + A * beta).
- Series Input -¿ R_inf = R_in *(1 + A* beta); Shunt Input -¿ R_inf = R_in / (1 + A * beta).
- Voltage Output -¿ R_of = R_o / (1 + A *beta); Current Output -¿ R_of = R_o* (1 + A * beta).
- Stability Criterion: Stable amplifier operation requires Phase Margin PM ¿= 45 deg (60 deg optimal) and Gain Margin GM ¿= 6 dB.
- Miller Compensation: Uses pole splitting via capacitor C_C to pull primary pole down and push secondary pole up, guaranteeing unconditional stability.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda & Systematic Outline

- System Architecture & Feedback Block Diagram Representation
- Derivation of Closed-Loop Voltage Gain Equation ($A_f = \frac{A}{1+A\beta}$)
- Asymptotic Limits & Feedback Ratio (β) Behavior at High Loop Gain
- Loop Transmission, Return Ratio, and Amount of Feedback in Decibels
- Gain Desensitivity & Fractional Variation Analysis ($\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\frac{dA}{A}$)
- Voltage-Series vs. Voltage-Shunt Topologies Impact on Voltage Gain
- Two-Port *h*-Parameter Modeling of Loaded Feedback Networks
- Non-Inverting Op-Amp Voltage Gain Derivation ($A_{Vf} = 1 + \frac{R_2}{R_1}$)
- Inverting Op-Amp Transresistance to Voltage Gain Conversion ($A_{Vf} = -\frac{R_f}{R_1}$)
- High-Frequency Response & Gain-Bandwidth Constancy ($A_{0f} \cdot \omega_{Hf} = A_0 \cdot \omega_H$)
- Numerical Problem: Gain Variation & Desensitivity Calculation
- Circuit Analysis Example: Discrete BJT Voltage-Series Feedback Amplifier
- Summary & Engineering Synthesis

System Architecture of Feedback Amplifiers

- Basic Block Structure: Consists of an open-loop basic amplifier with gain $A = V_o/V_i$, a passive feedback network with transfer ratio $\beta = V_f/V_o$, and an input summing junction where $V_i = V_s - V_f$.
- Signal Definitions: Source signal V_s, net internal error signal $V_i = V_s - \beta V_o$, output voltage $V_o = A \cdot V_i$, and feedback signal $V_f = \beta V_o$.
- Negative Feedback Phase Condition: Requires feedback signal V_f to subtract from input V_s, establishing a 180° phase shift relative to open-loop output to stabilize total gain.
- Ideal Feedback Assumptions: Basic amplifier is unilateral (A transmits forward only), feedback network is unilateral (β transmits backward only), and β network loading is fully accounted for.

Mathematical Derivation of Closed-Loop Gain (A_f)

- Output Equation Setup: Output voltage expressed in terms of open-loop gain A and net error input V_i: $V_o = AV_i = A(V_s - V_f)$.
- Feedback Substitution: Substituting feedback relationship $V_f = \beta V_o$ yields $V_o = A(V_s - \beta V_o) = AV_s - A\beta V_o$.
- Algebraic Rearrangement: Collecting output terms on the left side: $V_o + A\beta V_o = AV_s \implies V_o(1 + A\beta) = AV_s$.
- Closed-Loop Gain Formula: Dividing by V_s gives closed-loop voltage gain $A_f = \frac{V_o}{V_s} = \frac{A}{1+A\beta}$, where term $(1 + A\beta)$ is the desensitivity factor or amount of feedback.

Asymptotic Limits & Feedback Ratio (β) Behavior

- High Loop Gain Limit ($A\beta \gg 1$): When open-loop gain product $A\beta$ is extremely large ($A\beta \to \infty$), $1 + A\beta \approx A\beta$.
- Asymptotic Closed-Loop Gain: $A_f = \frac{A}{1+A\beta} \approx \frac{A}{A\beta} = \frac{1}{\beta}$. Closed-loop gain depends exclusively on feedback factor β.
- Passive Component Precision: Since β is constructed using stable passive resistors (R_1, R_2), closed-loop gain becomes virtually immune to transistor non-linearities, temperature drift, and manufacturing tolerances.
- Feedback Ratio Bounds: Passive feedback networks constrain $0 < \beta \leq 1$; for a pure unity voltage follower, $\beta = 1$, giving $A_f \approx 1$ V/V.

Loop Gain ($A\beta$), Return Ratio, and Feedback Measurement

- Loop Gain Definition: $T = A\beta$ represents the total voltage transmission around the feedback loop when broken at a specified node.
- Return Ratio Determination: Disconnect feedback path, inject test voltage V_t at break point with source ground $V_s = 0$; returned voltage $V_r = -A\beta V_t$. Return ratio $RR = -V_r/V_t = A\beta$.
- Amount of Feedback in Decibels (N_{dB}): Defined quantitatively as $N_{dB} = 20\log_{10}|1 + A\beta|$.
- Decibel Example: A desensitivity factor $(1 + A\beta) = 100$ corresponds to $20\log_{10}(100) = 40$ dB of feedback, reducing voltage gain by 40 dB while enhancing stability equally.

Gain Desensitivity & Fractional Variation Analysis

- Sensitivity Derivative: Differentiating closed-loop gain $A_f = \frac{A}{1+A\beta}$ with respect to open-loop gain A yields $\frac{dA_f}{dA} = \frac{(1+A\beta)-A\beta}{(1+A\beta)^2} = \frac{1}{(1+A\beta)^2}$.
- Fractional Gain Sensitivity Equation: Expressing relative change: $\frac{dA_f}{A_f} = \frac{dA}{A} \cdot \frac{A}{A_f} \cdot \frac{dA_f}{dA} = \frac{dA}{A} \cdot (1 + A\beta) \cdot \frac{1}{(1+A\beta)^2} = \frac{1}{1+A\beta} \frac{dA}{A}$.
- Desensitivity Factor Signification: Closed-loop gain fractional variation $\frac{dA_f}{A_f}$ is reduced by factor $(1 + A\beta)$ compared to open-loop variation $\frac{dA}{A}$.
- Sensitivity Function $S_A^{A_f}$: Defined as $S_A^{A_f} = \frac{\%\Delta A_f}{\%\Delta A} = \frac{1}{1+A\beta}$, proving that high loop gain renders the system desensitized to internal variations.

Voltage-Series vs. Voltage-Shunt Topology Impact on Gain

- Voltage-Series (Series-Shunt) Topology: Samples output voltage V_o and mixes feedback voltage V_f in series with source V_s. Ideal pure voltage amplifier with closed-loop voltage gain $A_{Vf} = \frac{A_V}{1+\beta_v A_V}$.
- Voltage-Shunt (Shunt-Shunt) Topology: Samples output voltage V_o and mixes feedback current I_f in shunt with source current I_s. Basic amplifier has transresistance gain $R_m = V_o/I_i$.
- Closed-Loop Transresistance (R_{mf}): $R_{mf} = \frac{R_m}{1+\beta_g R_m}$, where $\beta_g = I_f/V_o$ is feedback transconductance in Siemens.
- Terminal Voltage Gain Conversion: For voltage-shunt feedback with source resistance R_s, effective voltage gain $A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{mf}}{R_s} = \frac{R_m/(1+\beta_g R_m)}{R_s}$.

Two-Port Parameter Modeling of Loaded Feedback Networks

- Loading Effect Realization: Practical feedback networks load both input and output ports of the basic amplifier, altering open-loop gain from A to modified open-loop gain A'.
- Two-Port h-Parameter Extraction: For voltage-series feedback, β-network is modeled as an h-parameter two-port block: $h_{11} = Z_{in,\beta}|_{V_o=0}$, $h_{22}^{-1} = Z_{out,\beta}|_{I_i=0}$, $\beta = h_{12} = \left.\frac{V_f}{V_o}\right|_{I_i=0}$.
- Modified Basic Amplifier Construction: Include h_{11} in series with input impedance R_{in} and h_{22}^{-1} in parallel with output load R_L to form modified amplifier A'.
- Loaded Voltage Gain Equation: Compute $A' = \left.\frac{V_o'}{V_i'}\right|_{loaded}$; exact closed-loop gain is then $A_{Vf} = \frac{A'}{1+h_{12}A'}$.

Voltage Gain Analysis of Non-Inverting Op-Amp Amplifier

- Circuit Topology: Input voltage V_s applied to non-inverting terminal ($V_+ = V_s$); feedback voltage divider R_1, R_2 connected between output V_o and inverting terminal ($V_- = V_f$).
- Feedback Factor Calculation: $\beta = \frac{V_f}{V_o} = \frac{R_1}{R_1+R_2}$. Op-amp open-loop voltage gain is A_{OL}.
- Exact Voltage Gain Equation: $A_{Vf} = \frac{A_{OL}}{1+A_{OL}\beta} = \frac{A_{OL}}{1+A_{OL}\frac{R_1}{R_1+R_2}}$.
- Ideal Op-Amp Simplification ($A_{OL} \to \infty$): $A_{Vf} \approx \frac{1}{\beta} = \frac{R_1+R_2}{R_1} = 1 + \frac{R_2}{R_1}$. Voltage gain is completely determined by passive resistor ratios.

Voltage Gain Analysis of Inverting Feedback Amplifier

- Circuit Topology: Non-inverting terminal grounded ($V_+ = 0$ V); input V_s connected via R_1 to virtual ground node V_-; feedback resistor R_f connected from output V_o to V_-.
- Voltage-Shunt Analysis: Operates as voltage-shunt feedback. Transresistance gain $R_{mf} = \frac{V_o}{I_s} = -R_f$. Source current $I_s = \frac{V_s}{R_1}$.
- Closed-Loop Voltage Gain Derivation: $A_{Vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_1} = \frac{-R_f}{R_1}$.
- Finite Op-Amp Gain Correction: Including finite A_{OL}, exact voltage gain is $A_{Vf} = \frac{-R_f/R_1}{1+\frac{1+R_f/R_1}{A_{OL}}}$, revealing gain error when A_{OL} is small.

Numerical Problem: Gain Variation & Desensitivity Calculation

- Problem Statement: An amplifier has an open-loop voltage gain $A = 10,000 \pm 20\%$. Design a voltage-series feedback network to achieve a closed-loop gain $A_{Vf} = 100$ V/V. Calculate required feedback factor β, desensitivity factor, and final percentage variation in A_{Vf}.
- Step 1 - Calculate Required Feedback Factor (β): From $A_{Vf} = \frac{A}{1+A\beta} \implies 100 = \frac{10,000}{1+10,000\beta} \implies 1 + 10,000\beta = 100 \implies \beta = \frac{99}{10,000} = 0.0099$ (0.99%).
- Step 2 - Determine Desensitivity Factor: $(1 + A\beta) = 1 + (10,000 \times 0.0099) = 100$ (40 dB feedback).
- Step 3 - Calculate Closed-Loop Gain Variation: $\frac{dA_{Vf}}{A_{Vf}} = \frac{1}{1+A\beta}\frac{dA}{A} = \frac{1}{100} \times (\pm 20\%) = \pm 0.20\%$. Closed-loop gain varies by only $\pm 0.20\%$, bounded between 99.8 and 100.2 V/V!

Circuit Example: Single-Stage BJT Voltage-Series Amplifier

- Circuit Parameters: Common-Emitter stage with $R_C = 4.7$ kΩ, un-bypassed emitter resistor $R_E = 470\ \Omega$, $h_{fe} = 120$, $h_{ie} = 2.4$ kΩ, source $R_S = 600\ \Omega$. Feedback sampled at collector and fed to emitter.
- Step 1 - Unloaded Open-Loop Voltage Gain (A_V): Transconductance $g_m = \frac{h_{fe}}{h_{ie}} = \frac{120}{2400\ \Omega} = 50$ mA/V. Open-loop gain $A_V = -g_m R_C = -(0.050) \times 4700 = -235$ V/V.
- Step 2 - Feedback Factor (β): Local emitter resistor provides feedback ratio $\beta = \frac{R_E}{R_C} = \frac{470}{4700} = 0.10$.
- Step 3 - Closed-Loop Gain Calculation: Desensitivity factor $(1 + |A_V|\beta) = 1 + (235 \times 0.10) = 24.5$. Closed-loop gain $A_{Vf} = \frac{-235}{24.5} = -9.59$ V/V.

Summary & Key Takeaways: Voltage Gain of Feedback Amplifiers

- Closed-Loop Voltage Gain Formula: $A_f = \frac{A}{1+A\beta}$ quantitatively describes gain reduction by desensitivity factor $(1 + A\beta)$.
- Asymptotic Precision: For high loop gain ($A\beta \gg 1$), gain simplifies to $A_f \approx \frac{1}{\beta}$, trading raw gain magnitude for passive component precision.
- Gain Desensitivity: Relative gain variations are reduced by factor $(1 + A\beta)$ according to $\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\frac{dA}{A}$.
- Topological Modeling: Voltage-series feedback directly stabilizes voltage gain A_{Vf}, whereas voltage-shunt feedback stabilizes transresistance R_{mf} converted via source resistance R_s.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Advanced Feedback Analysis

- Unified Characterization of Primary Gain Types Across Four Topologies
- Rigorous Two-Port h-Parameter Analysis of Voltage-Series Amplifiers
- Voltage Gain Derivation for Two-Stage CE-CC Cascaded Feedback Pair
- FET Common-Drain & Common-Source Voltage Gain Derivations
- Transresistance (Voltage-Shunt) Feedback to Voltage Gain Conversion
- Multistage Op-Amp Closed-Loop Gain Dynamics & Finite Open-Loop Gain Error
- High-Frequency Response & Single-Pole vs Multi-Pole Response
- Gain-Bandwidth Product Invariance ($A_{0f} \cdot \omega_{Hf} = A_0 \cdot \omega_H$)
- Dominant Pole Frequency Compensation to Prevent Closed-Loop Peaking
- Solved Problem: Complete Two-Port Voltage-Series Analysis
- Solved Problem: High-Frequency Voltage Gain & Closed-Loop Bandwidth
- Impact of Source and Load Impedance Loading on Voltage Gain
- Summary & Engineering Synthesis

Unified Gain Characterization Across Topologies

- Voltage-Series (Series-Shunt): Input V_s, Output V_o. Transfer ratio $A_v = V_o/V_i$, feedback $\beta_v = V_f/V_o$. Closed-loop voltage gain $A_{vf} = \frac{A_v}{1+\beta_v A_v}$.
- Voltage-Shunt (Shunt-Shunt): Input I_s, Output V_o. Transfer ratio $R_m = V_o/I_i$ (transresistance in Ω). Feedback $\beta_g = I_f/V_o$ (Siemens). Terminal voltage gain $A_{vf} = \frac{V_o}{V_s} = \frac{R_{mf}}{R_s} = \frac{R_m/(1+\beta_g R_m)}{R_s}$.
- Current-Series (Series-Series): Input V_s, Output I_o. Transfer ratio $G_m = I_o/V_i$ (transconductance in Siemens). Feedback $\beta_z = V_f/I_o$ (Ω). Terminal voltage gain $A_{vf} = \frac{V_o}{V_s} = \frac{-I_o R_L}{V_s} = \frac{-G_{mf} R_L}{1+\beta_z G_{mf}}$.
- Current-Shunt (Shunt-Series): Input I_s, Output I_o. Transfer ratio $A_i = I_o/I_i$, feedback $\beta_i = I_f/I_o$. Terminal voltage gain $A_{vf} = \frac{V_o}{V_s} = \frac{-A_{if} R_L}{R_s}$.

Rigorous Two-Port Analysis of Voltage-Series Amplifiers

- Step 1 - Topology Verification: Output voltage sampled in parallel; feedback voltage injected in series $\rightarrow$ model feedback network as two-port h-parameter block.
- Step 2 - Determine Loaded Open-Loop Circuit: Load input port of basic amplifier with $h_{11} = Z_{in,\beta}\Big|_{V_o=0}$; load output port with $h_{22}^{-1} = Z_{out,\beta}\Big|_{I_i=0}$.
- Step 3 - Compute Loaded Open-Loop Gain (A_v'): Calculate $A_v' = \frac{V_o'}{V_i'}\Big|_{loaded}$ incorporating h_{11}, h_{22}^{-1}, source R_s, and load R_L.
- Step 4 - Evaluate Feedback Factor & Closed-Loop Gain: Determine $\beta = h_{12} = \frac{V_f}{V_o}\Big|_{I_i=0}$.

  Closed-loop gain is $A_{vf} = \frac{A_v'}{1+\beta A_v'}$.

Voltage Gain Derivation for Two-Stage CE-CC Feedback Pair

- Circuit Configuration: Stage 1 Common-Emitter Q_1, Stage 2 Emitter Follower Q_2. Feedback resistor R_f connected from Emitter of Q_2 back to Emitter of Q_1 (R_{E1}).
- First Stage Loaded Gain (A_{v1}): $A_{v1} = \frac{-h_{fe1}(R_{C1} \| R_{in2})}{r_{\pi 1} + (1+h_{fe1})(R_{E1} \| R_f)}$.
- Second Stage Loaded Gain (A_{v2}): Emitter follower gain $A_{v2} \approx 1.0$. Total open-loop gain $A'_v = A_{v1} \cdot A_{v2}$.
- Feedback Factor & Closed-Loop Gain: Feedback ratio $\beta = \frac{R_{E1}}{R_{E1}+R_f}$. Overall closed-loop voltage gain $A_{vf} = \frac{A'_v}{1+\beta A'_v} \approx \frac{1}{\beta} = 1 + \frac{R_f}{R_{E1}}$.

FET Common-Drain & Common-Source Voltage Gain Analysis

- JFET/MOSFET Voltage Amplifier Model: Small-signal model featuring transconductance g_m and drain output resistance r_d.
- Unbypassed Source Resistor R_S: Introduces local voltage-series feedback. Open-loop gain without feedback $A_v = -g_m(R_D \parallel r_d)$. Feedback ratio $\beta = \frac{R_S}{R_D}$.
- Exact Closed-Loop Gain Equation: Deriving from small-signal AC circuit: $A_{vf} = \frac{-g_m R_D}{1+g_m R_S + \frac{R_D+R_S}{r_d}}$.
- FET Gain Simplification ($r_d \to \infty$): $A_{vf} \approx \frac{-g_m R_D}{1+g_m R_S}$. For high transconductance loop gain ($g_m R_S \gg 1$), gain simplifies to $A_{vf} \approx -\frac{R_D}{R_S}$, independent of g_m!

Transresistance Feedback to Voltage Gain Conversion

- Voltage-Shunt Topology Model: Modeled using two-port y-parameters. Feedback factor $\beta_g = y_{12} = -\frac{I_f}{V_o} = -\frac{1}{R_f}$.
- Loaded Open-Loop Transresistance (R'_m): Calculated by loading input with $y_{11}^{-1} = R_f$ in parallel with R_s and output with $y_{22}^{-1} = R_f$ in parallel with R_L: $R'_m = \frac{V_o}{I_i}\Big|_{loaded}$.
- Closed-Loop Transresistance (R_{mf}): $R_{mf} = \frac{R'_m}{1+\beta_g R'_m} = \frac{R'_m}{1+R'_m/R_f}$.
- Terminal Voltage Gain Equation: $A_{vf} = \frac{V_o}{V_s} = \frac{V_o}{I_s R_s} = \frac{R_{mf}}{R_s} = \frac{-R_f}{R_s} \cdot \frac{1}{1+\frac{R_f+R_s}{R'_m}}$.

Multistage Op-Amp Voltage Gain Dynamics & Finite Gain Error

- Internal Op-Amp Architecture: Cascaded differential input stage ($A_1 \approx 40$ dB), high-gain intermediate stage ($A_2 \approx 60$ dB), and output buffer ($A_3 \approx 0$ dB). Total open-loop gain $A_{OL} = A_1 A_2 A_3 \approx 10^5$ V/V (100 dB).
- Finite Open-Loop Gain Equation: Closed-loop gain for non-inverting amplifier with finite A_{OL}: $A_{vf} = \frac{A_{ideal}}{1+\frac{A_{ideal}}{A_{OL}}}$, where $A_{ideal} = 1 + \frac{R_2}{R_1}$.
- Gain Error Percentage (ϵ_g): $\epsilon_g = \frac{A_{ideal} - A_{vf}}{A_{ideal}} = \frac{A_{ideal}}{A_{OL} + A_{ideal}} \approx \frac{A_{ideal}}{A_{OL}}$.
- Numerical Precision Example: If $A_{ideal} = 100$ V/V and $A_{OL} = 100,000$ V/V, fractional gain error $\epsilon_g = \frac{100}{100,000} = 0.001 = 0.1\%$. Actual gain is 99.9 V/V.

High-Frequency Response & Gain-Bandwidth Constancy

- Single-Pole Open-Loop Model: High-frequency gain response $A(s) = \frac{A_0}{1+s/\omega_H}$, where A_0 is midband gain and $\omega_H = 2\pi f_H$ is 3-dB cutoff frequency.
- Closed-Loop Frequency Transfer Function: Substituting $A(s)$ into $A_f(s) = \frac{A(s)}{1+\beta A(s)}$ yields $A_f(s) = \frac{\frac{A_0}{1+A_0\beta}}{1+\frac{s}{\omega_H(1+A_0\beta)}} = \frac{A_{0f}}{1+s/\omega_{Hf}}$.
- Closed-Loop Bandwidth Expansion: Midband gain drops to $A_{0f} = \frac{A_0}{1+A_0\beta}$, while closed-loop bandwidth expands to $\omega_{Hf} = \omega_H(1 + A_0\beta)$.
- Gain-Bandwidth Product (GBW) Invariance: Multiplying midband gain by bandwidth: $A_{0f} \cdot \omega_{Hf} = \left(\frac{A_0}{1+A_0\beta}\right) \cdot [\omega_H(1 + A_0\beta)] = A_0 \cdot \omega_H = \omega_T$. The GBW product is strictly conserved!

Dominant Pole Compensation & Closed-Loop Peaking

- Multi-Pole Transfer Function: Two-pole open-loop gain $A(s) = \frac{A_0}{(1+s/\omega_1)(1+s/\omega_2)}$ exhibits -180° phase shift at high frequencies.
- Closed-Loop Second-Order System: $A_f(s) = \frac{A_{0f}}{1+s\frac{\omega_1+\omega_2}{\omega_1\omega_2(1+A_0\beta)}+s^2\frac{1}{\omega_1\omega_2(1+A_0\beta)}}$.
- Damping Factor (ζ) & Peaking (M_p): Damping factor $\zeta = \frac{\omega_1+\omega_2}{2\sqrt{\omega_1\omega_2(1+A_0\beta)}}$. If $\zeta < 0.707$, frequency response exhibits peaking $M_p > 1$.
- Dominant Pole Compensation: Adding Miller capacitor C_c pushes dominant pole ω_1 down to ω_D, ensuring phase margin $\phi_m \geq 45^\circ$ to prevent gain peaking.

Numerical Problem: Complete Two-Port Voltage-Series Analysis

- Given Circuit: BJT stage with source $R_s = 1$ kΩ, feedback network resistors $R_1 = 9$ kΩ, $R_2 = 1$ kΩ, collector $R_C = 2$ kΩ, $h_{fe} = 100$, $h_{ie} = 1$ kΩ. Feedback taken from collector and connected to emitter via R_1, R_2.
- Step 1 - Feedback h-parameters: $h_{11} = R_1 \parallel R_2 = 9k \parallel 1k = 900\ \Omega$. $\beta = h_{12} = \frac{R_2}{R_1+R_2} = \frac{1k}{10k} = 0.10$. $h_{22}^{-1} = R_1 + R_2 = 10$ kΩ.
- Step 2 - Loaded Open-Loop Gain (A_v'): Total input resistance $R_{in}' = R_s + h_{ie} + h_{11} = 1000 + 1000 + 900 = 2900\ \Omega$. Total load resistance $R_L' = R_C \parallel h_{22}^{-1} = 2k \parallel 10k = 1.667$ kΩ. Loaded gain $A_v' = \frac{-h_{fe}R_L'}{R_{in}'} = \frac{-100\times 1667}{2900} = -57.48$ V/V.
- Step 3 - Closed-Loop Gain (A_{vf}): Desensitivity factor $(1 + \beta|A_v'|) = 1 + (0.10 \times 57.48) = 6.75$. Closed-loop voltage gain $A_{vf} = \frac{-57.48}{6.75} = -8.52$ V/V.

Numerical Problem: High-Frequency Gain & Bandwidth Calculation

- Problem Statement: An operational amplifier has DC open-loop gain $A_0 = 200,000$ V/V (106 dB) and dominant pole cutoff frequency $f_H = 5$ Hz. Find closed-loop gain A_{vf} and 3-dB bandwidth f_{Hf} for non-inverting feedback configurations with (a) $\beta = 0.01$ and (b) $\beta = 1.0$.
- Case (a) $\beta = 0.01$: Loop gain $A_0\beta = 200,000 \times 0.01 = 2000$. Desensitivity factor $(1 + A_0\beta) = 2001$. Closed-loop gain $A_{vf} = \frac{200,000}{2001} = 99.95$ V/V (40 dB). Closed-loop bandwidth $f_{Hf} = 5$ Hz $\times$ 2001 $= 10.005$ kHz.
- Case (b) Unity Gain Buffer ($\beta = 1.0$): Desensitivity factor $(1 + A_0\beta) = 200,001$. Closed-loop gain $A_{vf} = \frac{200,000}{200,001} \approx 0.999995$ V/V (0 dB). Closed-loop bandwidth $f_{Hf} = 5$ Hz $\times$ $200,001 = 1.000005$ MHz!
- Verification of GBW Invariance: Case (a) 99.95×10.005 kHz $= 1.0$ MHz. Case (b) 1.0×1.0 MHz $= 1.0$ MHz. Gain-bandwidth product is perfectly conserved at 1 MHz!

Impact of Source and Load Impedances on Overall Gain

- Terminal vs. Overall Voltage Gain: Terminal gain $A_v = V_o/V_i$; overall source-to-load voltage gain $A_{vs} = \frac{V_o}{V_s} = A_v \cdot \frac{R_{in}}{R_s+R_{in}} \cdot \frac{R_L}{R_{out}+R_L}$.
- Voltage-Series Loading Mitigation: Voltage-series feedback increases input resistance $R_{in,f} = R_{in}(1 + A\beta)$ and decreases output resistance $R_{out,f} = \frac{R_{out}}{1+A\beta}$.
- Input Loading Factor: $\frac{R_{in,f}}{R_s+R_{in,f}} \approx 1.0$ because $R_{in,f} \gg R_s$.
- Output Loading Factor: $\frac{R_L}{R_{out,f}+R_L} \approx 1.0$ because $R_{out,f} \ll R_L$. Overall gain $A_{vs,f} \approx A_{vf}$, isolating amplifier performance from source and load fluctuations.

Summary & Key Takeaways: Advanced Voltage Gain Dynamics

- Topological Conversion: All four feedback topologies can be converted to effective terminal voltage gain using source (R_s) and load (R_L) network transformations.
- Two-Port Modeling Precision: Modeling feedback loading via h_{11} and h_{22}^{-1} yields exact closed-loop voltage gain $A_{vf} = \frac{A'_v}{1+\beta A'_v}$.
- Gain-Bandwidth Product Invariance: Closed-loop gain reduction expands upper cutoff frequency ($f_{Hf} = f_H(1 + A_0\beta)$), maintaining $A_{0f} \cdot f_{Hf} = f_T$.
- Stability & Compensation: High loop gain in multi-pole systems can cause gain peaking; Miller dominant pole frequency compensation enforces phase margin $\phi_m \geq 45^\circ$.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Parameter-by-Parameter Breakdown

- Parameter 1: Closed-Loop Gain Reduction & Desensitivity Factor
- Parameter 2: Input Impedance Transformations ($R_{in,f}$ for Series vs. Shunt Mixing)
- Parameter 3: Output Impedance Transformations ($R_{out,f}$ for Voltage vs. Current Sampling)
- Parameter 4: System Stability Enhancement & Phase Margin
- Parameter 5: Bandwidth Extension ($f_{H,f}$ and $f_{L,f}$ Derivations)
- Parameter 6: Frequency Response Flattening & Phase Linearization
- Parameter 7: Reduction of Non-Linear Harmonic Distortion ($D_f = \frac{D}{1+A\beta}$)
- Parameter 8: Internal Noise & Power Supply Hum Suppression
- Solved Problem: Full Parameter Evaluation Under Feedback
- Solved Problem: Impedance Transformations in Current-Shunt Feedback
- Comparative Impact Matrix Across 4 Feedback Topologies
- Summary & Key Engineering Takeaways

Parameter 1: Gain Reduction & Desensitivity Factor

- Closed-Loop Gain Formula: $A_f = \frac{A}{1+A\beta}$, where A is open-loop gain and β is feedback ratio.
- Gain Reduction Quantifier: Gain is reduced by the desensitivity factor $(1 + A\beta)$, equivalent to a decibel reduction $N_{dB} = 20 \log_{10}(1 + A\beta)$.
- Gain Desensitivity Function: Sensitivity $S_A^{A_f} = \frac{\partial A_f / A_f}{\partial A / A} = \frac{1}{1+A\beta}$. Open-loop gain variations caused by temperature, aging, or supply fluctuations are suppressed by $(1 + A\beta)$.
- Asymptotic Stabilization: For $A\beta \gg 1$, $A_f \approx \frac{1}{\beta}$, establishing total gain independence from active transistor parameters.

Parameter 2: Input Impedance Transformations ($R_{in,f}$)

- Series Input Connection (Voltage-Series / Current-Series): Feedback voltage V_f opposes input source V_s. Net error voltage $V_i = V_s - V_f = V_s - \beta A V_i \implies V_i(1 + A\beta) = V_s$.
- Input Current Reduction: $I_i = \frac{V_i}{R_{in}} = \frac{V_s}{R_{in}(1+A\beta)}$.
- Series Input Impedance Formula: $R_{in,f} = \frac{V_s}{I_i} = R_{in}(1 + A\beta)$. Input impedance is BOOSTED by factor $(1 + A\beta)$.
- Shunt Input Connection (Voltage-Shunt / Current-Shunt): Feedback current I_f drains source current. Total input current $I_s = I_i + I_f = I_i(1 + A\beta)$.
- Shunt Input Impedance Formula: $R_{in,f} = \frac{V_i}{I_s} = \frac{R_{in}}{1+A\beta}$. Input impedance is REDUCED by factor $(1 + A\beta)$.

Parameter 3: Output Impedance Transformations ($R_{out,f}$)

- Voltage (Shunt) Output Sampling (Voltage-Series / Voltage-Shunt): Output voltage V_o sampled. Deactivate source ($V_s = 0$) and apply test voltage V_x at output port.
- Error Voltage Induced: $V_i = -V_f = -\beta V_x$. Test current $I_x = \frac{V_x - AV_i}{R_{out}} = \frac{V_x - A(-\beta V_x)}{R_{out}} = \frac{V_x(1+A\beta)}{R_{out}}$.
- Voltage Sampling Output Impedance: $R_{out,f} = \frac{V_x}{I_x} = \frac{R_{out}}{1+A\beta}$. Output impedance is REDUCED by factor $(1 + A\beta)$ (behaves as ideal voltage source).
- Current (Series) Output Sampling (Current-Series / Current-Shunt): Output current I_o sampled.
- Current Sampling Output Impedance: $R_{out,f} = R_{out}(1 + A\beta)$. Output impedance is BOOSTED by factor $(1 + A\beta)$ (behaves as ideal current source).

Parameter 4: System Stability Enhancement

- Operating Point Drift Stabilization: Temperature changes cause DC bias point shifts ΔI_C and gain drift ΔA. Closed-loop gain drift is restricted to $\Delta A_f = \frac{\Delta A}{(1+A\beta)^2}$.
- Nyquist Criterion Criterion: Negative feedback suppresses open-loop gain magnitude at critical high frequencies where phase shift approaches -180°.
- Gain Margin (GM) Expansion: $GM = -20\log_{10}|A(j\omega_{180})\beta|$. Increasing feedback desensitivity expands gain margin, preventing runaway oscillations.
- Transient Overshoot Control: Enhances phase margin ϕ_m, reducing ringing and settling time in closed-loop step response.

Parameter 5: Bandwidth Extension Derivations

- High-Frequency Response ($f_{H,f}$): Open-loop gain $A(f) = \frac{A_0}{1+j(f/f_H)}$. Closed-loop response $A_f(f) = \frac{A(f)}{1+\beta A(f)} = \frac{A_0/(1+A_0\beta)}{1+j\frac{f}{f_H(1+A_0\beta)}}$. Upper cutoff frequency becomes $f_{H,f} = f_H(1 + A_0\beta)$.
- Low-Frequency Response ($f_{L,f}$): Open-loop gain $A(f) = \frac{A_0}{1-j(f_L/f)}$. Closed-loop lower cutoff frequency becomes $f_{L,f} = \frac{f_L}{1+A_0\beta}$.
- Total Bandwidth (BW_f): $BW_f = f_{H,f} - f_{L,f} \approx f_H(1 + A_0\beta)$. Bandwidth expands by exact desensitivity factor $(1 + A_0\beta)$!
- Gain-Bandwidth Product Invariance: $A_f \times BW_f = \left(\frac{A_0}{1+A_0\beta}\right) \times [f_H(1 + A_0\beta)] = A_0 \times f_H = f_T$.

Parameter 6: Frequency Response Flattening & Phase Linearization

- Midband Gain Flatness: Within operating passband $f_{L,f} < f < f_{H,f}$, gain fluctuations caused by reactive coupling and stray capacitances are suppressed by factor $(1 + A\beta)$.
- Phase Shift Linearization: Open-loop phase lag $\theta(f) = -\arctan(f/f_H)$ causes non-linear phase delay. Feedback reduces net phase distortion across signal frequencies.
- Ripple Suppression: Smooths out midband ripples and peakings caused by multi-stage reactive networks.
- High-Fidelity Audio Impact: Essential for audio amplifiers to ensure uniform amplification across the full human audible spectrum (20 Hz – 20 kHz).

Parameter 7: Non-Linear Harmonic Distortion Reduction (D_f)

- Distortion Mechanism: Large signal swings push transistors into non-linear transfer regions, generating harmonic distortion voltage D at the output.
- Feedback Output Equation: Output voltage with distortion: $V_o = AV_i + D$. Substituting $V_i = V_s - \beta V_o$ gives $V_o = A(V_s - \beta V_o) + D$.
- Algebraic Derivation: $V_o(1 + A\beta) = AV_s + D \implies V_o = \frac{AV_s}{1+A\beta} + \frac{D}{1+A\beta}$.
- Closed-Loop Distortion Formula: $V_o = A_f V_s + D_f$, where closed-loop distortion $D_f = \frac{D}{1+A\beta}$. Non-linear harmonic distortion is reduced by exact factor $(1 + A\beta)$!

Parameter 8: Noise Reduction & Signal-to-Noise Ratio (SNR)

- Internal Stage Noise Suppression: Power supply hum (50/100 Hz ripple) and thermal noise N generated within intermediate driver or output stages are reduced: $N_f = \frac{N}{1+A\beta}$.
- Input Stage Noise Constraint: Noise voltage N_i generated at the primary input stage (first transistor) is amplified along with signal V_s.
- Output Signal & Noise Scaling: Output signal $V_{os} = A_f V_s$; output input-noise $V_{on} = A_f N_i$.
- SNR Invariance Rule: Signal-to-Noise Ratio at output $SNR_{out} = \frac{V_{os}}{V_{on}} = \frac{A_f V_s}{A_f N_i} = \frac{V_s}{N_i} = SNR_{in}$. Negative feedback CANNOT improve input stage SNR.

Numerical Problem: Full Parameter Evaluation Under Feedback

- Given Open-Loop Parameters: $A_0 = 1000$, $R_{in} = 2$ kΩ, $R_{out} = 40$ kΩ, $f_L = 50$ Hz, $f_H = 50$ kHz, harmonic distortion $D = 10\%$, internal noise $N = 20$ mV. Feedback ratio $\beta = 0.039$ (Voltage-Series topology).
- Desensitivity Factor Calculation: $(1 + A_0\beta) = 1 + (1000 \times 0.039) = 1 + 39 = 40$ (32 dB feedback).
- Calculated Closed-Loop Parameters:
- 1. Gain: $A_f = \frac{1000}{40} = 25$ V/V.
- 2. Input Impedance: $R_{in,f} = R_{in}(1 + A_0\beta) = 2k \times 40 = 80$ kΩ.
- 3. Output Impedance: $R_{out,f} = \frac{R_{out}}{1+A_0\beta} = \frac{40k}{40} = 1$ kΩ.
- 4. Upper Cutoff Frequency: $f_{H,f} = 50$ kHz $\times 40 = 2.0$ MHz.
- 5. Lower Cutoff Frequency: $f_{L,f} = \frac{50 \text{ Hz}}{40} = 1.25$ Hz.
- 6. Distortion: $D_f = \frac{10\%}{40} = 0.25\%$. 7. Internal Noise: $N_f = \frac{20 \text{ mV}}{40} = 0.5$ mV.

Numerical Problem: Impedance Transformation in Current-Shunt Feedback

- Given Circuit: Current-Shunt feedback amplifier with open-loop current gain $A_i = 400$, input impedance $R_{in} = 1.5$ kΩ, output impedance $R_{out} = 10$ kΩ, feedback factor $\beta_i = 0.09$.
- Desensitivity Factor: $(1 + A_i\beta_i) = 1 + (400 \times 0.09) = 1 + 36 = 37$.
- Input Impedance Analysis: Input connection is SHUNT $\implies R_{in,f} = \frac{R_{in}}{1+A_i\beta_i} = \frac{1500\ \Omega}{37} = 40.54\ \Omega$.
- Output Impedance Analysis: Output connection is SERIES (current sampling) $\implies R_{out,f} = R_{out}(1 + A_i\beta_i) = 10\ \text{k}\Omega \times 37 = 370\ \text{k}\Omega$.
- Engineering Function: Transforms stage into an ideal current amplifier with low R_{in} (40.54 Ω) and ultra-high R_{out} (370 kΩ).

Comparative Impact Matrix Across 4 Feedback Topologies

- Voltage-Series (Series-Shunt): Gain $A_{vf} = \frac{A_v}{1+A\beta}$; $R_{in,f} = R_{in}(1 + A\beta)$ (High); $R_{out,f} = \frac{R_{out}}{1+A\beta}$ (Low). Function: Ideal Voltage Amplifier.
- Voltage-Shunt (Shunt-Shunt): Gain $R_{mf} = \frac{R_m}{1+A\beta}$; $R_{in,f} = \frac{R_{in}}{1+A\beta}$ (Low); $R_{out,f} = \frac{R_{out}}{1+A\beta}$ (Low). Function: Ideal Transresistance Amplifier.
- Current-Series (Series-Series): Gain $G_{mf} = \frac{G_m}{1+A\beta}$; $R_{in,f} = R_{in}(1 + A\beta)$ (High); $R_{out,f} = R_{out}(1 + A\beta)$ (High). Function: Ideal Transconductance Amplifier.
- Current-Shunt (Shunt-Series): Gain $A_{if} = \frac{A_i}{1+A\beta}$; $R_{in,f} = \frac{R_{in}}{1+A\beta}$ (Low); $R_{out,f} = R_{out}(1 + A\beta)$ (High). Function: Ideal Current Amplifier.

Summary & Key Takeaways: Parameter Effects of Negative Feedback

- Gain & Desensitivity: Open-loop gain is reduced to $A_f = \frac{A}{1+A\beta}$, suppressing gain variations by factor $(1 + A\beta)$.
- Impedance Control: Series mixing boosts input impedance; shunt mixing reduces input impedance. Voltage sampling reduces output impedance; current sampling boosts output impedance.
- Bandwidth & Linearity: Bandwidth expands by $(1 + A\beta)$ $(BW_f = BW \cdot (1 + A\beta))$, while non-linear harmonic distortion drops to $D_f = \frac{D}{1+A\beta}$.
- Noise Limits: Internal stage noise and power supply hum are reduced to $N_f = \frac{N}{1+A\beta}$, but primary input stage SNR remains unchanged.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Benefits vs. Drawbacks Analysis

- Advantage 1: Gain Stabilization & Thermal/Parameter Immunity
- Advantage 2: Non-Linear Harmonic Distortion Suppression
- Advantage 3: Bandwidth Extension & Passband Flattening
- Advantage 4: Custom Input and Output Impedance Tailoring
- Advantage 5: Internal Noise & Power Supply Ripple Attenuation
- Disadvantage 1: Severe Loss of Overall Voltage Gain
- Disadvantage 2: High-Frequency Phase Shift & Oscillation Risks
- Disadvantage 3: Required Frequency Compensation & Slew Rate Limits
- Disadvantage 4: Inability to Improve Primary Input Stage SNR
- Solved Engineering Problem: Gain Loss vs. Distortion Improvement
- Comparative Summary Table: Advantages vs. Disadvantages
- Summary & Design Recommendations

Advantage 1: Gain Stabilization & Parameter Immunity

- Parameter Instability Problem: Open-loop transistor gain A fluctuates widely due to manufacturing beta spread ($\pm 50\%$), ambient temperature changes, and supply voltage noise.
- Desensitivity Mechanism: Closed-loop gain formula $A_f = \frac{A}{1+A\beta}$ yields fractional variation $\frac{dA_f}{A_f} = \frac{1}{1+A\beta}\frac{dA}{A}$.
- Quantitative Example: For desensitivity factor $(1 + A\beta) = 1000$, a 50% drop in open-loop gain causes only $\frac{50\%}{1000} = 0.05\%$ variation in closed-loop gain.
- IC Manufacturing Impact: Enables mass production of precision analog ICs (op-amps, instrumentation amplifiers) with matched gain without costly manual laser trimming.

Advantage 2: Non-Linear Distortion Reduction

- Transistor Non-Linearity: BJT exponential transfer characteristic ($I_C = I_S e^{V_{BE}/V_T}$) generates non-linear harmonic distortion (D_2, D_3) at large signal amplitudes.
- Distortion Attenuation Equation: Closed-loop harmonic distortion $D_f = \frac{D}{1+A\beta}$, where D is open-loop distortion.
- Quantitative Impact: A feedback factor of 100 (40 dB) reduces Total Harmonic Distortion (THD) from 5.0% down to 0.05%.
- Hi-Fi Audio Relevance: Essential in audio power amplifiers to eliminate push-pull crossover distortion and deliver clean, un-distorted audio signals.

Advantage 3: Bandwidth Extension & Response Flatness

- Frequency Extension: Upper 3-dB cutoff frequency extended to $f_{Hf} = f_H(1 + A_0\beta)$; lower cutoff reduced to $f_{Lf} = \frac{f_L}{1+A_0\beta}$.
- Bandwidth Expansion: Overall bandwidth $BW_f \approx f_H(1 + A_0\beta)$ expands proportionally to feedback factor.
- Gain-Bandwidth Trade-off Flexibility: Engineers can select precise gain-bandwidth combinations while maintaining constant product $A_{0f} \cdot f_{Hf} = f_T$.
- Passband Flattening: Suppresses gain peaking and midband ripples, establishing uniform frequency response across operating bands.

Advantage 4: Custom Input & Output Impedance Tailoring

- Input Impedance Boosting: Voltage-series feedback increases input resistance $R_{in,f} = R_{in}(1 + A\beta)$ into megaohms ($M\Omega$), preventing source loading.
- Output Impedance Minimization: Voltage-series feedback drops output resistance $R_{out,f} = \frac{R_{out}}{1+A\beta}$ to fractional ohms (Ω), creating ideal voltage drivers.
- Current Amplifier Customization: Current-shunt feedback drops R_{in} and boosts R_{out}, forming ideal current buffers.
- Versatile Buffer Design: Allows transformation of standard transistor stages into specialized voltage, current, transresistance, or transconductance amplifiers.

Advantage 5: Internal Noise & Power Supply Hum Suppression

- Internal Noise Mechanism: Thermal noise, shot noise, and 50/100 Hz power supply hum generated in intermediate or output power stages are attenuated by feedback.
- Attenuation Formula: Closed-loop internal stage noise $N_f = \frac{N}{1+A\beta}$.
- Power Supply Rejection Ratio (PSRR): High feedback desensitivity significantly improves op-amp PSRR.
- Operation from Unregulated Supplies: Allows high-power amplifiers to operate from simple unregulated DC power supplies without inducing audible 50 Hz/100 Hz hum.

Disadvantage 1: Severe Loss of Overall Voltage Gain

- Gain Reduction Penalty: Closed-loop gain $A_f = \frac{A}{1+A\beta}$ is reduced by factor $(1 + A\beta)$ compared to open-loop gain A.
- High Gain Loss: Achieving 40 dB of feedback desensitivity reduces voltage gain by 40 dB (100-fold drop).
- Multi-Stage Hardware Overhead: To maintain high closed-loop gain with feedback, designers must cascade multiple gain stages (Q_1, Q_2, Q_3).
- Power & Area Penalty: Increases total transistor count, silicon area, power dissipation, and component cost.

Disadvantage 2: High-Frequency Instability & Oscillation

- Phase Shift Accumulation: Parasitic device capacitances (C_π, C_μ, C_{load}) create high-frequency poles, accumulating phase lag $\theta(f)$.
- Barkhausen Criterion Risk: At frequency f_{180} where phase shift reaches -180°, negative feedback turns into POSITIVE feedback.
- Self-Oscillation Condition: If loop gain magnitude $|A(jf_{180})\beta| \geq 1.0$, the amplifier becomes unstable and oscillates spontaneously.
- Transient Ringing: Low phase margin ($\phi_m < 45^\circ$) causes step-response overshoot and severe transient ringing.

Disadvantage 3: Required Frequency Compensation & Slew Rate Limits

- Compensation Overhead: To guarantee phase margin $\phi_m \geq 60^\circ$, internal compensation networks (Miller capacitor C_c) must be added.
- Slew Rate Degradation: Dominant pole compensation capacitor C_c limits maximum rate of output voltage change: $SR = \frac{I_{tail}}{C_c}$.
- Large-Signal Bandwidth Restriction: High-frequency large-amplitude signals suffer from slew-rate induced distortion.
- Design Complexity: Requires extensive AC stability simulation (Bode plots, Nyquist diagrams, corner analysis), increasing engineering design time.

Disadvantage 4: Inability to Improve Primary Input Stage SNR

- Input Noise Origin: Thermal noise, shot noise, and flicker noise generated at the primary input transistor (Q_1) appear directly in series with source V_s.
- Scaling Behavior: Output signal $V_{os} = A_f V_s$; output input-stage noise $V_{on} = A_f N_i$.
- SNR Invariance: Signal-to-Noise Ratio at output $SNR_{out} = \frac{A_f V_s}{A_f N_i} = \frac{V_s}{N_i} = SNR_{in}$. Negative feedback CANNOT improve input stage SNR.
- LNA Design Restriction: Low-Noise Amplifiers (LNAs) in wireless receivers cannot rely on feedback for noise figure improvement; discrete low-noise components are mandatory.

Engineering Example: Quantifying Gain Loss vs. Distortion Improvement

- Design Requirement: An audio power amplifier requires total harmonic distortion $THD \leq 0.05\%$. Open-loop amplifier has voltage gain $A = 2000$ and open-loop $THD = 4.0\%$.
- Step 1 - Determine Required Desensitivity Factor: $1 + A\beta = \frac{THD_{open}}{THD_{closed}} = \frac{4.0\%}{0.05\%} = 80$ (38.06 dB feedback).
- Step 2 - Calculate Required Feedback Factor (β): $\beta = \frac{80-1}{2000} = \frac{79}{2000} = 0.0395$ (3.95%).
- Step 3 - Calculate Resulting Closed-Loop Gain (A_f): $A_f = \frac{2000}{80} = 25$ V/V (27.96 dB).
- Trade-Off Assessment: Voltage gain drops by 38.06 dB (from 2000 to 25) to achieve an 80-fold reduction in harmonic distortion!

Comparative Analysis: Advantages vs. Disadvantages Summary Matrix

- Gain Stability: + Fractional variation reduced by $(1 + A\beta)$ — - Severe gain reduction $(A_f = \frac{A}{1+A\beta})$
- Bandwidth: + Extended to $f_{Hf} = f_H(1 + A\beta)$ — - Slew rate limited by compensation $(SR = \frac{I}{C_c})$
- Distortion: + Harmonic distortion reduced $(D_f = \frac{D}{1+A\beta})$ — - No improvement in primary input SNR
- Impedance: + Flexible R_{in} boost and R_{out} reduction — - Risk of high-frequency self-oscillation
- Noise: + Internal stage noise and hum suppressed — - Increased circuit complexity and stage count

Summary & Strategic Engineering Design Rules

- Essential Benefits: Negative feedback provides indispensable gain stabilization, non-linear distortion suppression, bandwidth extension, and impedance tailoring.
- Engineering Costs: The price paid includes severe voltage gain loss, risk of high-frequency self-oscillation, slew-rate degradation, and multi-stage complexity.
- Design Rule 1: Always verify Phase Margin $\phi_m \geq 60^\circ$ using Bode plots to prevent instability.
- Design Rule 2: Use Miller dominant pole compensation to secure stability while minimizing slew rate degradation.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Emitter Follower Circuit Breakdown

- Circuit Topology & DC Biasing Analysis (V_B, V_E, I_E, r_e)
- Identification of 100% Voltage-Series Feedback Mechanism ($\beta = 1.0$)
- Small-Signal Hybrid-\{}pi$ AC Equivalent Circuit Modeling
- Exact Mathematical Derivation of Voltage Gain ($A_v = \frac{R'_E}{r_e + R'_E}$)
- Exact Mathematical Derivation of Input Impedance ($R_{in} = R_B \parallel [r_\pi + (1 + \beta_0)R'_E]$)
- Exact Mathematical Derivation of Output Impedance ($R_{out} = R_E \parallel [r_e + \frac{R'_S}{1+\beta_0}]$)
- Current Gain ($A_i \approx \beta_0$) and Power Gain ($A_p \approx \beta_0$) Analysis
- High-Frequency Response & Absence of Miller Effect Multiplication
- Solved Numerical Problem: Complete DC & AC Emitter Follower Analysis
- Practical Application: High-Impedance Sensor Buffer Design
- Large-Signal Drive Limitations & Asymmetrical Cutoff Clipping
- Summary & Key Engineering Takeaways

Circuit Topology & DC Operating Point Analysis

- Circuit Configuration: Collector connected directly to V_{CC} (AC ground), input signal V_i applied to Base, output signal V_o taken from Emitter across resistor R_E.
- Base Voltage DC Bias: Voltage divider biasing gives DC Base voltage $V_B = V_{CC} \frac{R_2}{R_1+R_2}$.
- Emitter DC Voltage & Current: Emitter DC voltage $V_E = V_B - V_{BE} = V_B - 0.7$ V. DC Emitter current $I_E = \frac{V_E}{R_E}$.
- Dynamic Emitter Resistance (r_e): $r_e = \frac{V_T}{I_E} = \frac{26 \text{ mV}}{I_E}$. Base-emitter dynamic resistance $r_\pi = (1 + \beta_0) r_e$.

Feedback Topology: 100% Voltage-Series Feedback

- Feedback Signal Sampling: Output voltage $V_o = V_E$ is sampled directly at the emitter.
- Series Feedback Injection: 100% of output voltage V_o is fed back in series opposition to base input V_i: $v_{be} = v_i - v_o = v_b - v_e$.
- Feedback Ratio: $\beta = 1.0$ (100% voltage-series negative feedback).
- Closed-Loop Gain Formulation: Open-loop gain $A_v = g_m(R_E \parallel r_o) \gg 1$. Closed-loop voltage gain $A_{vf} = \frac{A_v}{1+1 \cdot A_v} = \frac{A_v}{1+A_v} \approx 1.0$ V/V.

Small-Signal Hybrid-\{}pi$ AC Equivalent Circuit Model

- AC Model Representation: Replace BJT with hybrid-\{}pi*modelfeaturingbase* − *emitterresistancer*_\{}pi, *dependentcurrentsourceg*_m v_\{}pi = \{}beta_0 i_b, *andoutputload*R_E' = R_E \{}parallel R_L$.
- Input Voltage Loop Equation: $v_i = v_\pi + v_o = i_b r_\pi + i_e R'_E$.
- Emitter AC Current Relationship: $i_e = i_b + \beta_0 i_b = (1 + \beta_0) i_b$.
- Output Voltage Equation: $v_o = i_e R'_E = (1 + \beta_0) i_b R'_E$.

Exact Derivation of Voltage Gain (A_v)

- Gain Definition: $A_v = \frac{v_o}{v_i} = \frac{(1+\beta_0) i_b R'_E}{i_b r_\pi + (1+\beta_0) i_b R'_E} = \frac{(1+\beta_0) R'_E}{r_\pi + (1+\beta_0) R'_E}$.
- Simplification with r_e: Divide numerator and denominator by $(1+\beta_0)$, substituting $r_e = \frac{r_\pi}{1+\beta_0}$:
- Final Voltage Gain Formula: $A_v = \frac{R'_E}{r_e + R'_E}$, where $R'_E = R_E \parallel R_L$.
- Gain Characteristics: Since $R'_E \gg r_e$ (typically $R'_E \approx 1\ \text{k}\Omega - 10\ \text{k}\Omega$ vs $r_e \approx 5 - 25\ \Omega$), A_v is positive (in-phase output, 0° phase shift) and slightly less than unity ($0.98 - 0.999$).

Exact Derivation of Input Impedance (R_{in})

- Base Input Impedance ($R_{in,base}$): $R_{in,base} = \frac{v_i}{i_b} = \frac{i_b r_\pi + (1+\beta_0) i_b R'_E}{i_b} = r_\pi + (1+\beta_0) R'_E$.
- Resistance Reflection Rule: Emitter resistance R'_E reflected back into the base loop is multiplied by factor $(1+\beta_0)$.
- Total Stage Input Impedance (R_{in}): Including bias resistors $R_B = R_1 \parallel R_2$:
- Final Input Impedance Formula: $R_{in} = R_B \parallel R_{in,base} = R_B \parallel [r_\pi + (1+\beta_0)(R_E \parallel R_L)]$. Reaches hundreds of $k\Omega$ to $M\Omega$.

Exact Derivation of Output Impedance (R_{out})

- Test Source Setup: Deactivate source ($v_s = 0$ V), apply test voltage v_x at emitter port, measure test current i_x.
- Base Loop Equation: $i_b = -\frac{v_x}{r_\pi + (R_S \| R_B)}$, where $R'_S = R_S \parallel R_B$.
- Emitter Test Current: $i_x = -i_b - \beta_0 i_b + \frac{v_x}{R_E} = v_x \left[\frac{1+\beta_0}{r_\pi + R'_S} + \frac{1}{R_E} \right]$.
- Final Output Impedance Formula: $R_{out} = \frac{v_x}{i_x} = R_E \parallel \left[\frac{r_\pi + R'_S}{1+\beta_0} \right] = R_E \parallel \left[r_e + \frac{R_S \| R_B}{1+\beta_0} \right]$. Yields extremely low output impedance ($10\ \Omega - 50\ \Omega$).

Current Gain (A_i) & Power Gain (A_p) Derivation

- Transistor Current Gain: $A_{i,transistor} = \frac{i_e}{i_b} = 1 + \beta_0 \approx \beta_0$ (typically $100 - 300$).
- Stage Current Gain (A_{is}): Accounting for bias divider splitting and load splitting:
- Stage Current Gain Formula: $A_{is} = \frac{i_L}{i_s} = A_{i,transistor} \cdot \frac{R_B}{R_B + R_{in,base}} \cdot \frac{R_E}{R_E + R_L}$.
- Power Gain (A_p): $A_p = A_v \cdot A_{is} \approx 1.0 \cdot A_{is} \approx \beta_0$. Although voltage gain is unity, the Emitter Follower provides high power gain driven entirely by current amplification!

High-Frequency Response & Absence of Miller Effect

- Miller Effect Review: In Common-Emitter stages, base-collector capacitance C_μ is multiplied by $(1 + |A_v|)$, creating large input Miller capacitance $C_{in,M} = C_\mu(1 + A_v)$.
- Common Collector Immunity: In Emitter Follower, Collector is AC grounded. Base-to-Collector voltage equals base voltage v_b, so C_μ is NOT multiplied by voltage gain ($A_{v,BC} = 0$).
- Base-Emitter Capacitance Bootstrapping: Base-to-emitter voltage is $v_{be} = v_i(1 - A_v) \approx 0$. Effective C_π input capacitance is bootstrapped down to $C_{\pi,in} = C_\pi(1 - A_v) \ll C_\pi$.
- Ultra-Wide Bandwidth: Complete absence of Miller multiplication grants the Emitter Follower exceptionally high bandwidth, ideal for high-speed line drivers.

Numerical Problem: Complete AC & DC Emitter Follower Analysis

- Given Parameters: $V_{CC} = 15$ V, $R_1 = 33$ kΩ, $R_2 = 33$ kΩ, $R_E = 3.3$ kΩ, load $R_L = 1$ kΩ, source $R_S = 600$ Ω, transistor $\beta_0 = 150$, $V_{BE} = 0.7$ V.
- Step 1 - DC Analysis: $V_B = 15 \times \frac{33k}{66k} = 7.5$ V. $V_E = 7.5 - 0.7 = 6.8$ V. $I_E = \frac{6.8\text{ V}}{3.3\text{ kΩ}} = 2.06$ mA. Dynamic resistance $r_e = \frac{26\text{ mV}}{2.06\text{ mA}} = 12.62\ Ω$. $r_\pi = (151) \times 12.62 = 1.905$ kΩ.
- Step 2 - Voltage Gain (A_v): $R'_E = 3.3k \parallel 1k = 767.4\ Ω$. $A_v = \frac{767.4}{12.62+767.4} = 0.9838$ V/V.
- Step 3 - Input Impedance (R_{in}): $R_{in,base} = 1.905k + (151 \times 767.4) = 117.78$ kΩ. $R_B = 33k \parallel 33k = 16.5$ kΩ. $R_{in} = 16.5k \parallel 117.78k = 14.47$ kΩ.
- Step 4 - Output Impedance (R_{out}): $R'_S = R_S \parallel R_B = 600 \parallel 16.5k = 578.9\ Ω$. $R_{out} = 3.3k \parallel \left[12.62 + \frac{578.9}{151}\right] = 3.3k \parallel [12.62 + 3.83] = 3.3k \parallel 16.45 = 16.37\ Ω$!

Practical Application: High-Impedance Sensor Buffer Design

- Problem Scenario: A piezoelectric transducer with high source impedance $R_S = 100$ kΩ drives a low impedance load $R_L = 100$ Ω. Compare direct connection versus inserting an Emitter Follower buffer ($R_{in} = 500$ kΩ, $R_{out} = 10$ Ω, $A_v = 0.99$).
- Direct Connection Signal Voltage: $V_L = V_S \frac{R_L}{R_S + R_L} = V_S \frac{100}{100{,}000+100} = 0.000999 V_S$ (99.9% of signal LOST due to loading!).
- Buffered Connection Signal Voltage:
- Input voltage $V_{in} = V_S \frac{R_{in}}{R_S + R_{in}} = V_S \frac{500k}{600k} = 0.8333 V_S$.
- Output voltage $V_L = A_v V_{in} \frac{R_L}{R_{out} + R_L} = (0.99)(0.8333 V_S) \frac{100}{10+100} = 0.750 V_S$.
- Performance Gain: Signal voltage transfer restored from 0.1% to 75.0% — a 750-fold improvement in voltage delivered to the load!

Limitations of Emitter Follower: Cutoff & Clipping

- Asymmetrical Drive Capability: Emitter follower can source large transient currents (transistor turns ON hard), but sinking current is strictly limited by DC bias current $I_E = \frac{V_E - V_{EE}}{R_E}$.
- Negative Swing Cutoff Clipping: On large negative input voltage swings, if load current demand $\frac{\Delta V}{R_L} > I_E$, transistor cuts off completely ($I_C = 0$), clipping the negative waveform.
- Complementary Push-Pull Solution: Replace single transistor and resistor R_E with NPN-PNP complementary pair (Class-AB Emitter Follower).
- Push-Pull Advantage: NPN transistor sources positive load current; PNP transistor sinks negative load current, achieving symmetrical drive capability.

Summary & Key Takeaways: Emitter Follower Circuit

- Voltage Gain & Phase: Near-unity voltage gain ($A_v = \frac{R'_E}{r_e + R'_E} \approx 0.98 - 0.999$), non-inverting ($0^\circ$ phase shift).
- Impedance Transformation: High input impedance ($R_{in} = R_B \parallel [r_\pi + (1 + \beta_0)R'_E]$) and low output impedance ($R_{out} = R_E \parallel [r_e + \frac{R'_S}{1+\beta_0}]$).
- Feedback & Bandwidth: Operates as 100% voltage-series feedback amplifier ($\beta = 1.0$), immune to Miller multiplication, yielding ultra-wide bandwidth.
- Buffer Application: Ideal impedance matching buffer bridging high-impedance sensors and low-impedance loads.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Agenda: Positive Feedback in Oscillators

- Fundamentals of Positive vs Negative Feedback Topologies
- Derivation of Closed-Loop Gain $A_f(s) = \frac{A(s)}{1-A(s)\beta(s)}$
- Initiation of Oscillations: Thermal Noise & Transient Buildup
- Phase & Gain Conditions around the Closed Loop
- Comparative Analysis: Positive Feedback Amplifiers vs Oscillators
- Circuit Case Study: Non-Inverting Wien-Bridge Feedback Topology
- Circuit Case Study: Inverting 3-Stage RC Phase-Shift Feedback Topology
- Role of Frequency-Selective Feedback Networks (RC, LC, Crystal)
- Amplitude Stabilization: Automatic Gain Control (AGC) and Transistor Saturation
- Practical Design Challenges: Frequency Drift, Loading, and Phase Noise
- Summary & Key Engineering Takeaways

Fundamental Feedback Topologies: Positive vs Negative Feedback

- Summing Node Dynamics: In negative feedback, feedback voltage opposes input ($V_{in,eff} = V_s - V_f$); in positive feedback, feedback voltage reinforces input ($V_{in,eff} = V_s + V_f$).
- System Transfer Behavior: Positive feedback increases effective gain, narrows bandwidth, and decreases stability, creating regenerative feedback loops.
- Phase Synchronization: Positive feedback requires feedback signal $V_f = \beta V_{out}$ to be in phase (0° phase difference) with input signal V_{in} at oscillation frequency f_0.
- Energy Conversion Mechanism: Amplifier active components (BJTs, FETs, Op-Amps) draw DC energy from power supply V_{CC} and convert it to AC signal energy under control of positive feedback.

Derivation of Closed-Loop Gain under Positive Feedback

- Block Diagram Relations: Amplifier output voltage $V_{out} = A \cdot V_{in,eff}$; feedback voltage $V_f = \beta \cdot V_{out}$; summing equation $V_{in,eff} = V_s + \beta V_{out}$.
- Algebraic Substitution: $V_{out} = A(V_s + \beta V_{out}) \implies V_{out}(1 - A\beta) = AV_s$.
- Closed-Loop Gain Derivation: $A_f = \frac{V_{out}}{V_s} = \frac{A}{1-A\beta}$, where A is open-loop gain and β is feedback transfer factor.
- Condition for Oscillation without External Drive ($V_s = 0$): For finite output V_{out} with zero input $V_s = 0$, denominator $(1 - A\beta)$ must equal 0, yielding loop gain condition $A\beta = 1 + j0$.

Initiation of Oscillations: Thermal Noise & Transient Buildup

- White Noise Origin: Thermal agitation of electrons in circuit resistors produces white noise with power spectral density $v_n^2 = 4kTB\Delta f$ across all frequencies.
- Frequency Filtering: Frequency-selective feedback network $\beta(f)$ filters white noise, passing only frequency components near resonant frequency f_0.
- Exponential Buildup Dynamics: Initial loop gain $|A\beta| > 1$ places closed-loop poles in right-half s-plane ($s = \sigma \pm j\omega_0$ with $\sigma > 0$), producing exponentially growing envelope $v(t) = V_{noise}e^{\sigma t}\sin(\omega_0 t)$.
- Saturation Limiting: As amplitude grows, transistor non-linearities reduce effective large-signal gain A until steady-state loop gain satisfies $|A\beta| = 1$ with poles on $j\omega$-axis ($\sigma = 0$).

Phase Shift Distribution across Amplifier and Feedback Network

- Total Loop Phase Condition: Total phase shift around feedback loop must be $\angle A(j\omega_0) + \angle\beta(j\omega_0) = 0^\circ$ or 360° ($2\pi n$ radians).
- Inverting Amplifier Configuration: Inverting stage (CE BJT or inverting Op-Amp) introduces $\angle A = 180^\circ$; feedback network must provide $\angle\beta = 180^\circ$ at frequency f_0.
- Non-Inverting Amplifier Configuration: Non-inverting stage (CC BJT or non-inverting Op-Amp) introduces $\angle A = 0^\circ$; feedback network must provide $\angle\beta = 0^\circ$ at frequency f_0.
- Frequency Stability Factor: Phase slope $S_F = \omega_0 \frac{d\phi}{d\omega}\Big|_{\omega=\omega_0}$ determines frequency stability; higher phase slope resists frequency drift caused by component variations.

Comparison: Positive Feedback Amplifiers vs Oscillators

- Operating Loop Gain: Regenerative positive feedback amplifiers maintain $|A\beta| < 1$ (e.g. 0.95); oscillators require startup $|A\beta| > 1$ and steady-state $|A\beta| = 1$.
- Input Signal Requirement: Regenerative amplifiers boost an external input signal V_{in}; oscillators operate completely without external input ($V_{in} = 0$).
- Bandwidth vs Selectivity: Regenerative amplifiers narrow amplifier bandwidth around signal frequency; oscillators produce single pure discrete frequency f_0.
- Output Stability: Amplifiers aim for linear input-output response with low distortion; oscillators intentionally operate into non-linear gain saturation for amplitude limiting.

Circuit Analysis: Non-Inverting Wien-Bridge Oscillator

- Circuit Topology: Op-Amp non-inverting amplifier with gain $A_v = 1 + \frac{R_f}{R_1}$, paired with series-parallel RC Wien-Bridge feedback network.
- Feedback Transfer Factor Derivation: $\beta(s) = \frac{Z_p}{Z_s + Z_p} = \frac{sRC}{s^2R^2C^2 + 3sRC + 1}$; at resonant frequency $\omega_0 = \frac{1}{RC}$, $\beta(j\omega_0) = \frac{1}{3}\angle 0°$.
- Gain Threshold Calculation: For loop gain $A\beta = 1$, op-amp voltage gain must be $A_v = 3$, requiring resistor ratio $\frac{R_f}{R_1} = 2$.
- Practical Startup Criterion: Design sets $\frac{R_f}{R_1} = 2.1$ ($A_v = 3.1, |A\beta| = 1.033 > 1$) for fast startup, with dynamic gain reduction to $A_v = 3.0$ at steady-state amplitude.

Role of Frequency-Selective Networks in Feedback Loops

- Function of $\beta(\omega)$ Network: Acts as narrow bandpass filter establishing phase condition $\angle\beta(j\omega_0) = -\angle A(j\omega_0)$ at single frequency f_0.
- RC Feedback Networks: Lead-lag networks (Wien Bridge) and RC ladder networks (Phase Shift) for audio frequencies (10 Hz – 100 kHz).
- LC Resonant Tanks: Inductive-capacitive networks (Hartley, Colpitts) for radio frequencies (100 kHz – 500 MHz) using energy exchange between L and C.
- Piezoelectric Crystal Networks: Quartz crystals utilizing mechanical resonance for precision clocks (32.768 kHz – 200 MHz) with ultra-high quality factor $Q > 10,000$.

Circuit Analysis: Inverting 3-Stage RC Phase-Shift Oscillator

- Circuit Configuration: Inverting op-amp or BJT CE amplifier (180° phase shift) cascaded with 3-stage high-pass RC ladder feedback network.
- Transfer Function Analysis: \{}beta(s) = \{}frac{s^3 R^3 C^3}{s^3 R^3 C^3 + 6 s^2 R^2 C^2 + 5 s R C + 1}.
- Phase Shift & Resonant Frequency: Imaginary term vanishes at $\omega_0 = \frac{1}{\sqrt{6}RC}$, where phase shift across 3 RC stages is exactly 180°.
- Feedback Attenuation & Gain Requirement: At ω_0, feedback factor $\beta(j\omega_0) = -\frac{1}{29}$; amplifier must provide gain $|A_v| \geq 29$ to satisfy $|A\beta| \geq 1$.

Amplitude Stabilization Mechanisms in Positive Feedback Systems

- Need for Non-linear Gain Limiting: Linear positive feedback loops with $|A\beta| > 1$ grow indefinitely until hard transistor saturation/clipping occurs, causing severe harmonic distortion.
- Automatic Gain Control (AGC) with JFET: Dynamic drain-source resistance $r_{ds}(V_{out})$ of JFET in feedback loop automatically reduces gain A_v as output amplitude increases.
- Thermistors / PTC Resistors: Temperature-dependent resistor in op-amp feedback loop heats up with signal current, increasing resistance and lowering loop gain to exactly 1.
- Diode Clamping Networks: Antiparallel diodes in parallel with feedback resistor R_f conduct during signal peaks, lowering effective R_f and soft-clamping oscillation amplitude.

Practical Design Considerations & Non-Idealities

- Temperature Drift & Frequency Instability: Thermal variations in R and C values cause frequency drift $\Delta f_0 = \frac{\partial f_0}{\partial R}\Delta R + \frac{\partial f_0}{\partial C}\Delta C$.
- Power Supply Rejection: Voltage fluctuations on supply rails V_{CC} alter transistor bias and junction capacitances C_π, C_μ, shifting oscillation frequency.
- Loading Effects: Connecting external load impedance R_L directly across oscillator feedback network lowers effective loop gain below 1, killing oscillations.
- Buffer Stage Requirement: High input-impedance buffer amplifiers (emitter follower or op-amp unity follower) must isolate oscillator tank from external load.

Summary: Principles of Positive Feedback in Oscillators

- Regenerative Positive Feedback: Positive feedback feeds back output signal in phase with input ($V_f = \beta V_{out}$), enabling self-sustained waveform generation from DC power.
- Closed-Loop Criterion: Closed-loop gain $A_f = \frac{A}{1-A\beta}$ yields self-sustained output at $V_s = 0$ when loop gain satisfies $A\beta = 1\angle 0°$.
- Startup & Stabilization: Initial startup uses thermal noise seed with $|A\beta| > 1$; non-linear saturation or AGC dynamically adjusts $|A\beta| = 1$ in steady state.
- Frequency & Phase Control: Frequency-selective networks (RC, LC, Crystal) dictate oscillation frequency f_0, while buffer stages prevent load pulling.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Agenda: Barkhausen's Criteria for Oscillation

- Mathematical Statement of Barkhausen's Criteria
- Complex S-Plane Analysis & Pole Trajectories
- Startup Criterion ($|A\beta| > 1$) vs Steady-State Criterion ($|A\beta| = 1$)
- Phase Slope and Frequency Stability Factor (S_F)
- Application Case Study: RC Phase-Shift Oscillator
- Application Case Study: Wien-Bridge Oscillator
- Application Case Study: Colpitts LC Oscillator
- Non-linear Dynamic Limit Cycles and Transconductance Compression
- Limitations of Barkhausen Criterion & Nyquist Encirclement Test
- Phase Noise Analysis & Leeson's Model
- Summary & Engineering Design Principles

Mathematical Statement of Barkhausen's Criteria

- Loop Gain Definition: $T(s) = A(s)\beta(s)$, where $A(s)$ is amplifier open-loop transfer function and $\beta(s)$ is feedback transfer factor.
- Magnitude Condition: $|T(j\omega_0)| = |A(j\omega_0)\beta(j\omega_0)| = 1$. Energy supplied by amplifier exactly replaces energy dissipated per cycle in feedback network.
- Phase Condition: $\angle T(j\omega_0) = \angle A(j\omega_0) + \angle\beta(j\omega_0) = 2\pi n$ $(n = 0, 1, 2, \dots)$. Signals returning through feedback loop arrive perfectly in phase with original input.
- Combined Complex Representation: $A(j\omega_0)\beta(j\omega_0) = 1 + j0 = 1\angle 0^\circ$ at resonant frequency ω_0.

Complex S-Plane Analysis & Pole Trajectories

- Characteristic Equation: System closed-loop transfer function denominator $1 - A(s)\beta(s) = 0$ determines pole locations $s = \sigma \pm j\omega_0$.
- Left-Half Plane ($\sigma < 0$): Closed-loop poles at $s = -\alpha \pm j\omega_0$ produce exponentially damped oscillations $v(t) = V_0 e^{-\alpha t} \cos(\omega_0 t)$ (sub-critical feedback, $|A\beta| < 1$).
- Right-Half Plane ($\sigma > 0$): Closed-loop poles at $s = +\alpha \pm j\omega_0$ produce exponentially growing oscillations $v(t) = V_0 e^{+\alpha t} \cos(\omega_0 t)$ (super-critical feedback, $|A\beta| > 1$).
- $j\omega$-Axis Alignment ($\sigma = 0$): Steady-state Barkhausen condition places poles exactly on imaginary axis at $s = \pm j\omega_0$, maintaining constant amplitude sinusoidal output $v(t) = V_0 \cos(\omega_0 t)$.

Startup Condition vs Steady-State Criterion

- Small-Signal Startup Requirement: At power-up ($t = 0^+$), circuit requires $|A(j\omega_0)\beta(j\omega_0)| > 1$ (typically 1.05 to 3.0) to force poles into RHP and ensure reliable self-starting from thermal noise.
- Exponential Buildup Phase: Output voltage grows according to $v_{out}(t) = V_{noise} \cdot e^{\frac{|A\beta|-1}{2\tau}t} \cdot \sin(\omega_0 t)$.
- Transconductance Saturation: As AC voltage amplitude increases, active device operates across non-linear $I - V$ characteristic, causing large-signal transconductance $G_m(V_{amp})$ to decrease.
- Dynamic Pole Movement: Pole pair shifts leftward from RHP toward $j\omega$-axis, automatically settling at $|A(j\omega_0)\beta(j\omega_0)|_{large-signal} = 1.0$ at target amplitude V_0.

Phase Slope and Frequency Stability Factor

- Frequency Selection via Phase Zero-Crossing: Operating frequency f_0 is fixed where feedback loop phase $\phi(\omega) = \angle A(j\omega) + \angle \beta(j\omega) = 0°$.
- Frequency Stability Factor Definition: $S_F = \omega_0 \frac{d\phi}{d\omega}\Big|_{\omega=\omega_0} = \frac{d\phi}{d(\Delta f/f_0)}\Big|_{f=f_0}$.
- Sensitivity to Phase Noise: A phase perturbation $\Delta\phi$ caused by component variations produces frequency shift $\Delta f_0 \approx \frac{\Delta\phi}{d\phi/d\omega}$.
- High-Q Stabilization: Networks with high phase slope $\frac{d\phi}{d\omega}$ (such as Quartz crystals and high-Q LC tanks) dramatically increase S_F, minimizing frequency drift.

Application Case Study: RC Phase-Shift Oscillator

- Feedback Network Transfer Function: 3-stage high-pass RC ladder transfer factor $\beta(s) = \frac{s^3R^3C^3}{s^3R^3C^3+6s^2R^2C^2+5sRC+1}$.
- Evaluating on $j\omega$ Axis: $\beta(j\omega) = \frac{-j\omega^3R^3C^3}{(1-6\omega^2R^2C^2)+j(5\omega RC-\omega^3R^3C^3)}$.
- Imposing Phase Condition: Phase shift is 180° when imaginary part of denominator equals zero: $5\omega_0 RC - \omega_0^3R^3C^3 = 0 \implies \omega_0 = \frac{1}{\sqrt{6}RC}$.
- Imposing Magnitude Condition: Substituting ω_0 into real part gives $\beta(j\omega_0) = -\frac{1}{29}$. To satisfy Barkhausen criterion $A\beta = 1$, inverting amplifier gain must be $A_v = -29$ ($|A_v| = 29$).

Application Case Study: Wien-Bridge Oscillator

- Feedback Network Transfer Function: Lead-lag Wien bridge network $\beta(s) = \frac{Z_p}{Z_s+Z_p} = \frac{sRC}{s^2R^2C^2+3sRC+1}$.
- Evaluating on $j\omega$ Axis: $\beta(j\omega) = \frac{j\omega RC}{(1-\omega^2R^2C^2)+j3\omega RC}$.
- Phase Zero-Crossing Condition: Real term in denominator vanishes at $\omega_0^2R^2C^2 = 1 \implies \omega_0 = \frac{1}{RC} \implies f_0 = \frac{1}{2\pi RC}$.
- Magnitude Criterion Evaluation: At ω_0, $\beta(j\omega_0) = \frac{j\omega_0RC}{j3\omega_0RC} = \frac{1}{3}\angle 0^\circ$. Non-inverting op-amp voltage gain $A_v = 1 + \frac{R_f}{R_1}$ must equal 3 ($\frac{R_f}{R_1} = 2$).

Application Case Study: Colpitts LC Oscillator

- Circuit Model: Transistor amplifier coupled with LC tank consisting of split capacitors C_1, C_2 and inductor L.
- Tank Impedance & Resonance: Loop reactance vanishes at $\omega_0 L - \frac{1}{\omega_0 C_1} - \frac{1}{\omega_0 C_2} = 0 \implies \omega_0 = \frac{1}{\sqrt{L C_{eq}}}$, where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$.
- Feedback Factor Calculation: Voltage division across capacitive divider yields $\beta = \frac{V_f}{V_{out}} = \frac{X_{C1}}{X_{C2}} = \frac{C_2}{C_1}$ (with 180° phase inversion via common-emitter configuration).
- Barkhausen Gain Threshold: Transistor voltage gain requirement $|A_v| \geq \frac{C_1}{C_2}$, or transconductance $g_m R_L' \geq \frac{C_1}{C_2}$.

Non-linear Dynamic Limit Cycles & Transconductance Compression

- Phase-Space Representation: Trajectory in $(v, \frac{dv}{dt})$ state space evolves from origin (noise seed) into a stable closed orbit called a limit cycle.
- BJT Large-Signal Transconductance: Collector current under large AC base drive V_m: $I_C(t) = I_Q e^{\frac{V_m \cos \omega t}{V_T}} \implies G_m(V_m) = \frac{g_m}{V_m/V_T} \frac{2I_1(V_m/V_T)}{I_0(V_m/V_T)}$.
- Dynamic Self-Balancing: As peak amplitude V_m grows, large-signal transconductance $G_m(V_m)$ continuously decreases until $G_m(V_m)R_L\beta = 1.0$.
- Sinusoidal Purity Tradeoff: Operating near threshold ($A_{start}\beta \approx 1.1$) yields low distortion sinusoidal output; excessive startup gain ($A_{start}\beta \gg 1$) forces severe non-linear clipping.

Limitations of Barkhausen Criterion & Nyquist Encirclement Test

- Linearization Limitation: Barkhausen criterion assumes linear small-signal steady-state conditions; fails to predict non-linear latch-up or multi-frequency squegging.
- Necessity vs Sufficiency: $A\beta = 1\angle 0^\circ$ is a necessary condition for linear systems, but not always sufficient for complex multi-stage circuits with multiple phase crossings.
- Nyquist Stability Test: Plotting polar locus of $A(j\omega)\beta(j\omega)$ from $\omega = -\infty$ to $+\infty$; sustained oscillation requires Nyquist plot to pass through or encircle critical point $(1, j0)$.
- Gain & Phase Margins: Oscillators are engineered with negative gain margin at f_0 during startup to guarantee instability, transitioning to 0 dB margin at steady state.

Phase Noise & Spectral Purity Model

- Spectral Line Broadening: Ideal oscillator produces delta function spectrum $\delta(f - f_0)$; actual oscillator has phase noise sidebands due to thermal and flicker noise.
- Leeson's Phase Noise Model: $L(f_m) = 10 \log_{10} \left[\frac{1}{2} \left(1 + \left(\frac{f_0}{2Q_L f_m} \right)^2 \right) \left(1 + \frac{f_c}{f_m} \right) \frac{FkT}{P_{sig}} \right]$ in dBc/Hz.
- Key Parameters: f_m is offset frequency from carrier, Q_L is loaded quality factor, f_c is flicker noise corner frequency, F is amplifier noise figure, P_{sig} is signal power.
- Design Rule for High Spectral Purity: Maximize resonator quality factor Q_L and power dissipation P_{sig} while minimizing amplifier noise figure F.

Summary: Key Takeaways on Barkhausen's Criteria

- Barkhausen Conditions: Sustained oscillation requires loop gain magnitude $|A\beta| = 1$ and total loop phase shift $\angle A\beta = 0^\circ$ or 360°.
- Startup vs Steady-State: System requires small-signal $|A\beta| > 1$ for startup from thermal noise, settling to $|A\beta| = 1$ in steady state via gain compression.
- Frequency Determination: Operating frequency f_0 is set by phase condition $\phi(f_0) = 0^\circ$; phase slope $\frac{d\phi}{d\omega}$ dictates frequency stability S_F.
- Practical Applications: Validated across RC Phase-Shift ($f_0 = \frac{1}{2\pi RC\sqrt{6}}, A_v = 29$), Wien-Bridge ($f_0 = \frac{1}{2\pi RC}, A_v = 3$), and Colpitts ($f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}, A_v = \frac{C_1}{C_2}$).

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Agenda: Overall Gain of Positive Feedback Amplifier

- Derivation of Closed-Loop Gain $A_f = \frac{A}{1-A\beta}$
- Operating Regimes based on Loop Gain Magnitude ($A\beta < 1$, $A\beta = 1$, $A\beta > 1$)
- Sensitivity Analysis of Closed-Loop Gain ($S_A^{A_f} = \frac{1}{1-A\beta}$)
- Bandwidth Narrowing & Gain-Bandwidth Product Conservation
- Non-linear Distortion Multiplier & SNR Characteristics
- Quantitative Numerical Example: Gain Spikes & Sensitivity
- Circuit Case Study: Op-Amp Non-Inverting Positive Feedback Stage
- Historical Application: Armstrong Regenerative Receiver
- Comparative Matrix: Open-Loop vs Positive vs Negative Feedback
- Engineering Guidelines to Prevent Unintended Positive Feedback Oscillations
- Summary & Key Engineering Takeaways

Derivation of Closed-Loop Gain Expression

- Summing Node Equation: Effective input voltage $V_i = V_s + V_f = V_s + \beta V_o$, where V_s is source voltage, V_f is feedback voltage, and β is feedback factor.
- Amplifier Output Equation: Output voltage $V_o = A \cdot V_i = A(V_s + \beta V_o)$, where A is open-loop voltage gain.
- Algebraic Expansion: $V_o - A\beta V_o = AV_s \implies V_o(1 - A\beta) = AV_s$.
- Closed-Loop Voltage Gain: $A_f = \frac{V_o}{V_s} = \frac{A}{1-A\beta}$, where loop gain is defined as $T = A\beta$.

Operating Regimes based on Loop Gain Magnitude

- Regime 1 ($0 < A\beta < 1$): Stable Positive Feedback Amplification. Denominator $(1 - A\beta) < 1$, yielding closed-loop gain higher than open-loop gain ($A_f > A$).
- Regime 2 ($A\beta = 1$): Oscillation Threshold. Denominator $(1 - A\beta) = 0 \implies A_f \to \infty$. Circuit produces continuous output V_o with zero input $V_s = 0$.
- Regime 3 ($A\beta > 1$): Super-Critical Instability. Output grows exponentially until active devices saturate or hit power supply rails.
- Regenerative Threshold: Keeping $A\beta$ close to 1 (e.g. 0.99) produces enormous gain ($A_f = 100A$) in a single amplifier stage.

Sensitivity Analysis of Closed-Loop Gain

- Definition of Gain Sensitivity: Sensitivity of closed-loop gain A_f with respect to open-loop gain A: $S_A^{A_f} = \frac{dA_f/A_f}{dA/A} = \frac{dA_f}{dA}\frac{A}{A_f}$.
- Mathematical Derivation: Differentiation yields $\frac{dA_f}{dA} = \frac{(1-A\beta)-A(-\beta)}{(1-A\beta)^2} = \frac{1}{(1-A\beta)^2}$.
- Sensitivity Factor Formula: $S_A^{A_f} = \left[\frac{1}{(1-A\beta)^2}\right]\left[\frac{A}{\frac{A}{1-A\beta}}\right] = \frac{1}{1-A\beta}$.
- Comparison with Negative Feedback: Negative feedback reduces gain sensitivity ($S = \frac{1}{1+A\beta} < 1$), whereas positive feedback amplifies sensitivity ($S = \frac{1}{1-A\beta} > 1$), making gain vulnerable to thermal and parameter variations.

Bandwidth Narrowing & Gain-Bandwidth Product Conservation

- Open-Loop Frequency Response: Single-pole amplifier response $A(s) = \frac{A_0}{1+s/\omega_H}$, where A_0 is DC gain and ω_H is 3dB bandwidth.
- Closed-Loop Transfer Function Derivation: $A_f(s) = \frac{\frac{A_0}{1+s/\omega_H}}{1-\beta\frac{A_0}{1+s/\omega_H}} = \frac{A_0}{1-A_0\beta+s/\omega_H} = \frac{\frac{A_0}{1-A_0\beta}}{1+s/[\omega_H(1-A_0\beta)]}$.
- Closed-Loop Bandwidth Expression: Closed-loop 3dB bandwidth is $\omega_{Hf} = \omega_H(1 - A_0\beta)$.
- Gain-Bandwidth Conservation: $A_{f0} \cdot \omega_{Hf} = \left(\frac{A_0}{1-A_0\beta}\right)(\omega_H(1 - A_0\beta)) = A_0\omega_H = GBW$ (Constant).

Non-linear Distortion Multiplier & SNR Characteristics

- Harmonic Distortion Multiplier: Non-linear distortion generated in amplifier stage is multiplied by feedback factor: $D_f = \frac{D}{1-A\beta}$.
- Reduced Dynamic Range: Near $A\beta \approx 1$, small non-linearities in g_m create severe waveform clipping and intermodulation distortion.
- Noise Amplification: Internal amplifier thermal noise v_n is amplified by closed-loop gain A_f, elevating total output noise power spectral density.
- Selectivity Benefit: Despite distortion trade-offs, positive feedback provides narrow bandpass filtering around resonant frequency f_0, improving frequency selectivity.

Quantitative Numerical Example: Gain Spikes & Sensitivity

- Problem Statement: Consider an amplifier with open-loop gain $A = 100$. Calculate overall closed-loop gain A_f and gain sensitivity S for feedback factors $\beta = 0.005, 0.008, 0.009, 0.0099$.
- Case 1 ($\beta = 0.005$): $A\beta = 0.5 \implies A_f = \frac{100}{1-0.5} = 200$, Sensitivity $S = \frac{1}{0.5} = 2$.
- Case 2 ($\beta = 0.008$): $A\beta = 0.8 \implies A_f = \frac{100}{1-0.8} = 500$, Sensitivity $S = \frac{1}{0.2} = 5$.
- Case 3 ($\beta = 0.0099$): $A\beta = 0.99 \implies A_f = \frac{100}{1-0.99} = 10,000$, Sensitivity $S = \frac{1}{0.01} = 100$. (A 1% change in A causes a 100% change in A_f!).

Circuit Case Study: Op-Amp Positive Feedback Stage

- Circuit Setup: Op-amp connected with feedback resistor R_2 between output and non-inverting terminal $(+)$, and resistor R_1 from $(+)$ terminal to ground.
- Feedback Factor Derivation: Voltage division at $(+)$ terminal gives $\beta = \frac{R_1}{R_1+R_2}$.
- Closed-Loop Gain Formulation: $A_f = \frac{A_v}{1-A_v \frac{R_1}{R_1+R_2}}$, where A_v is op-amp open-loop gain.
- Hysteresis Thresholds in Schmitt Trigger: When $A_v \to \infty$, loop gain $A_v\beta \gg 1$ creates bi-stable switching with upper threshold $V_{UT} = +V_{sat}\frac{R_1}{R_1+R_2}$ and lower threshold $V_{LT} = -V_{sat}\frac{R_1}{R_1+R_2}$.

Historical Application: Armstrong Regenerative Receiver

- Historical Significance: Invented by Edwin Howard Armstrong in 1912; revolutionized radio communications.
- Operating Principle: Controlled positive feedback (regeneration) applied via a tickler coil back to grid circuit, maintaining loop gain $A\beta \approx 0.99$.
- Performance Breakthrough: Single vacuum tube achieved $1000\times$ voltage amplification and razor-sharp selectivity, receiving distant RF signals.
- Oscillation Threshold Risk: If operator adjusted tickler coil past $A\beta = 1$, receiver burst into self-oscillation, radiating interference to nearby radios.

Comparative Matrix: Open-Loop vs Positive vs Negative Feedback

- Gain Parameter: Open-Loop $= A$; Negative Feedback $= A_f = \frac{A}{1+A\beta} < A$; Positive Feedback $= A_f = \frac{A}{1-A\beta} > A$.
- Bandwidth Parameter: Open-Loop $= BW$; Negative Feedback $= BW(1 + A\beta)$ (Wider); Positive Feedback $= BW(1 - A\beta)$ (Narrower).
- Gain Stability / Sensitivity: Open-Loop = High; Negative Feedback = Extremely Low ($S = \frac{1}{1+A\beta}$); Positive Feedback = Extremely High ($S = \frac{1}{1-A\beta}$).
- Primary Applications: Open-Loop = Comparators; Negative Feedback = Linear Amplifiers; Positive Feedback = Oscillators, Schmitt Triggers, Regenerative Receivers.

Engineering Guidelines to Prevent Unintended Oscillations

- Parasitic Feedback Isolation: Minimize parasitic capacitance C_{gd} or C_{μ} between amplifier output and input traces on PCB.
- Power Supply Decoupling: Install ceramic (0.1 μF) and electrolytic (10 μF) decoupling capacitors directly at amplifier supply pins to prevent supply line feedback.
- Ground Plane Design: Utilize continuous low-impedance ground plane to prevent common ground impedance coupling.
- Shielding & Component Placement: Separate input and output stage components physically to prevent radiative electromagnetic positive feedback.

Summary: Key Takeaways on Overall Gain

- Closed-Loop Gain Formulation: Positive feedback increases overall gain to $A_f = \frac{A}{1-A\beta}$.
- Operating Regimes: $0 < A\beta < 1$ yields stable gain enhancement; $A\beta = 1$ triggers self-sustained oscillation ($A_f \to \infty$).
- Gain-Bandwidth Trade-off: Gain increases by $\frac{1}{1-A\beta}$ while 3dB bandwidth narrows by $(1 - A\beta)$, keeping GBW constant.
- Design Caution: High sensitivity $S = \frac{1}{1-A\beta}$ and elevated distortion require strict control of feedback factor β and parasitic coupling.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Agenda: Tank Circuit Fundamentals

- Operational Principles & Flywheel Energy Exchange in LC Tanks
- Derivation of Resonant Frequency $f_0 = \frac{1}{2\pi\sqrt{LC}}$
- Impedance & Admittance Analysis of Ideal vs Practical Tank Circuits
- Quality Factor (Q) Definition, Derivation, and Selectivity
- Differential Analysis of Damped Oscillations & Logarithmic Decrement
- Quantitative Numerical Example: Design & Parameter Calculation
- Tapped Tank Circuits: Hartley Inductive and Colpitts Capacitive Dividers
- Electronic Frequency Tuning via Varactor Diodes and Ferrite Cores
- Loading Effects and Loaded Quality Factor (Q_L)
- Quartz Crystal as an Ultra-High Q Equivalent LC Tank Circuit
- Summary & Key Engineering Takeaways

Operational Principles & Flywheel Energy Exchange

- Energy Storage Elements: Capacitor stores electrostatic energy $E_C = \frac{1}{2}CV^2$; Inductor stores magnetic energy $E_L = \frac{1}{2}LI^2$.
- Flywheel Effect Cycle 1: Fully charged capacitor discharges current $i(t)$ into inductor, building up magnetic flux in inductor coil.
- Flywheel Effect Cycle 2: As capacitor voltage drops to zero, collapsing magnetic field induces electromotive force (EMF) $e = -L\frac{di}{dt}$, recharging capacitor with opposite polarity.
- Self-Sustained Sinusoidal Exchange: In ideal lossless tank ($R_L = 0$), continuous back-and-forth charge circulation maintains constant amplitude sinusoidal voltage waveform.

Derivation of Resonant Frequency f_0

- Admittance Formulation: Inductive admittance $Y_L = \frac{1}{j\omega L} = -j\frac{1}{\omega L}$; Capacitive admittance $Y_C = j\omega C$.
- Total Parallel Admittance: $Y(j\omega) = Y_L + Y_C = j\left(\omega C - \frac{1}{\omega L}\right)$.
- Resonance Condition: Imaginary part of admittance vanishes: $\text{Im}(Y) = 0 \implies \omega_0 C - \frac{1}{\omega_0 L} = 0$.
- Resonant Frequency Formulas: $\omega_0^2 = \frac{1}{LC} \implies \omega_0 = \frac{1}{\sqrt{LC}} \implies f_0 = \frac{1}{2\pi\sqrt{LC}}$.

Impedance Analysis of Ideal vs Practical Tank Circuit

- Ideal Parallel Tank Impedance: At resonance, $Y(\omega_0) = 0 \implies Z_0 = \frac{1}{Y} \to \infty$ (infinite dynamic impedance, acts as open circuit).
- Practical Coil Resistance: Inductor winding has internal resistance R_L. Inductive branch impedance $Z_L = R_L + j\omega L$.
- Practical Parallel Admittance Derivation: $Y = j\omega C + \frac{1}{R_L + j\omega L} = \frac{R_L + j(\omega L - \omega C R_L^2 - \omega^3 L^2 C)}{R_L^2 + \omega^2 L^2}$.
- Equivalent Parallel Resistance (R_p): At resonance $\omega_0 \approx \frac{1}{\sqrt{LC}}$, real conductance $G_p = \frac{R_L}{\omega_0^2 L^2} \implies R_p = \frac{L}{R_L C} = Q^2 R_L$.

Quality Factor (Q) & Selectivity

- Quality Factor Definition: $Q = 2\pi \frac{\text{Maximum Energy Stored}}{\text{Energy Dissipated per Cycle}} = \frac{\omega_0 L}{R_L} = \frac{1}{\omega_0 C R_L}$.
- Parallel Resistance Form: Expressed in terms of equivalent parallel impedance: $Q = \frac{R_p}{\omega_0 L} = R_p \omega_0 C = R_p \sqrt{\frac{C}{L}}$.
- 3dB Bandwidth Relation: $BW = f_2 - f_1 = \frac{f_0}{Q}$.
- Selectivity & Phase Slope: Higher Q produces narrower 3dB bandwidth, sharper frequency selection, and steeper phase transition slope $\left.\frac{d\phi}{d\omega}\right|_{\omega_0} = \frac{2Q}{\omega_0}$.

Differential Analysis of Damped Oscillations

- Differential Equation: Applying KVL around practical RLC tank: $L\frac{d^2q}{dt^2} + R_L\frac{dq}{dt} + \frac{q}{C} = 0$.
- Damping Factor & Damped Natural Frequency: Damping coefficient $\alpha = \frac{R_L}{2L}$; damped resonant frequency $\omega_d = \sqrt{\omega_0^2 - \alpha^2} = \omega_0\sqrt{1 - \frac{1}{4Q^2}}$.
- Transient Voltage Response: Under-damped response ($Q > 0.5$): $v(t) = V_0 e^{-\alpha t}\cos(\omega_d t)$.
- Logarithmic Decrement (δ): Natural logarithm of ratio of successive peak amplitudes: \{}delta = \{}ln\{}left(\{}frac{V_n}{V_{n+1}}\{}right) = \{}alpha T_d \{}approx \{}frac{\{}pi}{Q}.

Quantitative Numerical Example: Design & Parameter Calculation

- Problem Statement: An LC tank circuit uses inductor $L = 100\ \mu$H with winding resistance $R_L = 5\ \Omega$, and tuning capacitor $C = 200$ pF. Calculate f_0, Q, R_p, and BW.
- 1. Resonant Frequency: $f_0 = \frac{1}{2\pi\sqrt{100\times10^{-6}\times200\times10^{-12}}} = \frac{1}{2\pi\sqrt{2\times10^{-14}}} = 1.1254$ MHz.
- 2. Reactance & Quality Factor:
  $X_L = 2\pi f_0 L = 2\pi(1.1254\times10^6)(10^{-4}) = 707.1\ \Omega \implies Q = \frac{707.1}{5} = 141.42.$
- 3. Equivalent Parallel Impedance: $R_p = Q^2 R_L = (141.42)^2 \times 5 = 100$ kΩ (or $R_p = \frac{L}{R_L C} = \frac{10^{-4}}{5\times2\times10^{-10}} = 100$ kΩ).
- 4. 3dB Bandwidth: $BW = \frac{f_0}{Q} = \frac{1.1254\times10^6\ \text{Hz}}{141.42} = 7.958$ kHz.

Tapped Tank Circuits: Inductive & Capacitive Dividers

- Hartley Inductive Tap: Tank inductor split into two series coils L_1 and L_2 with mutual inductance M. Voltage tap fraction $\beta = \frac{L_1+M}{L_1+L_2+2M}$.
- Colpitts Capacitive Tap: Tank capacitor split into series pair C_1 and C_2. Voltage tap fraction $\beta = \frac{V_f}{V_{out}} = \frac{C_1}{C_2}$.
- Impedance Transformation Ratio: Tapping acts as step-down transformer ($n = \frac{N_1}{N_2}$ or $\frac{C_2}{C_1}$), matching high tank impedance R_p (100 kΩ) to low transistor input impedance (1 kΩ).
- Preservation of Tank Q: Tapped impedance transformation prevents heavy loading of main tank resonator by low transistor input impedance.

Electronic Frequency Tuning & Variable Tank Circuits

- Varactor Diode Tuning: Reverse-biased PN junction capacitance $C_v(V_R) = \frac{C_0}{(1+V_R/V_{bi})^n}$. Varying DC tuning voltage V_R sweeps resonant frequency $f_0(V_R) = \frac{1}{2\pi\sqrt{LC_v(V_R)}}$.
- Permeability Tuning: Mechanically shifting high-permeability ferrite core inside inductor coil alters effective inductance $L = \mu_r L_0$, adjusting f_0.
- Switched Capacitor Banks: Digitally switched PIN diode / MOSFET capacitor arrays for wideband multi-band RF synthesizers.
- Air Trimmer Capacitors: Precision mechanical tuning capacitors ($5 - 30$ pF) for high-stability frequency calibration.

Loading Effects and Loaded Quality Factor (Q_L)

- Unloaded vs Loaded Tank: Unloaded tank impedance is $R_p = Q_{unloaded}\omega_0 L$. Connecting external load R_{load} places R_{load} in parallel with R_p.
- Total Parallel Load Resistance: $R_{total} = R_p || R_{load} = \frac{R_p R_{load}}{R_p + R_{load}}$.
- Loaded Quality Factor Formula: $Q_L = \frac{R_{total}}{\omega_0 L} = Q_{unloaded} \cdot \left(\frac{R_{load}}{R_p + R_{load}} \right) = \frac{Q_{unloaded}}{1 + R_p / R_{load}}$.
- Impact on Performance: Heavy loading ($R_{load} < R_p$) drastically reduces Q_L, widening bandwidth $BW_L = \frac{f_0}{Q_L}$ and degrading phase noise.

Quartz Crystal as an Equivalent Ultra-High Q LC Tank

- Piezoelectric Quartz Wafer: Electromechanical coupling converts mechanical vibrations into high-precision electrical resonance.
- Butterworth-Van Dyke (BVD) Model: Motional branch with series L_m (Henries), C_m (femtoFarads), R_m (Ohms), in parallel with static electrode capacitance C_0 (picoFarads).
- Dual Resonance Characteristics: Series resonant frequency $f_s = \frac{1}{2\pi\sqrt{L_m C_m}}$; Parallel resonant frequency $f_p = \frac{1}{2\pi\sqrt{L_m \frac{C_m C_0}{C_m + C_0}}}$.
- Ultra-High Quality Factor: Motional inductance L_m is large (mH to H) while motional resistance R_m is small ($10 - 50\ \Omega$), achieving $Q = \frac{\omega_0 L_m}{R_m} \sim 10,000$ to $500,000$.

Summary: Key Takeaways on LC Tank Circuits

- Resonance Mechanism: Parallel LC tank provides energy exchange between C and L with resonant frequency $f_0 = \frac{1}{2\pi\sqrt{LC}}$.
- Impedance & Loss: Practical tank has finite equivalent parallel resistance $R_p = \frac{L}{R_L C} = Q^2 R_L$ at resonance.
- Quality Factor Impact: Quality factor $Q = \frac{\omega_0 L}{R_L}$ controls selectivity, loaded bandwidth $BW = \frac{f_0}{Q_L}$, and phase slope.
- Advanced Configurations: Tapped tanks (Hartley/Colpitts) provide impedance transformation; varactor diodes enable electronic tuning; quartz crystals provide ultra-high Q resonance.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Agenda: Different Types of Oscillators

- Classification Framework: Waveform Type, Resonator Network, and Frequency Spectrum
- RC Audio Oscillators: 3-Stage RC Phase-Shift Topology
- RC Audio Oscillators: Wien-Bridge Lead-Lag Topology
- LC RF Oscillators: Hartley Tapped-Inductor Topology
- LC RF Oscillators: Colpitts Split-Capacitor Topology
- LC RF Oscillators: Clapp High-Stability Variant
- Crystal Oscillators: Quartz Resonator & Pierce Architecture
- Non-Sinusoidal Relaxation Oscillators & IC 555 Astable Circuits
- Voltage-Controlled Oscillators (VCO) & Phase-Locked Loops (PLL)
- Comparative Analysis Matrix across all Oscillator Families
- Summary & Engineering Selection Guide

Classification Framework for Electronic Oscillators

- Classification by Output Waveform: Sinusoidal (Harmonic) Oscillators produce pure sine waves; Non-Sinusoidal (Relaxation) Oscillators produce square, pulse, or triangular waveforms.
- Classification by Frequency Network: RC Networks (10 Hz – 1 MHz); LC Tanks (100 kHz – 500 MHz); Piezoelectric Crystals (32.768 kHz – 200 MHz); Cavity Resonators ($>$ 1 GHz).
- Classification by Frequency Spectrum: Audio Frequency (AF: 20 Hz – 20 kHz); Radio Frequency (RF: 100 kHz – 300 MHz); Very High Frequency (VHF/UHF: 30 MHz – 3 GHz); Microwave ($>$ 3 GHz).
- Classification by Excitation Mode: Self-excited (feedback oscillators) vs Negative resistance (Gunn/Tunnel diode oscillators).

RC Audio Oscillators: 3-Stage RC Phase-Shift Topology

- Circuit Topology: Inverting amplifier (Op-Amp or CE BJT, 180° phase shift) cascaded with 3-stage high-pass RC ladder feedback network (180° phase shift).
- Resonant Frequency Formula: $f_0 = \frac{1}{2\pi RC\sqrt{6}}$ for equal R, C ladder stages.
- Feedback Factor & Gain Criterion: Feedback factor $\beta(j\omega_0) = -\frac{1}{29}$. To satisfy Barkhausen criterion $A\beta = 1$, inverting amplifier gain must be $|A_v| \geq 29$.
- Engineering Pros & Cons: Pro: Does not require bulky inductors, ideal for fixed audio frequencies (10 Hz – 100 kHz). Con: Poor frequency tuning flexibility since changing f_0 requires ganging 3 variable capacitors.

RC Audio Oscillators: Wien-Bridge Lead-Lag Topology

- Circuit Topology: Non-inverting Op-Amp stage (0° phase shift) paired with series-parallel RC bridge feedback network.
- Resonant Frequency Formula: $f_0 = \frac{1}{2\pi RC}$.
- Feedback Factor & Gain Criterion: At $\omega_0 = \frac{1}{RC}$, phase shift is zero and feedback factor $\beta(j\omega_0) = \frac{1}{3}\angle 0^\circ$. Requires non-inverting amplifier gain $A_v = 1 + \frac{R_f}{R_1} = 3$ ($\frac{R_f}{R_1} = 2$).
- Features & Applications: Excellent frequency tuning across 10 Hz – 1 MHz using dual-ganged variable resistors/capacitors; extremely low total harmonic distortion (THD $< 0.1\%$) when stabilized with JFET AGC or thermistor.

LC RF Oscillators: Hartley Tapped-Inductor Topology

- Circuit Topology: Transistor amplifier combined with LC tank consisting of tapped inductor (L_1, L_2) and single tuning capacitor C.
- Resonant Frequency Formula: $f_0 = \frac{1}{2\pi\sqrt{L_T C}}$, where equivalent total inductance is $L_T = L_1 + L_2 + 2M$ (M is mutual inductance).
- Feedback Factor & Gain Criterion: Feedback ratio $\beta = \frac{L_1+M}{L_2+M}$; required amplifier voltage gain $|A_v| \geq \frac{L_2+M}{L_1+M}$.
- Applications & Limitations: Easily tuned across RF band (100 kHz – 30 MHz) using single variable capacitor C. Main disadvantage: Mutual inductance variations between coil taps cause frequency instability.

LC RF Oscillators: Colpitts Split-Capacitor Topology

- Circuit Topology: Active amplifier coupled with tank circuit using split capacitive voltage divider (C_1, C_2) and single inductor L.
- Resonant Frequency Formula: $f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$, where $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$.
- Feedback Factor & Gain Criterion: Feedback ratio $\beta = \frac{C_1}{C_2}$; required amplifier voltage gain $|A_v| \geq \frac{C_1}{C_2}$.
- Superior Stability: Eliminates mutual inductance problems of Hartley oscillator; provides excellent high-frequency performance in RF/VHF range (1 MHz – 300 MHz).

LC RF Oscillators: Clapp High-Stability Variant

- Circuit Enhancement: Advanced derivative of Colpitts oscillator incorporating a small variable tuning capacitor $C_3 \ll C_1, C_2$ in series with tank inductor L.
- Equivalent Capacitance Derivation: $C'_{eq} = \frac{1}{\frac{1}{C_1}+\frac{1}{C_2}+\frac{1}{C_3}} \approx C_3$ (since $C_3 \ll C_1, C_2$).
- Resonant Frequency Formula: $f_0 \approx \frac{1}{2\pi\sqrt{LC_3}}$.
- Transistor Parasitic Immunity: Transistor junction capacitances C_{in}, C_{out} appear in parallel with large capacitors C_1, C_2. Because $C_3 \ll C_1, C_2$, thermal variations in transistor capacitances have negligible impact on f_0, providing outstanding frequency stability.

Crystal Oscillators: Quartz Resonator & Pierce Architecture

- Piezoelectric Mechanism: Piezoelectric AT-cut quartz crystal wafer converts mechanical acoustic resonance into electrical oscillations.
- Pierce Oscillator Topology: Quartz crystal operates in inductive region between series load capacitors C_1, C_2, connected across CMOS inverter or BJT amplifier.
- Resonant Frequency Stability: Frequency drift is less than $\pm 1 - 10$ ppm over temperature, backed by crystal quality factor $Q \sim 100,000$.
- Ubiquitous Applications: Digital system clocking (32.768 kHz watch crystals, 12 MHz microcontrollers, 25 MHz Ethernet PHYs, 100 MHz PCIe clocks).

Relaxation Oscillators & IC 555 Astable Circuits

- Operating Principle: Non-sinusoidal periodic signal generation through dynamic charging and discharging of timing capacitor C between threshold voltages.
- IC 555 Astable Multivibrator Topology: Capacitor C charges through $(R_A + R_B)$ to $\frac{2}{3}V_{CC}$ and discharges through R_B to $\frac{1}{3}V_{CC}$.
- Timing & Frequency Equations: Charge time $t_H = 0.693(R_A + R_B)C$; Discharge time $t_L = 0.693R_BC$; Total Period $T = 0.693(R_A + 2R_B)C$; Frequency $f = \frac{1.44}{(R_A+2R_B)C}$.
- Duty Cycle Formulation: $D = \frac{t_H}{T} = \frac{R_A+R_B}{R_A+2R_B}$ (always $> 50\%$ for standard configuration).

Voltage-Controlled Oscillators (VCO) & Synthesizers

- VCO Core Architecture: LC tank or ring oscillator where effective tuning capacitance is varied by an external control voltage V_{ctrl} using varactor diodes.
- VCO Transfer Characteristic: Linearized output frequency equation $f_o = f_c + K_{VCO} \cdot V_{ctrl}$, where K_{VCO} is VCO gain constant in MHz/V.
- Ring Oscillator VCO: Chain of an odd number N of CMOS inverters; frequency $f_o = \frac{1}{2Nt_{pd}(V_{ctrl})}$, tuned by controlling inverter supply current.
- Phase-Locked Loop (PLL) Integration: VCO is locked to a stable crystal reference oscillator inside PLL frequency synthesizers for FM modulation and clock multiplication.

Comparative Oscillator Performance Matrix

- RC Phase-Shift: Frequency Range 10 Hz – 100 kHz — Formula $f_0 = \frac{1}{2\pi RC\sqrt{6}}$ — Medium Stability — Uses Inverting Gain $|A_v| \geq 29$ — Audio Fixed Signals.
- Wien-Bridge: Frequency Range 10 Hz – 1 MHz — Formula $f_0 = \frac{1}{2\pi RC}$ — High Stability (Low THD) — Uses Non-inverting Gain $A_v = 3$ — Precision Audio Generators.
- Hartley: Frequency Range 100 kHz – 30 MHz — Formula $f_0 = \frac{1}{2\pi\sqrt{L_T C}}$ — Fair Stability — Tapped Inductor $\beta = \frac{L_1+M}{L_2+M}$ — RF Transmitters.
- Colpitts: Frequency Range 1 MHz – 300 MHz — Formula $f_0 = \frac{1}{2\pi\sqrt{LC_{eq}}}$ — Good Stability — Split Capacitor $\beta = \frac{C_1}{C_2}$ — VHF/RF Receivers.
- Clapp: Frequency Range 10 MHz – 500 MHz — Formula $f_0 \approx \frac{1}{2\pi\sqrt{LC_3}}$ — Excellent Stability — Series Capacitor $C_3 \ll C_1, C_2$ — High-Stability RF local oscillators.
- Pierce Crystal: Frequency Range 32 kHz – 200 MHz — Formula $f_0 = f_s$ or f_p — Ultra-High (± 1 ppm) — Quartz Resonator ($Q \sim 10^5$) — Microcontroller / Digital Clocks.

Summary: Key Takeaways on Oscillator Types

- RC Oscillators: Phase-Shift ($f_0 = \frac{1}{2\pi RC\sqrt{6}}, A_v = 29$) and Wien-Bridge ($f_0 = \frac{1}{2\pi RC}, A_v = 3$) for audio frequency generation.
- LC Oscillators: Hartley (tapped coil), Colpitts (split capacitor), and Clapp (series capacitor C_3) for radio frequency and VHF applications.
- Crystal Oscillators: Quartz crystal resonators ($Q \sim 100,000$) deliver $\pm 1 - 10$ ppm frequency stability in Pierce configurations.
- Relaxation & VCO Systems: IC 555 astable multivibrators generate square waves ($f = \frac{1.44}{(R_A+2R_B)C}$), while VCOs enable electronic frequency synthesis in PLLs.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: LC Resonant Oscillators

- 1. Principles of LC Resonance & Barkhausen Criterion for Sustained Oscillation
- 2. Hartley Oscillator Topology: Circuit Schematic, Tapped Inductor & Operation
- 3. Mathematical Derivation of Hartley Oscillation Frequency (f_o) and Minimum Gain (A_v)
- 4. Colpitts Oscillator Topology: Circuit Schematic, Capacitive Divider & Operation
- 5. Mathematical Derivation of Colpitts Oscillation Frequency (f_o) and Minimum Gain (A_v)
- 6. Op-Amp vs. Transistor (CE) Implementations & Practical High-Frequency Constraints
- 7. Clapp Oscillator Enhancement & Frequency Stability Improvements

Principles of LC Resonance & Barkhausen Criterion

- Parallel LC Resonant Tank: Consists of an inductor L and capacitor C in parallel. Tank impedance is given by $Z_{tank} = \frac{j\omega L}{1-\omega^2 LC}$. At resonance $\omega_0 = 1/\sqrt{LC}$, $Z_{tank} \to \infty$ (purely resistive $R_p = Q\omega_0 L$).
- Barkhausen Criterion for Oscillation: Loop gain must satisfy $|T(j\omega_0)| = |A(j\omega_0)\beta(j\omega_0)| \geq 1$ with total phase shift $\angle T(j\omega_0) = 0^\circ$ or 360°.
- Phase Distribution: Active amplifying device (e.g., Common-Emitter BJT) provides 180° phase inversion; feedback network $\beta(j\omega)$ must provide an additional 180° phase shift at resonance ω_0.
- Energy Exchange Dynamics: Energy continuously exchanges between the magnetic field of inductor L ($E_B = \frac{1}{2}LI^2$) and electric field of capacitor C ($E_E = \frac{1}{2}CV^2$). The active amplifier replenishing I^2R tank losses to maintain constant amplitude.

Hartley Oscillator Topology & Operation

- Tank Circuit Architecture: Employs a center-tapped (split) inductor (L_1, L_2) or two series inductors connected in parallel with a single tuning capacitor C.
- Feedback Mechanism: The tap point of the inductor is connected to AC ground (or cathode/emitter reference). Inductor L_1 forms collector load; inductor L_2 connects to base/emitter feedback path.
- Autotransformer Action: Currents flowing in opposite directions relative to the grounded tap create a 180° phase shift between input and output voltages across the tank.
- Total Equivalent Inductance: $L_{eq} = L_1 + L_2 + 2M$, where M is mutual inductance between coils ($L_{eq} = L_1 + L_2$ if mutual coupling is negligible).
- DC Biasing & Isolation: DC collector bias supplied through RF Choke (RFC) presenting high impedance to RF signals; blocking capacitors isolate DC voltages from tank coils.

Hartley Oscillator Derivation & Mathematical Analysis

- Feedback Factor (β): Defined as ratio of feedback voltage across L_2 to output voltage across L_1: $\beta = \frac{V_{fb}}{V_{out}} = \frac{X_{L2}}{X_{L1}} = \frac{j\omega L_2 + j\omega M}{j\omega L_1 + j\omega M} = \frac{L_2+M}{L_1+M}$.
- Oscillation Frequency (f_o): Resonant frequency where net tank reactance is zero: $f_o = \frac{1}{2\pi\sqrt{L_{eq}C}} = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$.
- Minimum Gain Requirement: Substituting β into Barkhausen criterion $|A_v\beta| \geq 1$ yields $|A_v| \geq \frac{1}{\beta} = \frac{L_1+M}{L_2+M}$. Without mutual coupling ($M = 0$), $|A_v| \geq \frac{L_1}{L_2}$.
- Transconductance Condition for BJT CE Stage: $g_m R'_L \geq \frac{L_1}{L_2}$, where $R'_L = R_C \parallel R_{in,stage} \parallel r_o$ is equivalent load resistance.

Hartley Oscillator Component Design Example

- Problem Statement: Design a BJT Hartley oscillator to operate at $f_o = 1.0$ MHz using a tuning capacitor $C = 470$ pF. The common-emitter amplifier provides voltage gain $A_v = 15$. Determine total required inductance L_{eq} and individual inductances L_1 and L_2 (assume mutual coupling $M = 0$).
- Step 1: Compute Total Equivalent Inductance (L_{eq}):
  $L_{eq} = \frac{1}{4\pi^2 f_o^2 C} = \frac{1}{4\pi^2 (10^6)^2 (470 \times 10^{-12})} \approx 53.89\ \mu$H.
- Step 2: Apply Gain Criterion to determine Inductance Ratio: $|A_v| = \frac{L_1}{L_2} = 15 \Rightarrow L_1 = 15L_2$.
- Step 3: Solve System of Equations for L_1 and L_2: $L_{eq} = L_1 + L_2 = 15L_2 + L_2 = 16L_2 = 53.89\ \mu$H.
- Step 4: Calculate Component Values: $L_2 = \frac{53.89\ \mu\text{H}}{16} \approx 3.37\ \mu$H; $L_1 = 15 \times 3.37\ \mu\text{H} \approx 50.52\ \mu$H.

Colpitts Oscillator Topology & Capacitive Divider

- Tank Circuit Architecture: Consists of a single inductor L connected in parallel with a capacitive voltage divider comprising two series capacitors C_1 and C_2.
- Center Tap Grounding: Junction between C_1 and C_2 is connected to AC ground. Capacitor C_1 is connected across output (collector/drain); C_2 is connected across input (base/gate).
- Phase Inversion Mechanism: AC current through series pair (C_1, C_2) creates equal and opposite polarities across C_1 and C_2 relative to central ground node, yielding exact 180° phase shift.
- Equivalent Series Tank Capacitance (C_{eq}): $C_{eq} = \frac{C_1 C_2}{C_1 + C_2}$.
- Superior High-Frequency Performance: Parasitic input/output capacitances of transistor are absorbed directly into parallel tuning capacitors C_1 and C_2.

Colpitts Oscillator Derivation & Mathematical Analysis

- Feedback Factor (β): Defined as ratio of feedback voltage across C_2 to output voltage across C_1: $\beta = \frac{V_{fb}}{V_{out}} = \frac{X_{C2}}{X_{C1}} = \frac{1/(j\omega C_2)}{1/(j\omega C_1)} = \frac{C_1}{C_2}$.
- Oscillation Frequency (f_o): Resonant frequency of LC tank: $f_o = \frac{1}{2\pi\sqrt{LC_{eq}}} = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}}$.
- Minimum Gain Requirement: Applying Barkhausen criterion $|A_v\beta| \geq 1$ gives $|A_v| \geq \frac{1}{\beta} = \frac{C_2}{C_1}$.
- Small-Signal BJT Transistor Condition: $h_{fe} \geq \frac{C_2}{C_1}$ or $g_m R'_L \geq \frac{C_2}{C_1}$. To ensure reliable startup, design ratio is typically set to $C_2/C_1 \approx 10$ to 20.

Colpitts Oscillator Detailed Calculation Example

- Problem Statement: A Colpitts oscillator operates at $f_o = 5.0$ MHz using an inductor $L = 10.0\ \mu$H. If the active stage requires a gain condition $A_v = C_2/C_1 = 10$, calculate C_1, C_2, and equivalent capacitance C_{eq}.
- Step 1: Calculate Required Equivalent Capacitance (C_{eq}): $C_{eq} = \frac{1}{4\pi^2 f_o^2 L} = \frac{1}{4\pi^2(5\times10^6)^2(10\times10^{-6})} = \frac{1}{4\pi^2(2.5\times10^{14})(10^{-5})} \approx 101.32$ pF.
- Step 2: Express C_{eq} in Terms of C_1 using $C_2 = 10C_1$: $C_{eq} = \frac{C_1(10C_1)}{C_1+10C_1} = \frac{10C_1^2}{11C_1} = \frac{10}{11}C_1$.
- Step 3: Solve for C_1: $C_1 = \frac{11}{10}C_{eq} = 1.1 \times 101.32$ pF ≈ 111.45 pF.
- Step 4: Solve for C_2: $C_2 = 10 \times C_1 = 10 \times 111.45$ pF ≈ 1114.5 pF (standard 1.1 nF).

Op-Amp Based Hartley & Colpitts Implementations

- Inverting Op-Amp Configuration: Op-amp connected in inverting amplifier configuration provides 180° internal phase shift with voltage gain $A_v = -R_f/R_1$.
- Op-Amp Hartley Circuit: Tapped inductor tank (L_1, L_2, C) connected between output and inverting input. Closed-loop gain constraint: $\frac{R_f}{R_1} \geq \frac{L_1}{L_2}$.
- Op-Amp Colpitts Circuit: Capacitive divider tank (C_1, C_2, L) connected in feedback path. Closed-loop gain constraint: $\frac{R_f}{R_1} \geq \frac{C_2}{C_1}$.
- Frequency Limitations of Op-Amps: Limited by Gain-Bandwidth Product (GBWP) and Slew Rate $(SR = 2\pi f V_p)$, restricting Op-Amp LC oscillators to frequencies below $\sim 10 - 20$ MHz. High-frequency RF oscillators (> 50 MHz) use discrete BJTs or MOSFETs.

Comparison: Hartley vs. Colpitts Oscillators

- Frequency Tuning & Adjustment: Hartley is easier to tune across a continuous frequency band using a single variable capacitor C; Colpitts requires ganged variable capacitors (C_1, C_2) or variable inductor L.
- Waveform Purity & Harmonics: Colpitts yields superior spectral purity and lower harmonic distortion because capacitors C_1 and C_2 provide low-impedance bypass paths for high-frequency harmonics.
- Parasitic Effects: Hartley suffers from parasitic inter-winding capacitance of tapped coil; Colpitts absorbs transistor parasitic input/output capacitances into C_1 and C_2.
- Frequency Range: Hartley used primarily in RF/AM broadcast bands (100 kHz – 30 MHz); Colpitts preferred in VHF/UHF radio bands (up to hundreds of MHz).

Frequency Stability & Clapp Oscillator Enhancement

- Frequency Drift Factors: Thermal expansion of inductors, temperature-coefficient of capacitors, and variations in transistor junction capacitances (C_{be}, C_{bc}) due to temperature and voltage fluctuations.
- Clapp Oscillator Architecture: A high-stability variant of Colpitts oscillator that adds a small series tuning capacitor $C_3 \ll C_1, C_2$ in series with inductor L.
- Equivalent Series Capacitance (C'_{eq}): $\frac{1}{C'_{eq}} = \frac{1}{C_1} + \frac{1}{C_2} + \frac{1}{C_3}$. Since $C_3 \ll C_1, C_2$, $C'_{eq} \approx C_3$.
- Oscillation Frequency (f_o): $f_o = \frac{1}{2\pi\sqrt{LC_3}}$. Oscillation frequency becomes virtually independent of C_1, C_2 and transistor stray capacitances, dramatically improving frequency stability.

Summary of LC Oscillators & Design Guidelines

- LC oscillators operate on Barkhausen criterion ($A\beta = 1\angle 0^\circ$) using frequency-selective LC resonant tanks for RF frequency generation.
- Hartley Oscillator uses a tapped inductor ratio (L_1/L_2) for feedback $\beta = L_2/L_1$, requiring amplifier voltage gain $|A_v| \geq L_1/L_2$.
- Colpitts Oscillator uses a split capacitor ratio (C_1/C_2) for feedback $\beta = C_1/C_2$, requiring amplifier voltage gain $|A_v| \geq C_2/C_1$.
- Colpitts provides superior harmonic suppression and high-frequency stability; Clapp topology further isolates frequency from parasitic drift using series capacitor C_3.

Formula Reference & Key Equations

- Hartley Resonant Frequency: $f_o = \frac{1}{2\pi\sqrt{(L_1+L_2+2M)C}}$, Gain Condition: $|A_v| \geq \frac{L_1+M}{L_2+M}$.
- Colpitts Resonant Frequency: $f_o = \frac{1}{2\pi\sqrt{L\frac{C_1C_2}{C_1+C_2}}}$, Gain Condition: $|A_v| \geq \frac{C_2}{C_1}$.
- Clapp Resonant Frequency: $f_o \approx \frac{1}{2\pi\sqrt{LC_3}}$ (where $C_3 \ll C_1, C_2$).
- Tank Quality Factor (Q): $Q = \frac{\omega_0 L}{R_s} = \frac{R_p}{\omega_0 L}$, where higher Q enhances frequency selectivity and phase stability.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Audio Frequency RC Oscillators

- 1. Need for RC Oscillators & Low-Frequency Phase-Shift Principles
- 2. Op-Amp RC Phase-Shift Oscillator: Circuit Schematic & Working
- 3. Mathematical Derivation of Phase-Shift Oscillation Frequency (f_o) and Gain ($A_v \geq 29$)
- 4. BJT-Based Phase-Shift Oscillator: Transistor Loading Effects & h_{fe} Requirements
- 5. Wien-Bridge Oscillator Topology: Lead-Lag Network Resonance & Zero Phase Condition
- 6. Wien-Bridge Op-Amp Design: Derivation of $f_o = 1/(2\pi RC)$ and Gain Requirement ($A_v \geq 3$)
- 7. Automatic Gain Control (AGC) & Non-Linear Amplitude Stabilization Techniques

Low Frequency Oscillation & RC Phase-Shift Principle

- Limitations of LC Oscillators at Audio Frequencies: Resonant frequency $f_o = 1/(2\pi\sqrt{LC})$ requires impractically large inductors (H) and capacitors (μF), causing heavy core losses, bulk, and high cost.
- RC High-Pass Filter Phase Shift: Single RC section $V_{out}/V_{in} = \frac{j\omega RC}{1+j\omega RC}$ introduces a phase lead $\theta = \arctan\left(\frac{1}{\omega RC}\right)$ up to $90^c irc$.
- Three-Stage RC Ladder Network: An inverting amplifier provides 180° phase shift; feedback ladder must provide remaining 180°. A minimum of 3 RC stages is required (each contributing 60° phase shift at f_o).
- Transfer Function of 3-Stage High-Pass RC Ladder: $\beta(s) = \frac{s^3R^3C^3}{s^3R^3C^3+6s^2R^2C^2+5sRC+1}$.

Op-Amp RC Phase-Shift Oscillator Analysis

- Circuit Configuration: Inverting operational amplifier with gain $A_v = -R_f/R_1$ cascaded with a 3-stage high-pass RC feedback ladder (C in series, R to ground).
- Frequency of Oscillation (f_o): Substituting $s = j\omega$ into transfer function $\beta(s)$ and setting imaginary part of denominator to zero:
  $\text{Im}[1 - 6\omega^2 R^2 C^2 + j(5\omega RC - \omega^3 R^3 C^3)] = 0 \Rightarrow 5\omega RC = \omega^3 R^3 C^3 \Rightarrow \omega_0 = \frac{1}{\sqrt{6}RC} \Rightarrow f_o = \frac{1}{2\pi\sqrt{6}RC}$.
- Feedback Attenuation at ω_0: Substituting ω_0 into real part yields $\beta(j\omega_0) = \frac{1}{1-6(1/6)} = -\frac{1}{29}$. Network attenuates signal by factor of 29 with 180° phase inversion.
- Amplifier Gain Requirement: Barkhausen criterion $|A_v\beta| \geq 1 \Rightarrow |A_v| \geq 29 \Rightarrow \frac{R_f}{R} \geq 29$ (setting $R_1 = R$).

BJT-Based RC Phase-Shift Oscillator

- Transistor Loading Considerations: Input resistance of Common-Emitter BJT stage ($h_{ie} \approx \beta_0 r_e$) loads the third RC stage. To maintain equal resistance R, third resistor is chosen as $R_3' = R - h_{ie}$.
- Current Feedback Derivation: Analysis using mesh current analysis for CE transistor with collector load R_C alters frequency equation parameters.
- BJT Oscillation Frequency (f_o): $f_o = \frac{1}{2\pi RC\sqrt{6+4k}}$, where $k = R_C/R$. If $R_C = R$ ($k = 1$), $f_o = \frac{1}{2\pi\sqrt{10}RC}$.
- Minimum Transistor Current Gain (h_{fe}): $h_{fe,min} = 23 + 29\left(\frac{R}{R_C}\right) + 4\left(\frac{R_C}{R}\right)$. For $R_C = R$, minimum transistor current gain is $h_{fe,min} = 56$.

Design Example: Op-Amp Phase-Shift Oscillator

- Problem Statement: Design an Op-Amp RC phase-shift oscillator to generate an audio signal at $f_o = 1.0$ kHz using capacitors $C = 10$ nF. Calculate required resistance R and feedback resistor R_f.
- Step 1: Calculate Timing Resistance (R):
  $f_o = \frac{1}{2\pi\sqrt{6}RC} \Rightarrow R = \frac{1}{2\pi\sqrt{6}f_oC} = \frac{1}{2\pi\sqrt{6}(1000\text{ Hz})(10\times10^{-9}\text{ F})} = \frac{1}{2\pi(2.4495)(10^{-5})} \approx 6.497$ kΩ (standard 6.49 kΩ 1%).
- Step 2: Calculate Minimum Feedback Resistor (R_f):
  $|A_v| = \frac{R_f}{R} \geq 29 \Rightarrow R_f = 29 \times 6.497\text{ kΩ} \approx 188.41$ kΩ.
- Step 3: Practical Implementation Adjustment: Choose R_f as a 180 kΩ resistor in series with a 20 kΩ potentiometer (set to ~ 195 kΩ) to guarantee start-up ($|A\beta| > 1$) and trim amplitude.

Wien-Bridge Oscillator: Bridge Network & Resonance

- Bridge Topology: Incorporates a lead-lag RC bridge network comprising a series arm (R_1, C_1) and parallel arm (R_2, C_2) connected to non-inverting input of Op-Amp.
- Lead-Lag Network Transfer Function $(\beta(s))$: $\beta(s) = \frac{Z_p}{Z_s+Z_p} = \frac{\frac{R_2/(j\omega C_2)}{R_2+1/(j\omega C_2)}}{(R_1+\frac{1}{j\omega C_1})+\frac{R_2/(j\omega C_2)}{R_2+1/(j\omega C_2)}}$.
- Symmetrical Case $(R_1 = R_2 = R,\ C_1 = C_2 = C)$: $\beta(j\omega) = \frac{j\omega RC}{1-\omega^2R^2C^2+3j\omega RC}$.
- Zero Phase Shift Condition: Phase shift $\angle\beta(j\omega) = 0^\circ$ occurs when imaginary term $1 - \omega^2R^2C^2 = 0 \Rightarrow \omega_0 = \frac{1}{RC} \Rightarrow f_o = \frac{1}{2\pi RC}$.

Wien-Bridge Op-Amp Amplifier & Gain Requirements

- Attenuation at Resonant Frequency: Substituting $\omega_0 = 1/(RC)$ into transfer function: $\beta(j\omega_0) = \frac{j(1)}{0+3j(1)} = +\frac{1}{3}\angle 0^\circ$. Lead-lag network attenuates signal by factor of 3 without phase shift.
- Non-Inverting Op-Amp Amplifier: Closed-loop voltage gain equation: $A_v = 1 + \frac{R_f}{R_1}$.
- Barkhausen Criterion Compliance: Loop gain $A_v\beta = \left(1 + \frac{R_f}{R_1}\right) \times \frac{1}{3} \geq 1 \Rightarrow 1 + \frac{R_f}{R_1} \geq 3 \Rightarrow \frac{R_f}{R_1} \geq 2$.
- Exact Balance State: Maintaining $A_v = 3$ exactly ($R_f = 2R_1$) produces sustained, stable, low-distortion sine wave oscillations.

Wien-Bridge Oscillator Component Design Example

- Problem Statement: Design a Wien-bridge oscillator for an audio signal generator operating at $f_o = 10.0$ kHz using standard capacitors $C = 1.0$ nF. Determine resistance R, feedback resistors R_1 and R_f.
- Step 1: Calculate Resistor R:
  $f_o = \frac{1}{2\pi RC} \Rightarrow R = \frac{1}{2\pi f_o C} = \frac{1}{2\pi(10{,}000\ \text{Hz})(1.0\times10^{-9}\ \text{F})} = \frac{1}{2\pi(10^{-5})} \approx 15.915\ \text{k}\Omega$ (standard 15.8 kΩ 1%).
- Step 2: Select Ground Resistor R_1: Choose standard precision resistor $R_1 = 10.0$ kΩ.
- Step 3: Calculate Feedback Resistor R_f: $R_f = 2 \times R_1 = 2 \times 10.0\ \text{k}\Omega = 20.0\ \text{k}\Omega$.
- Step 4: Real-World Adjustments: Use a 18.0 kΩ resistor in series with a 5.0 kΩ trimmer resistor to fine-tune loop gain to 3.00.

Amplitude Stabilization & Automatic Gain Control (AGC)

- Thermal & Tolerance Instability: If $A_v < 3$, oscillations exponentially decay to zero; if $A_v > 3$, oscillations exponentially grow until Op-Amp clips against supply rails (V_{CC}, V_{EE}), introducing severe distortion.
- JFET Automatic Gain Control (AGC): Replace resistor R_1 with a JFET operating in its voltage-controlled linear ohmic region ($r_{ds} = \frac{r_o}{1 - V_{GS}/V_P}$). Output peak voltage is rectified and fed back to JFET gate (V_{GS}), dynamically adjusting $A_v = 3.00$.
- Incandescent Lamp / Thermistor Method: Lamp with positive temperature coefficient (PTC) placed as R_1; rising output amplitude heats filament, increasing R_1 and reducing gain $1 + R_f/R_1$ back to 3.
- Diode Limiting Network: Parallel back-to-back diodes across portion of R_f smoothly decrease effective feedback resistance as peak signal voltage exceeds diode threshold ($V_\gamma \approx 0.7$ V).

Comparison: Phase-Shift vs. Wien-Bridge Oscillators

- Operating Frequency Band: Phase-Shift (1 Hz – 100 kHz); Wien-Bridge (5 Hz – 1 MHz with high-speed Op-Amps).
- Frequency Tuning Capability: Phase-Shift requires simultaneous adjustment of 3 ganged components (3R's or 3C's); Wien-Bridge requires adjusting only 2 ganged components (2R's or 2C's), making it standard for laboratory signal generators.
- Spectral Purity & THD: Wien-Bridge offers ultra-low Total Harmonic Distortion (THD $< 0.01\%$ with AGC); Phase-Shift exhibits higher THD due to high required amplifier gain ($A_v = 29$).
- Gain Requirements: Phase-Shift ($A_v \geq 29$ inverting); Wien-Bridge ($A_v \geq 3$ non-inverting).

Quadrature & State-Variable RC Oscillator Variants

- Quadrature RC Oscillator: Utilizes two cascaded Op-Amp integrators and one inverter in a feedback loop to simultaneously generate sine ($V_{\sin}$) and cosine ($V_{\cos}$) outputs in phase quadrature (90° phase difference).
- Quadrature Frequency Equation: $f_o = \frac{1}{2\pi RC}$.
- State-Variable Active Filter Oscillator: Derived from state-variable active filter by removing damping resistor ($Q \to \infty$), causing second-order poles to sit precisely on $j\omega$-axis.
- Wide Sweep Capability: State-variable topologies enable wide continuous frequency tuning over a 1000:1 range without amplitude breakdown.

Summary of RC Oscillator Topologies

- RC Oscillators are designed for audio frequency generation (1 Hz – 1 MHz), overcoming the size and loss limitations of LC tanks.
- Phase-Shift Oscillator uses a 3-stage high-pass RC ladder providing 180° shift at $f_o = \frac{1}{2\pi\sqrt{6}RC}$, requiring an inverting gain $|A_v| \geq 29$.
- Wien-Bridge Oscillator uses a lead-lag RC bridge providing 0° shift at $f_o = \frac{1}{2\pi RC}$, requiring a non-inverting gain $A_v = 1 + R_f/R_1 \geq 3$.
- Automatic Gain Control (AGC) using JFETs or thermistors is critical in Wien-Bridge circuits to maintain $A_v = 3.00$ and achieve ultra-low harmonic distortion.

Formula Reference & Key Equations

- Op-Amp Phase-Shift Frequency: $f_o = \frac{1}{2\pi\sqrt{6}RC}$, Gain Condition: $|A_v| = \frac{R_f}{R} \geq 29$.
- BJT Phase-Shift Frequency ($R_C = R$): $f_o = \frac{1}{2\pi\sqrt{10}RC}$, Minimum BJT Current Gain: $h_{fe,min} = 56$.
- Wien-Bridge Frequency: $f_o = \frac{1}{2\pi RC}$, Gain Condition: $A_v = 1 + \frac{R_f}{R_1} \geq 3 \Rightarrow R_f \geq 2R_1$.
- JFET Resistance in Ohmic Region: $r_{ds} = \frac{r_{ds0}}{1 - V_{GS}/V_P}$, used for dynamic AGC loop gain stabilization.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Quartz Crystal Resonators

- 1. Physics of the Piezoelectric Effect & Quartz (SiO_2) Crystal Cuts
- 2. Butterworth-Van Dyke (BVD) Electrical Equivalent Circuit Model (L_m, C_m, R_m, C_p)
- 3. Series (f_s) and Parallel (f_p) Resonance Frequencies & Reactance Characteristics
- 4. Quality Factor (Q) & Extreme Frequency Stability Derivations
- 5. Mathematical Parameter Calculation Example for Quartz Resonators
- 6. Pierce Crystal Oscillator Topology: Circuit Schematic, Biasing & Load Capacitance (C_L)
- 7. Advanced Stability: TCXO, OCXO, VCXO & Drive Level Considerations

The Piezoelectric Effect in Quartz (SiO2)

- Direct Piezoelectric Effect: Mechanical stress (compression or tension) applied across specific crystallographic axes of a quartz wafer induces proportional electrical charge polarization ($Q = d \cdot F$).
- Inverse Piezoelectric Effect: An applied electric field across crystal electrodes induces proportional physical mechanical deformation/strain ($\epsilon = d \cdot E$).
- Quartz Material Properties: Single-crystal Silicon Dioxide (SiO_2) exhibits high mechanical hardness, chemical inertness, elastic stability, and an exceptionally low internal friction coefficient.
- AT-Cut Crystal Characteristics: Cut at an angle of $35°15'$ relative to the optical Z-axis. AT-cut crystals operate in thickness-shear mode and exhibit a near-zero temperature coefficient around $25°C$ (frequency drift $< \pm 10$ ppm over $-20°C$ to $+70°C$).

Butterworth-Van Dyke (BVD) Circuit Model

- Electrical Equivalent Circuit: Represents the mechanical quartz resonator as an electrical 4-element network comprising a series motional branch (L_m, C_m, R_m) in parallel with a static electrode capacitance (C_p or C_0).
- Motional Inductance (L_m): Represents the mechanical vibrating mass of the crystal wafer; typically extremely large (mH to hundreds of H).
- Motional Capacitance (C_m): Represents the mechanical elasticity/compliance of the crystal lattice; extremely small (fF to pF).
- Motional Resistance (R_m): Represents internal mechanical friction and acoustic losses; small (10 Ω to 100 Ω).
- Shunt Capacitance (C_p): Electrostatic capacitance formed by metal electrodes sandwiching the quartz dielectric; $C_p \gg C_m$ (typically ratio $r = C_p/C_m \approx 100 - 1000$).

Series (f_s) and Parallel (f_p) Resonance Modes

- Series Resonant Frequency (f_s): Reactance of motional branch cancels out ($X_{Lm} = X_{Cm}$): $f_s = \frac{1}{2\pi\sqrt{L_m C_m}}$. At f_s, motional impedance is purely resistive and at its minimum: $Z(f_s) \approx R_m$.
- Parallel (Anti-Resonant) Frequency (f_p): Net inductive reactance of motional branch resonates with shunt capacitance C_p: $f_p = \frac{1}{2\pi\sqrt{L_m \frac{C_m C_p}{C_m + C_p}}} = f_s\sqrt{1 + \frac{C_m}{C_p}}$. At f_p, net impedance is purely resistive and reaches maximum value.
- Narrow Frequency Bandwidth: Fractional frequency separation: $\frac{\Delta f}{f_s} = \frac{f_p - f_s}{f_s} \approx \frac{C_m}{2C_p} \approx 0.05\% - 0.5\%$.
- Inductive Reactance Region: The crystal exhibits inductive reactance ONLY in the extremely narrow frequency window between f_s and f_p.

Quality Factor (Q) & Extreme Frequency Stability

- Unmatched Quality Factor (Q): Defined as ratio of stored energy to dissipated energy per cycle: $Q = \frac{\omega_s L_m}{R_m} = \frac{1}{\omega_s C_m R_m}$.
- Numerical Comparison: Standard LC tanks achieve $Q \approx 50 - 200$; quartz crystal resonators achieve $Q = 10,000$ to $1,000,000$.
- Extreme Phase Slope ($d\phi/d\omega$): Phase slope derivative at resonance: $\frac{d\phi}{d\omega} \approx \frac{2Q}{\omega_s}$. High Q produces an extremely steep phase curve.
- Frequency Stability Impact: A massive $d\phi/d\omega$ means that any circuit noise or phase disturbance produces an infinitesimally small frequency shift Δf, yielding stability of 10^{-6} to 10^{-10} (1 ppm $-$ 0.001 ppm).

Crystal Resonator Parameter Calculation Example

- Problem Statement: A quartz crystal has BVD equivalent parameters $L_m = 0.8$ H, $C_m = 0.012$ pF, $R_m = 50\ \Omega$, and $C_p = 4.0$ pF. Calculate: (a) Series resonant frequency f_s, (b) Parallel resonant frequency f_p, (c) Bandwidth Δf, and (d) Quality factor Q.
- Step 1: Calculate f_s:
  $f_s = \frac{1}{2\pi\sqrt{L_m C_m}} = \frac{1}{2\pi\sqrt{(0.8)(0.012\times10^{-12})}} = \frac{1}{2\pi\sqrt{9.6\times10^{-15}}} \approx 1,624,146$ Hz $= 1.624146$ MHz.
- Step 2: Calculate f_p:
  $f_p = f_s\sqrt{1+\frac{C_m}{C_p}} = 1.624146 \times \sqrt{1+\frac{0.012\ \text{pF}}{4.0\ \text{pF}}} = 1.624146 \times \sqrt{1.003} \approx 1.626584$ MHz.
- Step 3: Compute Bandwidth (Separation Δf):
  $\Delta f = f_p - f_s = 1.626584$ MHz $- 1.624146$ MHz $= 2.438$ kHz.
- Step 4: Compute Quality Factor (Q): $Q = \frac{2\pi f_s L_m}{R_m} = \frac{2\pi(1.624146\times10^6)(0.8)}{50} \approx 163,277$.

Pierce Crystal Oscillator Topology

- Circuit Architecture: Uses a digital CMOS inverter (or BJT/Op-Amp) operating as an inverting amplifier, with the crystal connected between input and output, alongside load capacitors C_{L1}, C_{L2} to ground.
- Operation Mode: The crystal operates in its parallel inductive region between f_s and f_p, replacing the inductor in a Colpitts-like topology.
- Load Capacitance (C_L): Total capacitance presented across crystal terminals: $C_L = \frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}} + C_{stray}$.
- Actual Oscillation Frequency (f_L): $f_L = f_s\sqrt{1 + \frac{C_m}{2(C_p+C_L)}}$.
- Feedback Biasing Resistor (R_f): High-value resistor (1 MΩ – 10 MΩ) connected across inverter to bias it in its linear linear high-gain region ($V_{in} = V_{out} = V_{DD}/2$).

Colpitts & Miller Crystal Oscillator Topologies

- Colpitts Crystal Oscillator: Replaces the LC tank inductor with a quartz crystal. Operates in series mode (f_s) when placed in the low-impedance feedback branch, or in parallel mode (f_p) when replacing the main tank coil.
- Miller Crystal Oscillator: Crystal connected between Base and Ground (or Gate and Ground); a tuned LC tank in Collector/Drain circuit is tuned slightly above f_s to present an inductive load.
- Overtone Crystal Oscillators: At frequencies above ~ 30 MHz, fundamental crystal wafers become too thin and mechanically fragile. Overtone circuits operate crystals at odd mechanical harmonics (3rd, 5th, 7th overtones).
- Tuned Selective LC Tank: An auxiliary LC tank is added to suppress fundamental oscillations and select the desired 3rd or 5th overtone mode.

Pierce Oscillator Load Capacitance Design Example

- Problem Statement: A 12.0 MHz Pierce crystal specifies a manufacturer load capacitance $C_L = 18.0$ pF. Estimated PCB trace stray capacitance is $C_{stray} = 3.0$ pF. Calculate required matching external capacitors C_{L1} and C_{L2} (assume $C_{L1} = C_{L2}$).
- Step 1: Set Up Load Capacitance Equation:
  $C_L = \frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}} + C_{stray} \Rightarrow 18.0 = \frac{C_{L1}^2}{2C_{L1}} + 3.0 = \frac{C_{L1}}{2} + 3.0.$
- Step 2: Solve for C_{L1}: $\frac{C_{L1}}{2} = 18.0 - 3.0 = 15.0$ pF $\Rightarrow C_{L1} = 30.0$ pF.
- Step 3: Set C_{L2}: $C_{L2} = C_{L1} = 30.0$ pF (standard 30 pF or 33 pF 5% NPO ceramic capacitors).
- Step 4: Power Drive Level Verification: Check drive power $P_d = I_{rms}^2 R_m < 1.0$ mW to prevent physical crystal damage or thermal frequency pulling.

Temperature-Compensated & Oven-Controlled Oscillators

- TCXO (Temperature Compensated Crystal Oscillator): Uses a varactor diode in series with the crystal alongside a thermistor temperature-sensing network to continuously adjust load capacitance C_L and cancel thermal drift to ± 0.5 ppm.
- OCXO (Oven Controlled Crystal Oscillator): Encloses quartz crystal and heating element inside a thermally insulated oven maintained at a constant zero-temp-coefficient turnover temperature ($\sim 75^{\circ}\text{C} - 85^{\circ}\text{C}$); yields ± 0.001 ppm (1 ppb) stability.
- VCXO (Voltage Controlled Crystal Oscillator): Pulls crystal frequency over a narrow range (± 100 ppm) by varying DC control voltage on a series varactor diode; essential for Phase-Locked Loops (PLLs).
- Stability Hierarchy: Standard Crystal ($10 - 50$ ppm) $<$ TCXO ($0.5 - 2$ ppm) $<$ OCXO ($0.001 - 0.01$ ppm).

Crystal Drive Level & Parasitic Spurious Modes

- Drive Level Limitations: Power dissipated in motional resistor R_m ($P_d = I_{rms}^2 R_m$) must be kept below maximum rating ($10\ \mu\text{W} - 500\ \mu\text{W}$). Overdriving causes non-linear frequency frequency shifts, micro-cracking, and accelerated aging.
- Drive Level Dependency (DLD): Abrupt changes in motional resistance R_m and resonant frequency under low drive levels caused by surface micro-contaminants or crystal lattice imperfections.
- Spurious Anharmonic Resonances: Unwanted secondary mechanical vibration modes occurring near desired operating frequency; suppressed through proper crystal blank geometry and dampening.
- Aging Effects: Long-term frequency drift ($1 - 5$ ppm/year) caused by mass transfer (outgassing) onto electrodes or stress relaxation in crystal mounting structures.

Summary of Crystal Oscillators

- Quartz crystal resonators leverage direct and inverse piezoelectricity to achieve unmatched frequency stability ($10^{-6} - 10^{-10}$).
- Butterworth-Van Dyke (BVD) model consists of series motional branch (L_m, C_m, R_m) in parallel with electrostatic electrode capacitance C_p.
- Exhibits dual resonances: Series resonance $f_s = \frac{1}{2\pi\sqrt{L_m C_m}}$ (minimum impedance) and Parallel anti-resonance $f_p = f_s\sqrt{1 + C_m/C_p}$ (maximum impedance).
- Pierce oscillator circuit is the industry-standard microcontroller clock topology, operating crystal in parallel inductive mode between f_s and f_p with load capacitance C_L.

Formula Reference & Key Equations

- Series Resonant Frequency: $f_s = \frac{1}{2\pi\sqrt{L_m C_m}}$.
- Parallel Resonant Frequency: $f_p = f_s\sqrt{1 + \frac{C_m}{C_p}}$.
- Quality Factor (Q): $Q = \frac{\omega_s L_m}{R_m} = \frac{1}{\omega_s C_m R_m}$.
- Pierce Net Load Capacitance: $C_L = \frac{C_{L1}C_{L2}}{C_{L1}+C_{L2}} + C_{stray}$.
- Frequency Pulling Formula: $f_L = f_s\sqrt{1 + \frac{C_m}{2(C_p+C_L)}}$.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: Unijunction Transistor Physics

- 1. Physical Structure, Doping Profile & Circuit Symbol of UJT
- 2. Equivalent Circuit Model & Intrinsic Standoff Ratio (η) Derivation
- 3. Operational Modes: Cut-off Region, Peak Point Voltage (V_P), and Triggering
- 4. Hole Injection Mechanism & Conductivity Modulation in Base-1 Region
- 5. Voltage-Current (V-I) Characteristic Curve Analysis (Cut-off, Negative Resistance, Saturation)
- 6. Temperature Compensation Techniques for Peak Voltage V_P using Base-2 Resistor R_2
- 7. Programmable Unijunction Transistor (PUT): Construction, Operation & Design Formulas

Physical Structure & Terminal Geometry of UJT

- Semiconductor Bar Construction: Formed on a lightly doped N-type silicon bar with two ohmic contact terminals at opposite ends designated as Base 1 (B_1) and Base 2 (B_2).
- Emitter Junction Formation: A heavily doped P-type alloyed region (P^+) is diffused into the N-bar closer to B_2 than B_1, creating a single PN junction.
- Asymmetrical Geometry: Physical distance from Emitter to B_2 is shorter than distance from Emitter to B_1. Unbiased channel resistance R_{B1} is greater than R_{B2}.
- Circuit Symbol Features: Triangle arrow on Emitter terminal points inward toward N-type bar, indicating direction of forward PN junction current ($P \rightarrow N$).
- Terminal Definitions: Emitter (E) acts as trigger/control terminal; Base 1 (B_1) is output reference; Base 2 (B_2) is bias voltage terminal.

UJT Equivalent Circuit & Standoff Ratio (\{}eta)

- Interbase Resistance (R_{BB}): Total resistance of N-bar between B_1 and B_2 with Emitter open-circuited ($I_E = 0$): $R_{BB} = R_{B1} + R_{B2}$ (typical values 4.7 kΩ – 10.0 kΩ).
- Internal Potential Divider: Voltage at internal node N (cathode of PN junction) relative to B_1: $V_N = V_{BB} \times \frac{R_{B1}}{R_{B1}+R_{B2}} = \eta V_{BB}$.
- Intrinsic Standoff Ratio (η): Dimensionless structural parameter defined as $\eta = \frac{R_{B1}}{R_{B1}+R_{B2}} = \frac{R_{B1}}{R_{BB}}$. Typical range $\eta = 0.51$ to 0.82.
- Equivalent Circuit Model: Represented electrically as an ideal PN junction diode D_E connected to internal node N between fixed resistor R_{B2} and variable resistor R_{B1}.

Operational Modes: Cut-Off Region & Triggering

- Cut-Off State ($V_E < V_P$): When applied Emitter voltage V_E is less than node voltage $V_N = \eta V_{BB} + V_D$ (where $V_D \approx 0.6\ \text{V} - 0.7\ \text{V}$ is PN junction diode drop), diode D_E is reverse biased.
- Reverse Leakage Current: Emitter current $I_E = -I_{EO}$ (minority carrier reverse leakage, μA range). UJT presents high input impedance ($M\Omega$) and remains OFF.
- Peak Point Voltage (V_P): Threshold firing voltage required to forward-bias diode D_E: $V_P = \eta V_{BB} + V_D$.
- Peak Point Current (I_P): Minimum emitter current required to trigger UJT from cut-off into negative resistance region (typically $1.0\ \mu\text{A} - 10.0\ \mu\text{A}$).

Negative Resistance & Conductivity Modulation

- Forward Conduction Triggering: When $V_E \geq V_P$, diode D_E becomes forward biased, injecting holes (P^+) into the lightly doped N-type B_1 region.
- Conductivity Modulation Mechanism: Injected minority carriers (holes) attract majority carriers (electrons) into the B_1 channel to maintain charge neutrality, drastically increasing free carrier concentration.
- Collapse of R_{B1}: Increased conductivity causes resistance R_{B1} to drop rapidly from several kΩ down to $20\ \Omega - 50\ \Omega$.
- Negative Resistance Dynamic: As emitter current I_E increases, voltage drop across R_{B1} decreases (V_E drops while I_E rises), creating a negative differential resistance region where $R_{diff} = \frac{dV_E}{dI_E} < 0$.

V-I Characteristic Curve Regions

- Region 1: Cut-off Region ($V_E < V_P$): High impedance state, $I_E \approx 0$. Ends abruptly at Peak Point (V_P, I_P).
- Region 2: Negative Resistance Region ($V_P > V_E > V_V$): Dynamic conductivity modulation occurs. Emitter voltage V_E decreases exponentially as emitter current I_E increases. Ends at Valley Point (V_V, I_V).
- Region 3: Saturation Region ($V_E < V_V, I_E > I_V$): Base-1 region becomes fully flooded with charge carriers; R_{B1} reaches minimum limit $R_{B1,sat}$. Further increase in I_E causes V_E to rise slowly ($R_{diff} > 0$), behaving as a low-resistance ohmic conductor.
- Key Parameter Thresholds: Valley Voltage ($V_V \approx 1.5\ \text{V} - 3.0\ \text{V}$), Valley Current ($I_V \approx 1.0\ \text{mA} - 10.0\ \text{mA}$).

UJT Parameter Calculation Example

- Problem Statement: A UJT has interbase resistance $R_{BB} = 8.0\ \text{k}\Omega$ and intrinsic standoff ratio $\eta = 0.65$. Given supply voltage $V_{BB} = 20.0\ \text{V}$ and PN junction drop $V_D = 0.7\ \text{V}$, calculate: (a) Unbiased base resistances R_{B1} and R_{B2}, (b) Peak point voltage V_P, (c) Interbase leakage current I_{BB} prior to turn-on.
- Step 1: Calculate R_{B1}: $R_{B1} = \eta R_{BB} = 0.65 \times 8.0\ \text{k}\Omega = 5.2\ \text{k}\Omega$.
- Step 2: Calculate R_{B2}: $R_{B2} = R_{BB} - R_{B1} = 8.0\ \text{k}\Omega - 5.2\ \text{k}\Omega = 2.8\ \text{k}\Omega$.
- Step 3: Calculate Peak Point Voltage (V_P):
  $V_P = \eta V_{BB} + V_D = (0.65 \times 20.0\ \text{V}) + 0.7\ \text{V} = 13.0\ \text{V} + 0.7\ \text{V} = 13.7\ \text{V}$.
- Step 4: Compute Interbase Leakage Current (I_{BB}): $I_{BB} = \frac{V_{BB}}{R_{BB}} = \frac{20.0\ \text{V}}{8.0\ \text{k}\Omega} = 2.5\ \text{mA}$.

Temperature Compensation of Peak Voltage V_P

- Temperature Drift Mechanisms: Peak voltage $V_P = \eta V_{BB} + V_D(T)$. PN junction voltage V_D decreases with temperature by ≈ -2.2 mV/°C, while interbase resistance R_{BB} increases with temperature (positive temperature coefficient $+0.8\%/^\circ\text{C}$).
- Compensation Circuit Topology: Place an external resistor R_2 in series with Base 2 terminal (B_2).
- Modified Base Voltage (V'_{BB}): $V'_{BB} = V_{CC} \times \frac{R_{BB}}{R_{BB}+R_2}$. As temperature rises, R_{BB} increases, raising V'_{BB} and compensating for the drop in V_D.
- Optimal Compensation Resistor Equation: $R_2 \approx \frac{0.7R_{BB}}{\eta V_{CC}}$ or empirically $R_2 \approx \frac{10000}{\eta V_{CC}}$ for silicon UJTs.

Programmable Unijunction Transistor (PUT)

- Limitation of Standard UJT: Intrinsic standoff ratio η is fixed permanently during silicon wafer fabrication.
- PUT Structure & Terminals: Four-layer PNPN device (similar to an SCR) featuring three terminals: Anode (A), Cathode (K), and Gate (G) connected to N-region adjacent to Anode.
- Programmable Standoff Ratio (η): Set externally using two resistors (R_A, R_B) forming a voltage divider at Gate terminal: $\eta = \frac{R_B}{R_A+R_B}$.
- PUT Firing Voltage (V_P): $V_P = V_G + V_D = \eta V_{GG} + V_D = \left(\frac{R_B}{R_A+R_B}\right) V_{GG} + V_D$.
- Superior Performance Characteristics: Lower peak current ($I_P < 0.1\ \mu$A), faster switching speeds, adjustable peak firing voltage.

PUT Parameter Design Example

- Problem Statement: Design a PUT gate voltage divider to establish an effective standoff ratio $\eta = 0.70$ with supply voltage $V_{GG} = 15.0$ V and equivalent gate resistance $R_G = 10.0$ kΩ. Calculate peak firing voltage V_P (assume $V_D = 0.6$ V).
- Step 1: Set Up Gate Bias Equations:
  $\eta = \frac{R_B}{R_A+R_B} = 0.70 \Rightarrow R_B = 0.70(R_A + R_B) \Rightarrow R_A = \frac{0.30}{0.70} R_B = 0.4286 R_B$.
- Step 2: Apply Gate Resistance Constraint ($R_G = R_A \parallel R_B$):
  $R_G = \frac{R_A R_B}{R_A+R_B} = 0.70 R_A = 0.70(0.4286 R_B) = 0.30 R_B = 10.0$ kΩ.
- Step 3: Solve for R_B and R_A: $R_B = \frac{10.0 \text{ k}\Omega}{0.30} \approx 33.33$ kΩ; $R_A = 0.4286 \times 33.33$ kΩ ≈ 14.28 kΩ.
- Step 4: Compute Firing Voltage (V_P):
  $V_P = \eta V_{GG} + V_D = (0.70 \times 15.0 \text{ V}) + 0.6 \text{ V} = 10.5 \text{ V} + 0.6 \text{ V} = 11.1 \text{ V}$.

Comparison: UJT vs. BJT vs. FET vs. PUT

- Junction Architecture: UJT (1 PN junction, 3 terminals); BJT (2 PN junctions, 3 terminals); FET (1 channel, 3 terminals); PUT (3 PN junctions, 4 layers).
- Control Mechanism: BJT (current-controlled I_B); FET (voltage-controlled V_{GS}); UJT/PUT (voltage-triggered negative resistance threshold V_P).
- Terminal Designations: UJT (E, B_1, B_2); BJT (B, C, E); FET (G, D, S); PUT (A, K, G).
- Primary Circuit Applications: BJT/FET (linear analog amplification, digital switching); UJT/PUT (relaxation oscillators, SCR/TRIAC phase control triggers, timing delays).

Summary of UJT Structure & Characteristics

- UJT is a 3-terminal, single-junction device (E, B_1, B_2) exhibiting negative differential resistance via conductivity modulation.
- Intrinsic Standoff Ratio $\eta = R_{B1}/R_{BB}$ $(0.51 - 0.82)$ determines peak firing voltage $V_P = \eta V_{BB} + V_D$.
- Conductivity modulation collapses R_{B1} from several kΩ down to $\sim 20\ \Omega$ upon forward biasing diode D_E.
- Base-2 resistor R_2 provides temperature compensation for V_P; PUT allows external programming of η using a two-resistor gate divider.

Formula Reference & Key Equations

- Interbase Resistance: $R_{BB} = R_{B1} + R_{B2} \approx 4.7\ \text{k}\Omega - 10.0\ \text{k}\Omega$.
- Intrinsic Standoff Ratio: $\eta = \frac{R_{B1}}{R_{BB}} = \frac{R_{B1}}{R_{B1}+R_{B2}}$.
- Peak Point Firing Voltage: $V_P = \eta V_{BB} + V_D$.
- Base-2 Temperature Compensation Resistor: $R_2 \approx \frac{10000}{\eta V_{CC}}$.
- PUT Standoff Ratio & Peak Voltage: $\eta = \frac{R_B}{R_A+R_B}$, $V_P = \eta V_{GG} + V_D$.

Electronics Circuit and Application (ECA)

Complete Course Presentation

Course Code: DI02011011

Lecture Agenda: UJT Relaxation Oscillators

- 1. Circuit Configuration & Terminal Topology of UJT Relaxation Oscillator
- 2. Step-by-Step Operational Mechanics & Waveform Cycles (V_E, V_{B1}, V_{B2})
- 3. Mathematical Derivation of Period (T) & Oscillation Frequency (f_o)
- 4. Derivation of Upper ($R_{T,max}$) and Lower ($R_{T,min}$) Resistance Design Bounds
- 5. Numerical Design Example & Component Parameter Selection
- 6. Industrial Application: SCR Phase-Control Triggering & Line Synchronization
- 7. Constant Current Charging for Linear Sawtooth Ramp Generation

Circuit Topology & Component Roles

- Core Circuit Architecture: Timing resistor R_T connected between V_{CC} and Emitter (E); timing capacitor C_T connected between Emitter (E) and Ground.
- Base Terminal Bias Connections: Base 2 (B_2) connected to V_{CC} via temperature compensation resistor R_2; Base 1 (B_1) connected to Ground via small output load resistor R_1 ($50\ \Omega - 100\ \Omega$).
- Output Waveform Terminals: Sawtooth exponential ramp wave taken across capacitor C_T (V_E); sharp positive gate trigger spikes taken across R_1 (V_{B1}); sharp negative spikes taken across R_2 (V_{B2}).
- Dual-Function Capability: Generates timing sweep signals while simultaneously serving as an isolated, high-current trigger pulse generator for power thyristors.

Step-by-Step Operational Mechanics & Cycles

- Phase 1: Capacitor Charging (OFF State): Initially $V_E = 0 < V_P$. Diode D_E is reverse biased. C_T charges exponentially from valley voltage V_V toward V_{CC} through R_T with time constant $\tau = R_T C_T$. Emitter current $I_E \approx 0$. Charging equation: $V_E(t) = V_{CC} - (V_{CC} - V_V)e^{-t/R_T C_T}$.
- Phase 2: UJT Firing & Rapid Discharge (ON State): When $V_E(t)$ reaches peak firing voltage $V_P = \eta V_{BB} + V_D$, UJT fires ON. Resistance R_{B1} collapses to $R_{B1,sat} \approx 20\ \Omega$. C_T rapidly discharges through $R_{B1,sat}$ and R_1 with small time constant $\tau_{dis} = (R_{B1,sat} + R_1)C_T \ll \tau_{charge}$, producing a sharp voltage spike across R_1.
- Phase 3: Turn-OFF & Cycle Reset: When V_E drops down to valley voltage V_V and $I_E < I_V$, UJT turns OFF, restoring high R_{B1} impedance and repeating the cycle.

Derivation of Oscillation Frequency (f_o)

- Charging Period Approximation: Because discharge time constant $\tau_{dis} \ll \tau_{charge}$, total oscillation period $T \approx t_{charge}$.
- Setting Boundary Voltage Conditions: $V_E(T) = V_P = \eta V_{CC} + V_D$. Assuming initial voltage $V_V \approx 0$ and $V_D \ll V_{CC}$:
- Voltage Equation: $\eta V_{CC} = V_{CC}(1 - e^{-T/R_T C_T}) \Rightarrow 1 - \eta = e^{-T/R_T C_T}$.
- Taking Natural Logarithm: $\frac{T}{R_T C_T} = \ln\left(\frac{1}{1-\eta}\right) \Rightarrow T = R_T C_T \ln\left(\frac{1}{1-\eta}\right)$.
- Oscillation Frequency (f_o): $f_o = \frac{1}{T} = \frac{1}{R_T C_T \ln\left(\frac{1}{1-\eta}\right)}$.
- Standoff Ratio Simplification: For typical UJT with $\eta = 0.632$, $\ln\left(\frac{1}{1-0.632}\right) = \ln(2.718) = 1.00 \Rightarrow f_o \approx \frac{1}{R_T C_T}$.

Design Limits & Bounds for Timing Resistor (R_T)

- Upper Bound ($R_{T,max}$ for Successful Turn-ON): Current supplied through R_T when $V_E = V_P$ must exceed Peak Point Current I_P to trigger negative resistance: $R_{T,max} = \frac{V_{CC} - V_P}{I_P}$. If $R_T > R_{T,max}$, capacitor C_T fails to reach V_P and UJT never fires.
- Lower Bound ($R_{T,min}$ for Successful Turn-OFF): Current supplied through R_T when $V_E = V_V$ must be less than Valley Point Current I_V to allow UJT to turn OFF: $R_{T,min} = \frac{V_{CC} - V_V}{I_V}$. If $R_T < R_{T,min}$, UJT remains latched ON continuously.
- Permissible Resistance Window: $\frac{V_{CC} - V_P}{I_P} > R_T > \frac{V_{CC} - V_V}{I_V}$.
- Design Selection Rule: Select R_T safely near the geometric mean of $R_{T,min}$ and $R_{T,max}$ to guarantee reliable oscillation.

UJT Oscillator Complete Design Example

- Problem Statement: Design a UJT relaxation oscillator operating at $f_o = 400$ Hz with $C_T = 0.1$ μF. Given UJT parameters $\eta = 0.65$, $V_P = 13.7$ V, $V_V = 2.0$ V, $I_P = 5.0$ μA, $I_V = 4.0$ mA, and supply $V_{CC} = 20.0$ V, calculate required timing resistor R_T and verify design bounds.
- Step 1: Calculate Target Oscillation Period (T): $T = \frac{1}{f_o} = \frac{1}{400\ \text{Hz}} = 2.5\ \text{ms} = 2.5 \times 10^{-3}$ s.
- Step 2: Calculate Required Timing Resistor (R_T):
  $T = R_T C_T \ln\left(\frac{1}{1-\eta}\right) \Rightarrow 2.5 \times 10^{-3} = R_T(0.1 \times 10^{-6}) \ln\left(\frac{1}{1-0.65}\right) = R_T(10^{-7}) \ln(2.857) =$
  $R_T(10^{-7})(1.0498) \Rightarrow R_T = \frac{2.5 \times 10^{-3}}{1.0498 \times 10^{-7}} \approx 23.81$ kΩ (standard 24 kΩ).
- Step 3: Calculate Upper Resistance Limit ($R_{T,max}$):
  $R_{T,max} = \frac{V_{CC} - V_P}{I_P} = \frac{20.0\ \text{V} - 13.7\ \text{V}}{5.0 \times 10^{-6}\ \text{A}} = \frac{6.3\ \text{V}}{5.0 \times 10^{-6}\ \text{A}} = 1.26$ MΩ.
- Step 4: Calculate Lower Resistance Limit ($R_{T,min}$):
  $R_{T,min} = \frac{V_{CC} - V_V}{I_V} = \frac{20.0\ \text{V} - 2.0\ \text{V}}{4.0 \times 10^{-3}\ \text{A}} = \frac{18.0\ \text{V}}{4.0 \times 10^{-3}\ \text{A}} = 4.5$ kΩ.
- Step 5: Verify Design Validity: $4.5\ \text{k}\Omega < 23.81\ \text{k}\Omega < 1.26\ \text{M}\Omega$ (Design is fully valid and stable).

Output Pulse Characteristics across Base-1 (R_1)

- Peak Trigger Voltage (V_{p1}): Peak pulse voltage appearing across R_1 during discharge: $V_{p1} \approx \frac{R_1}{R_1 + R_{B1,sat}}(V_P - V_V)$.
- Pulse Duration ($t_p|_{50\%}$): Determined by C_T discharge time constant: $t_p \approx (R_1 + R_{B1,sat})C_T$. Typically narrow ($1.0\ \mu s - 20.0\ \mu s$).
- Resistor Selection Guidelines: R_1 must be kept small ($20\ \Omega - 100\ \Omega$) to minimize quiescent DC voltage drop during OFF state while producing sufficient pulse amplitude ($1.0\ V - 3.0\ V$) to trigger SCR gates.
- Base-2 Resistor Selection: $R_2 \approx \frac{10000}{\eta V_{CC}}$ to stabilize peak firing voltage V_P across ambient temperature variations.

Application: SCR Phase-Control Triggering

- Synchronized Firing Topology: UJT relaxation oscillator powered by Zener-clamped full-wave rectified AC voltage (V_{zener}).
- Zero-Crossing Synchronization: At the end of each AC half-cycle, Zener voltage drops to zero, discharging C_T to zero and synchronizing oscillator timing with line frequency (50 Hz/60 Hz).
- Firing Angle Control (α): Adjusting variable timing resistor R_T alters capacitor charging rate, sweeping SCR trigger firing angle α smoothly from 0° to 180°.
- Industrial Applications: Light dimmers, motor speed control, electric heater regulators, and controlled AC-to-DC converters.

SCR Firing Angle Calculation Example

- Problem Statement: A UJT relaxation oscillator synchronized to a 50 Hz AC line ($T_{half} = 10.0$ ms) triggers an SCR. Given $C_T = 0.22\ \mu$F and $\eta = 0.632$, calculate timing resistor R_T required for firing angles: (a) $\alpha = 45^\circ$, (b) $\alpha = 90^\circ$.
- Step 1: Calculate Delay Time for $\alpha = 45^\circ$: $t_{d1} = \frac{45^\circ}{180^\circ} \times 10.0\ \text{ms} = 2.5\ \text{ms}$.
- Step 2: Solve for R_{T1} at $\alpha = 45^\circ$: Since $\eta = 0.632$, $\ln\left(\frac{1}{1-0.632}\right) = 1.00 \Rightarrow t_{d1} = R_{T1} C_T \Rightarrow R_{T1} = \frac{2.5 \times 10^{-3}\ \text{s}}{0.22 \times 10^{-6}\ \text{F}} \approx 11.36\ \text{k}\Omega$.
- Step 3: Calculate Delay Time for $\alpha = 90^\circ$: $t_{d2} = \frac{90^\circ}{180^\circ} \times 10.0\ \text{ms} = 5.0\ \text{ms}$.
- Step 4: Solve for R_{T2} at $\alpha = 90^\circ$: $R_{T2} = \frac{5.0 \times 10^{-3}\ \text{s}}{0.22 \times 10^{-6}\ \text{F}} \approx 22.73\ \text{k}\Omega$.

Linear Sawtooth Generation via Constant Current

- Non-Linearity Problem: Standard passive $R_T C_T$ charging produces an exponential curve ($V_E(t) = V_{CC}(1 - e^{-t/\tau})$), causing sweep non-linearity.
- Constant Current Charging Solution: Replace passive timing resistor R_T with a PNP transistor constant current source ($I_C = \frac{V_{CC} - V_B - V_{BE}}{R_E}$).
- Linear Voltage Ramp Equation: Capacitor charges linearly according to $V_E(t) = \frac{I_C}{C_T} \times t$.
- Linear Period Formula: $T = \frac{C_T(V_P - V_V)}{I_C} = \frac{C_T(\eta V_{CC} + V_D - V_V)}{I_C}$.
- Applications: Oscilloscope Cathode Ray Tube (CRT) time-base sweep generators and linear ramp analog-to-digital converters.

Comparison: UJT Relaxation vs. Op-Amp Astable

- Waveform Outputs: UJT (exponential/linear sawtooth across C_T + narrow trigger spikes across R_1); Op-Amp Astable (square wave output + exponential triangle across C).
- Component Count & Simplicity: UJT requires only 1 discrete 3-terminal transistor + 3 resistors + 1 capacitor; Op-Amp astable requires multi-transistor IC package.
- High Peak Current Discharge: UJT discharges C_T through collapsed channel ($R_{B1,sat} \approx 20\ \Omega$), delivering heavy peak current pulses (> 1 A) ideal for SCR triggering; Op-Amp output current is internally limited ($\sim 20 - 40$ mA).
- Frequency Range: UJT (up to ~ 500 kHz); Op-Amp Astable (up to several MHz).

Summary of UJT Relaxation Oscillator

- UJT Relaxation Oscillator converts DC supply into exponential sawtooth ramps (V_E) and sharp positive gate pulses (V_{B1}).
- Oscillation period $T = R_T C_T \ln\left(\frac{1}{1-\eta}\right) \approx R_T C_T$ (when $\eta \approx 0.632$).
- Timing resistance must be bounded within $\frac{V_{CC}-V_P}{I_P} > R_T > \frac{V_{CC}-V_V}{I_V}$ to ensure turn-ON and turn-OFF.
- Extensively applied in SCR/TRIAC phase control, linear time-base ramp generators, and pulse timing delays.

Formula Reference & Key Equations

- Oscillation Period: $T = R_T C_T \ln\left(\frac{1}{1-\eta}\right)$.
- Oscillation Frequency: $f_o = \frac{1}{T} = \frac{1}{R_T C_T \ln(1/(1-\eta))}$.
- Timing Resistance Bounds: $\frac{V_{CC}-V_P}{I_P} > R_T > \frac{V_{CC}-V_V}{I_V}$.
- Base-1 Peak Pulse Voltage: $V_{p1} \approx \frac{R_1}{R_1+R_{B1,sat}}(V_P - V_V)$.
- Linear Ramp Period (Current Source I_C): $T = \frac{C_T(V_P-V_V)}{I_C}$.