Eca (4321103) - Problem Solver

Antigravity AI

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To my students,
who constantly inspire me to find new analogies,
break down complex theories, and make learning
an engineered science.

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Preface

About this Book

Welcome to **Computer Networks**! This textbook is meticulously designed to serve as a comprehensive problem solver and study companion. It provides a robust and intuitive foundation in the core principles of this subject, bridging the gap between theoretical models and practical applications. A unique feature of this book is its focus on decoding complex concepts using clear, step-by-step methodologies and real-world analogies.

Target Audience

This book is intended for students and professionals looking to master the concepts of Computer Networks. Whether you are revising for exams, seeking to solidify your fundamental understanding, or looking for practical examples to clarify abstract concepts, this book has been structured to support your learning journey. It serves as an accessible guide designed to remove the fear of complex topics, replacing it with an appreciation for the underlying mechanics.

Scope and Coverage

The coverage is divided logically to follow standard academic curriculums. Each chapter focuses on key topics, breaking them down into digestible sections:

- **Theoretical Insights** – Core concepts explained intuitively.
- **Method Blocks** – Standardized, step-by-step procedures for solving specific types of problems.
- **Worked Examples** – Fully solved problems that apply the methods in practice.

We hope this resource proves invaluable in your studies and helps you achieve excellence in **Computer Networks**. Happy learning!

Acknowledgments

Writing a comprehensive book that connects the fundamental forces of Chemistry with practical engineering applications requires more than just academic knowledge—it requires a community of support. I would like to express my sincere gratitude to everyone who contributed to the realization of this project.

Specially, I extend my heartfelt gratitude to the **Department of Technical Education (DTE), Government of Gujarat**, and **Government Polytechnic, Palanpur**, for providing an environment that fosters innovation, academic rigor, and continuous professional development.

I am deeply thankful to my family for their unwavering patience and support during the countless hours spent researching, formatting, and refining these chapters.

Finally, my deepest appreciation goes to my students. Your curiosity, challenging questions, and continuous feedback are the true driving force behind the unique analogies and streamlined structure of this book. This textbook was engineered for you.

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About the Author

Milav Jayeshkumar Dabgar is an engineering educator and R&D professional with over 9 years of experience in electronics hardware development, embedded systems, AI/ML, and full-stack software engineering. He currently serves as a **Lecturer (Class - II) & Innovation Leader** at Government Polytechnic, Palanpur, under the Education Department of the Government of Gujarat.

Milav holds a Master of Engineering (ME) in Communication Systems from L.D. College of Engineering and a Bachelor of Engineering (BE) in Electronics & Communication. He is also currently pursuing a **BS in Data Science and Applications from IIT Madras**, where he has completed both the **Diploma in Programming** and the **Diploma in Data Science** with distinction.

Most recently, he completed the **AICTE QIP PG Certificate Program in Deep Learning from SVNIT Surat** with a **perfect 10/10 CGPA**, topping his batch.

A dedicated mentor, Milav has guided numerous student teams in securing over **INR 45 lakhs** in innovation funding, including INR 25 lakhs from Shark Tank India and INR 20 lakhs through iHub Gujarat, resulting in two student patents. He is recognized as an **NPTEL Evangelist** and **NPTEL Discipline Star** in Computer Science, reflecting his commitment to continuous learning and academic excellence.

His technical expertise spans from embedded systems (8051, STM32, Arduino) to modern web technologies (Next.js, Python, PostgreSQL) and Data Science (TensorFlow, PyTorch). Through this textbook, he aims to simplify complex Engineering Chemistry concepts by integrating relatable, real-world analogies drawn from modern tech and engineering landscapes.

Milav is also an active content creator, running a popular **YouTube channel** (@milav.dabgar) where he shares technical tutorials and academic resources. He maintains a personal blog and resource hub at milav.in and can be reached for professional collaborations on LinkedIn.

CHAPTER 1

Transistor Biasing Circuits and Thermal Stability

1.1 Biasing of Amplifier and Operating Point

Transistor biasing is the process of setting a specific direct current (DC) voltage and current level to establish the correct operating point (Q-point) for amplification. The Q-point is defined by the DC collector current (I_C) and the DC collector-emitter voltage (V_{CE}).

Methodology:

Operating Point Calculation To find the Q-point (I_C and V_{CE}) of a bipolar junction transistor (BJT) circuit:

1. **Apply Kirchhoff's Voltage Law (KVL) to the Base-Emitter loop:** Write the equation involving the base supply voltage, base resistor R_B, and the base-emitter voltage V_{BE}. For a silicon transistor, assume $V_{BE} = 0.7$ V.
2. **Solve for Base Current (I_B):** Rearrange the equation to isolate I_B.
3. **Calculate Collector Current (I_C):** Use the relationship $I_C = \beta I_B$, where β (or h_{FE}) is the common-emitter current gain.
4. **Apply KVL to the Collector-Emitter loop:** Write the equation involving the collector supply voltage V_{CC}, voltage drops across R_C (and R_E if present), and V_{CE}.
5. **Solve for V_{CE}:** Rearrange the equation to find the operating collector-emitter voltage.

The coordinate pair (V_{CE}, I_C) represents the Q-point.

Worked Example:

Determine Q-Point for a Fixed Bias Circuit A fixed bias circuit has $V_{CC} = 12$ V, $R_B = 240$ kΩ, $R_C = 2.2$ kΩ, and a silicon transistor with $\beta = 50$. Determine the operating point.

Step 1: Apply KVL to the base loop.

$$V_{CC} - I_B R_B - V_{BE} = 0$$

Step 2: Solve for I_B.

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\text{ V} - 0.7\text{ V}}{240\text{ k}\Omega} = \frac{11.3}{240 \times 10^3} = 47.08\,\mu\text{A}$$

Step 3: Calculate I_C.

$$I_C = \beta I_B = 50 \times 47.08\,\mu\text{A} = 2.35\text{ mA}$$

Step 4: Apply KVL to the collector loop and solve for V_{CE}.

$$V_{CC} - I_C R_C - V_{CE} = 0$$

$$V_{CE} = V_{CC} - I_C R_C = 12 \text{ V} - (2.35 \text{ mA} \times 2.2 \text{ k}\Omega) = 12 - 5.17 = 6.83 \text{ V}$$

Final Q-Point: $(6.83 \text{ V}, 2.35 \text{ mA})$

1.2 D.C. and A.C. Load Lines

The D.C. load line represents all possible DC operating points for a given circuit, defined by its saturation and cutoff limits. The A.C. load line accounts for the effective AC resistance seen by the collector, which includes external loads coupled via capacitors.

Methodology:

Constructing DC and AC Load Lines **Part A: DC Load Line**

1. **Find Cutoff Point (X-axis intercept):** Set $I_C = 0$. The maximum voltage is $V_{CE(cutoff)} = V_{CC}$.
2. **Find Saturation Point (Y-axis intercept):** Set $V_{CE} = 0$. The maximum current is $I_{C(sat)} = \frac{V_{CC}}{R_C + R_E}$.
3. Draw a straight line between $(V_{CC}, 0)$ and $(0, I_{C(sat)})$.

Part B: AC Load Line

1. **Calculate AC Collector Resistance (r_{ac}):** For a load R_L coupled via a capacitor to the collector, $r_{ac} = R_C \parallel R_L = \frac{R_C R_L}{R_C + R_L}$.
2. **Find AC Saturation Current:** $I_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_{ac}}$, where (V_{CEQ}, I_{CQ}) is the Q-point.
3. **Find AC Cutoff Voltage:** $V_{ce(cutoff)} = V_{CEQ} + I_{CQ} r_{ac}$.
4. Draw a line passing through the Q-point, intersecting the axes at $I_{c(sat)}$ and $V_{ce(cutoff)}$.

Worked Example:

Calculate Load Line Intercepts A biased transistor circuit has $V_{CC} = 15$ V, $R_C = 3$ kΩ, $R_E = 1$ kΩ, and an external AC load $R_L = 6$ kΩ coupled to the collector. The Q-point is computed as $V_{CEQ} = 7$ V and $I_{CQ} = 2$ mA. Calculate the DC and AC load line endpoints.

Step 1: DC Cutoff Point.

$$V_{CE(cutoff)} = V_{CC} = 15 \text{ V}$$

Point: $(15 \text{ V}, 0 \text{ mA})$

Step 2: DC Saturation Point.

$$I_{C(sat)} = \frac{V_{CC}}{R_C + R_E} = \frac{15}{3 \text{ k}\Omega + 1 \text{ k}\Omega} = \frac{15}{4 \text{ k}\Omega} = 3.75 \text{ mA}$$

Point: $(0 \text{ V}, 3.75 \text{ mA})$

Step 3: Calculate AC Collector Resistance.

$$r_{ac} = R_C \parallel R_L = \frac{3 \text{ k}\Omega \times 6 \text{ k}\Omega}{3 \text{ k}\Omega + 6 \text{ k}\Omega} = \frac{18}{9} = 2 \text{ k}\Omega$$

Step 4: AC Saturation Point.

$$I_{c(sat)} = I_{CQ} + \frac{V_{CEQ}}{r_{ac}} = 2 \text{ mA} + \frac{7 \text{ V}}{2 \text{ k}\Omega} = 2 + 3.5 = 5.5 \text{ mA}$$

Point: $(0 \text{ V}, 5.5 \text{ mA})$

Step 5: AC Cutoff Point.

$$V_{ce(cutoff)} = V_{CEQ} + I_{CQ} r_{ac} = 7 \text{ V} + (2 \text{ mA} \times 2 \text{ k}\Omega) = 7 + 4 = 11 \text{ V}$$

Point: $(11 \text{ V}, 0 \text{ mA})$

1.3 Biasing Methods

Several circuit configurations are used to bias a transistor. The most common robust method is Voltage Divider Bias (or Self-Bias), which makes the Q-point largely independent of β.

Methodology:

Voltage Divider Bias Analysis To accurately analyze a voltage divider bias circuit (R_1 and R_2 forming a divider at the base, R_E at the emitter):

1. **Find Thevenin Equivalent Voltage (V_{TH}):**

$$V_{TH} = V_{CC}\frac{R_2}{R_1 + R_2}$$

2. **Find Thevenin Equivalent Resistance (R_{TH}):**

$$R_{TH} = \frac{R_1 R_2}{R_1 + R_2}$$

3. **Calculate Base Current (I_B):** Apply KVL to the Thevenin equivalent base-emitter loop:

$$I_B = \frac{V_{TH} - V_{BE}}{R_{TH} + (\beta + 1)R_E}$$

4. **Determine I_C and V_{CE}:**

$$I_C = \beta I_B \quad \text{and} \quad V_{CE} = V_{CC} - I_C R_C - I_E R_E \approx V_{CC} - I_C(R_C + R_E)$$

Worked Example:

Analyze Voltage Divider Circuit Given a voltage divider circuit with $V_{CC} = 20$ V, $R_1 = 39$ kΩ, $R_2 = 3.9$ kΩ, $R_C = 10$ kΩ, $R_E = 1.5$ kΩ, and $\beta = 140$. Find I_C and V_{CE}. Assume $V_{BE} = 0.7$ V.

Step 1: Calculate V_{TH} and R_{TH}.

$$V_{TH} = 20 \times \frac{3.9\text{ k}}{39\text{ k} + 3.9\text{ k}} = 20 \times \frac{3.9}{42.9} = 1.82\text{ V}$$

$$R_{TH} = \frac{39\text{ k} \times 3.9\text{ k}}{39\text{ k} + 3.9\text{ k}} = 3.55\text{ k}\Omega$$

Step 2: Calculate I_B.

$$I_B = \frac{1.82\text{ V} - 0.7\text{ V}}{3.55\text{ k}\Omega + (141)(1.5\text{ k}\Omega)} = \frac{1.12}{3.55\text{ k} + 211.5\text{ k}} = \frac{1.12}{215.05 \times 10^3} = 5.21\,\mu\text{A}$$

Step 3: Calculate I_C and V_{CE}.

$$I_C = 140 \times 5.21\,\mu\text{A} = 0.73\text{ mA}$$

$$V_{CE} = 20 - 0.73\text{ mA} \times (10\text{ k}\Omega + 1.5\text{ k}\Omega) = 20 - 0.73(11.5) = 20 - 8.4 = 11.6\text{ V}$$

Result: Q-point is $(11.6\text{ V}, 0.73\text{ mA})$.

1.4 Stability Factor

The stability factor S measures the sensitivity of the collector current I_C to changes in the reverse saturation current I_{CO} due to temperature variations. A lower S indicates better thermal stability.

Methodology:

Calculation of Stability Factor S The general formula for stability factor is:

$$S = \frac{\partial I_C}{\partial I_{CO}} = \frac{1+\beta}{1-\beta\left(\frac{\partial I_B}{\partial I_C}\right)}$$

To compute S for a specific configuration:

1. **Fixed Bias:** $\frac{\partial I_B}{\partial I_C} = 0 \implies S = 1+\beta$ (Poor stability).
2. **Collector-to-Base Bias:** $S = \frac{1+\beta}{1+\beta\left(\frac{R_C}{R_C+R_B}\right)}$.
3. **Voltage Divider Bias:** $S = \frac{(1+\beta)(R_{TH}+R_E)}{R_{TH}+(1+\beta)R_E}$.

Worked Example:

Evaluate Stability Factor S Calculate the stability factor S for the voltage divider circuit from the previous example, where $R_{TH} = 3.55\ \text{k}\Omega$, $R_E = 1.5\ \text{k}\Omega$, and $\beta = 140$. Compare it to the stability factor if a fixed bias circuit was used with the same β.

Step 1: Evaluate S for Voltage Divider Bias.

$$S = \frac{(1+140)(3.55\ \text{k}+1.5\ \text{k})}{3.55\ \text{k}+(1+140)1.5\ \text{k}} = \frac{141\times 5.05\ \text{k}}{3.55\ \text{k}+211.5\ \text{k}}$$

$$S = \frac{712.05}{215.05} = 3.31$$

Step 2: Evaluate S for Fixed Bias.

$$S_{fixed} = 1+\beta = 1+140 = 141$$

Conclusion: The voltage divider bias provides excellent stability ($S = 3.31$) compared to fixed bias ($S = 141$).

1.5 Compensation Techniques for Bias Stability

When biasing circuits alone cannot provide sufficient stabilization against temperature changes, temperature-sensitive components like diodes, thermistors, or sensistors are added.

Methodology:

Thermistor Compensation Calculation A thermistor has a negative temperature coefficient (NTC). When placed in parallel with R_2 in a voltage divider bias circuit:

1. **Calculate equivalent resistance at room temperature (T_1):** $R_{2(eq1)} = R_2 \parallel R_{thermistor}(T_1)$. Use this to compute I_{C1}.
2. **Calculate equivalent resistance at elevated temperature (T_2):** $R_{2(eq2)} = R_2 \parallel R_{thermistor}(T_2)$.
3. **Recalculate I_C:** Use the new $R_{2(eq2)}$ to find the new V_{TH} and I_{C2}. The drop in $R_{2(eq)}$ reduces V_{TH}, lowering I_B and opposing the thermal increase in I_C.

Worked Example:

Calculate Compensated Voltage Drift A bias circuit produces a Thevenin base voltage $V_{TH} = 2.0$ V at 25°C. Due to temperature rise to 75°C, the transistor's I_C inherently tends to increase. A compensating

NTC thermistor is connected across the divider such that at 75°C, the effective Thevenin voltage drops to $V'_{TH} = 1.85$ V. If $R_{TH} = 4$ kΩ, $R_E = 2$ kΩ, $\beta = 100$, and V_{BE} drops by 2 mV/°C, calculate the base currents at 25°C and 75°C.

Step 1: Calculate initial base current at 25°C. $V_{BE} = 0.7$ V.

$$I_{B1} = \frac{2.0 \text{ V} - 0.7 \text{ V}}{4 \text{ k}\Omega + (101)(2 \text{ k}\Omega)} = \frac{1.3}{206 \text{ k}} = 6.31\,\mu\text{A}$$

Step 2: Determine parameters at 75°C. $\Delta T = 75 - 25 = 50$°C. New $V_{BE} = 0.7 \text{ V} - (50 \times 0.002 \text{ V}) = 0.6$ V. New $V'_{TH} = 1.85$ V.

Step 3: Calculate new base current at 75°C.

$$I_{B2} = \frac{1.85 \text{ V} - 0.6 \text{ V}}{206 \text{ k}\Omega} = \frac{1.25}{206 \text{ k}} = 6.07\,\mu\text{A}$$

Conclusion: The thermistor actively reduces I_B (from 6.31 μA to 6.07 μA) to offset the increase in β and leakage current at high temperatures.

1.6 Thermal Runaway and Thermal Stability

Thermal runaway occurs when an increase in temperature causes an increase in collector current, leading to more power dissipation, which further increases temperature, ultimately destroying the transistor.

Methodology:

Thermal Stability Condition To prevent thermal runaway, the rate at which heat is removed from the junction must exceed the rate at which internal heat dissipation increases with temperature:

$$\frac{\partial P_D}{\partial T_j} < \frac{1}{\theta}$$

Where:

- $P_D = V_{CE} I_C$ is the DC power dissipated at the collector junction.
- T_j is the junction temperature.
- θ is the total thermal resistance from junction to ambient (in °C/W).

In practical terms, for a circuit with a DC load $R_{DC} = R_C + R_E$, a circuit is unconditionally stable if $V_{CE} < \frac{V_{CC}}{2}$.

Worked Example:

Determine Thermal Stability Requirement A transistor dissipates power P_D. The mathematical model for its power generation yields $\frac{\partial P_D}{\partial T_j} = 0.015$ W/°C. Determine the maximum allowable thermal resistance θ to ensure the transistor does not suffer thermal runaway.

Step 1: Apply the thermal stability criterion.

$$\frac{\partial P_D}{\partial T_j} < \frac{1}{\theta}$$

Step 2: Substitute the known rate of power variation.

$$0.015 < \frac{1}{\theta}$$

Step 3: Solve for θ.

$$\theta < \frac{1}{0.015}$$

$$\theta < 66.67 \text{ °C/W}$$

Conclusion: The total thermal resistance must be strictly less than 66.67 °C/W to guarantee thermal stability.

1.7 Thermal Resistance and Heat Sinks

A heat sink is a mechanical device attached to a transistor to increase the surface area and decrease the thermal resistance to ambient air, aiding heat dissipation.

Methodology:

Thermal Resistance and Power Dissipation Calculations The fundamental thermal equation analogous to Ohm's Law ($V = IR$) is:

$$T_j = T_A + P_D(\theta_{JC} + \theta_{CS} + \theta_{SA})$$

Where:

- T_j: Maximum junction temperature (°C)
- T_A: Ambient temperature (°C)
- P_D: Power dissipation (Watts)
- θ_{JC}: Thermal resistance, junction-to-case
- θ_{CS}: Thermal resistance, case-to-sink (insulator/thermal paste)
- θ_{SA}: Thermal resistance, sink-to-ambient (depends on Heat Sink type)

Heat Sink Selection Algorithm:

1. Calculate the total required thermal resistance: $\theta_{total} = \frac{T_j - T_A}{P_D}$.
2. Subtract intrinsic resistances to find required sink-to-ambient rating: $\theta_{SA(max)} = \theta_{total} - \theta_{JC} - \theta_{CS}$.
3. Select a heat sink type (e.g., Stamped metal ≈ 10-50°C/W, Extruded fin ≈ 1-10°C/W) such that its specific $\theta_{SA} \leq \theta_{SA(max)}$.

Worked Example:

Calculate Required Heat Sink Thermal Resistance A power transistor dissipates 15 W of power. The maximum junction temperature is 150°C, and the maximum ambient temperature is 50°C. The transistor has $\theta_{JC} = 1.5$ °C/W, and the mica insulator and thermal paste provide $\theta_{CS} = 0.5$ °C/W. Calculate the required thermal resistance of the heat sink (θ_{SA}) and suggest a suitable type.

Step 1: Calculate maximum allowable total thermal resistance.

$$\theta_{total} = \frac{T_j - T_A}{P_D} = \frac{150°\text{C} - 50°\text{C}}{15 \text{ W}} = \frac{100}{15} = 6.67 \text{ °C/W}$$

Step 2: Calculate maximum allowable θ_{SA}.

$$\theta_{total} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

$$6.67 = 1.5 + 0.5 + \theta_{SA}$$

$$\theta_{SA} = 6.67 - 2.0 = 4.67 \text{ °C/W}$$

Step 3: Conclusion and Heat Sink Selection. The heat sink must have a thermal resistance of 4.67 °C/W or lower. A heavy-duty extruded aluminum finned heat sink is typically required for values in this range, as simple stamped metal heat sinks generally have higher thermal resistances.

CHAPTER 2

Frequency Response of Transistor Amplifier

2.1 Gain Bandwidth and Gain-Bandwidth Product

Methodology:

Calculation of Gain and Bandwidth The performance of an amplifier is evaluated using its gain, bandwidth, and their product.

1. **Voltage Gain (A_v)**: The ratio of output voltage to input voltage.

$$A_v = \frac{V_{out}}{V_{in}}$$

2. **Power Gain (A_p)**: The ratio of output power to input power.

$$A_p = \frac{P_{out}}{P_{in}}$$

3. **Gain in Decibels (dB)**: Gain is often expressed in logarithmic scale.

$$A_{v(dB)} = 20 \log_{10}(A_v)$$

$$A_{p(dB)} = 10 \log_{10}(A_p)$$

4. **Bandwidth (BW)**: The range of frequencies over which the amplifier gain drops by no more than 3 dB (or $1/\sqrt{2}$ of its mid-band maximum).

$$BW = f_H - f_L$$

where f_H is the upper cut-off frequency and f_L is the lower cut-off frequency.

5. **Gain-Bandwidth Product (GBW)**: A constant parameter for a given amplifier configuration that represents the trade-off between gain and bandwidth.

$$GBW = A_{mid} \times BW$$

If $f_L \ll f_H$, then $BW \approx f_H$, and $GBW \approx A_{mid} \times f_H$.

Worked Example:

Determining Amplifier Bandwidth and Gain An amplifier has a mid-band voltage gain of 100. Its lower cut-off frequency is 50 Hz and upper cut-off frequency is 20 kHz. Calculate: 1. Mid-band gain in dB 2. Bandwidth 3. Gain-Bandwidth Product 4. The voltage gain at the cut-off frequencies.

Solution:

1. **Mid-band gain in dB**:
$$A_{v(dB)} = 20 \log_{10}(100) = 20 \times 2 = 40 \text{ dB}$$

2. **Bandwidth (BW)**:
$$BW = f_H - f_L = 20000 \text{ Hz} - 50 \text{ Hz} = 19950 \text{ Hz} = 19.95 \text{ kHz}$$

3. **Gain-Bandwidth Product (GBW)**:
$$GBW = A_{mid} \times BW = 100 \times 19950 = 1.995 \times 10^6 \text{ Hz} = 1.995 \text{ MHz}$$

4. **Gain at Cut-off Frequencies**: At cut-off frequencies (f_L and f_H), the gain drops to $1/\sqrt{2}$ of the mid-band gain.
$$A_{cutoff} = \frac{100}{\sqrt{2}} \approx \frac{100}{1.414} \approx 70.7$$
In decibels, the gain drops by 3 dB, so it is 40 dB − 3 dB = 37 dB.

2.2 Effect of Emitter Bypass and Coupling Capacitors

Methodology:

Calculating Lower Cut-off Frequencies Coupling and bypass capacitors in an amplifier circuit act as short circuits at mid and high frequencies but introduce high-pass filter effects at low frequencies. This dictates the lower cut-off frequency (f_L).

1. **Input Coupling Capacitor (C_{c1})**: Forms a high-pass filter with the equivalent input resistance (R_{in}).
$$f_{L1} = \frac{1}{2\pi R_{in} C_{c1}}$$

2. **Output Coupling Capacitor (C_{c2})**: Forms a high-pass filter with the equivalent output resistance (R_{out}) and load resistance (R_L).
$$f_{L2} = \frac{1}{2\pi (R_{out} + R_L) C_{c2}}$$

3. **Emitter Bypass Capacitor (C_E)**: Determines the low-frequency limit caused by emitter degeneration.
$$f_{LE} = \frac{1}{2\pi R_{eq} C_E}$$
where R_{eq} is the Thevenin resistance seen by C_E, often approximated as $R_E \parallel r_e$ (for basic analysis).

4. **Dominant Lower Cut-off Frequency**: The highest among f_{L1}, f_{L2}, and f_{LE} dominates the low-frequency response and becomes the overall f_L.

Worked Example:

Evaluating Capacitor Effects on Lower Cut-off A single-stage Common Emitter (CE) amplifier has the following parameters: $R_{in} = 2$ kΩ, $C_{c1} = 10$ μF, $R_{out} = 4$ kΩ, $R_L = 10$ kΩ, $C_{c2} = 5$ μF, R_{eq} (seen by C_E) = 20 Ω, and $C_E = 100$ μF. Find the dominant lower cut-off frequency.
Solution:

1. **Calculate f_{L1} due to C_{c1}**:
$$f_{L1} = \frac{1}{2\pi R_{in} C_{c1}} = \frac{1}{2\pi \times (2000) \times (10 \times 10^{-6})}$$

$$f_{L1} = \frac{1}{0.1256} \approx 7.96 \text{ Hz}$$

2. **Calculate f_{L2} due to C_{c2}:**

$$f_{L2} = \frac{1}{2\pi(R_{out} + R_L)C_{c2}} = \frac{1}{2\pi \times (4000 + 10000) \times (5 \times 10^{-6})}$$

$$f_{L2} = \frac{1}{2\pi \times 14000 \times (5 \times 10^{-6})} = \frac{1}{0.4398} \approx 2.27 \text{ Hz}$$

3. **Calculate f_{LE} due to C_E:**

$$f_{LE} = \frac{1}{2\pi R_{eq} C_E} = \frac{1}{2\pi \times 20 \times (100 \times 10^{-6})}$$

$$f_{LE} = \frac{1}{0.01256} \approx 79.6 \text{ Hz}$$

4. **Dominant Frequency**: The overall lower cut-off frequency f_L is the maximum of the three calculated frequencies.

$$f_L \approx \max(7.96 \text{ Hz}, 2.27 \text{ Hz}, 79.6 \text{ Hz}) = 79.6 \text{ Hz}$$

2.3 Frequency Response of Single Stage Amplifier

Methodology:

Determining High Frequency Response The high-frequency roll-off of an amplifier is caused by internal device capacitances (junction capacitances) and stray wiring capacitances, which act as low-pass filters.

1. **Miller Effect**: A feedback capacitance (C_{bc} or C_μ) between output and input is reflected to the input multiplied by the gain.

$$C_{Miller} = C_{bc}(1 + |A_v|)$$

2. **Total Input Capacitance**:

$$C_{in(total)} = C_{be} + C_{Miller} + C_{stray(in)}$$

3. **Upper Cut-off Frequency (f_H)**: Governed by the input circuit time constant.

$$f_H = \frac{1}{2\pi R_{s(th)} C_{in(total)}}$$

where $R_{s(th)}$ is the Thevenin equivalent resistance seen at the input (source resistance parallel with input resistance).

Worked Example:

Calculation of Upper Cut-off Frequency A CE amplifier has a mid-band gain $|A_v| = 50$, base-emitter capacitance $C_{be} = 20$ pF, and base-collector capacitance $C_{bc} = 5$ pF. The Thevenin resistance at the input is $R_{s(th)} = 1$ kΩ. Ignoring stray capacitance, calculate the upper cut-off frequency.

Solution:

1. **Calculate Miller Capacitance**:

$$C_{Miller} = C_{bc}(1 + |A_v|) = 5 \text{ pF} \times (1 + 50) = 5 \text{ pF} \times 51 = 255 \text{ pF}$$

2. **Calculate Total Input Capacitance**:

$$C_{in(total)} = C_{be} + C_{Miller} = 20 \text{ pF} + 255 \text{ pF} = 275 \text{ pF}$$

3. **Calculate Upper Cut-off Frequency (f_H)**:

$$f_H = \frac{1}{2\pi R_{s(th)} C_{in(total)}} = \frac{1}{2\pi \times 1000 \times (275 \times 10^{-12})}$$

$$f_H = \frac{1}{1.728 \times 10^{-6}} \approx 578703 \text{ Hz} \approx 578.7 \text{ kHz}$$

2.4 Coupling Techniques

Methodology:

Evaluation of Multistage Coupling Methods Different coupling methods affect the gain, frequency response, and impedance matching between stages.

1. **RC Coupling**: Most common. Uses resistors and capacitors. Blocks DC, passing AC. Bandwidth is limited by coupling capacitors at low frequencies and parasitic capacitors at high frequencies.
2. **Transformer Coupling**: Uses a transformer. Excellent for impedance matching to maximize power transfer.

   $$R_{in(reflected)} = n^2 R_L = \left(\frac{N_1}{N_2}\right)^2 R_L$$

   Frequency response is poor due to transformer inductance and stray capacitance (bulky and poor at very low/high frequencies).
3. **Direct Coupling**: No coupling components. DC is passed along with AC. Ideal for very low frequency (including DC, $f_L = 0$ Hz) amplification. However, it suffers from high thermal drift.
4. **LC (Tuned) Coupling**: Uses inductors and capacitors tuned to a specific frequency. Used in RF amplifiers. Bandwidth is very narrow (selective).

Worked Example:

Impedance Matching via Transformer Coupling An amplifier has an output impedance of 4 kΩ and needs to drive an 8 Ω speaker using a matching transformer. Calculate the required turns ratio (N_1/N_2) for maximum power transfer.
Solution:

1. For maximum power transfer, the reflected impedance ($R_{in(reflected)}$) must equal the amplifier's output impedance.

   $$R_{in(reflected)} = 4000 \ \Omega$$

2. **Apply the impedance matching formula**:

   $$R_{in(reflected)} = \left(\frac{N_1}{N_2}\right)^2 \times R_L$$

   $$4000 = \left(\frac{N_1}{N_2}\right)^2 \times 8$$

3. **Solve for the turns ratio (n)**:

   $$\left(\frac{N_1}{N_2}\right)^2 = \frac{4000}{8} = 500$$

$$\frac{N_1}{N_2} = \sqrt{500} \approx 22.36$$

The required turns ratio is approximately 22.36 : 1.

2.5 Frequency Response of Two Stage RC Coupled Amplifier

Methodology:

Analysis of Cascaded RC Coupled Amplifiers When multiple identical amplifier stages are cascaded, the overall gain increases, but the bandwidth shrinks.

1. **Overall Voltage Gain**:

$$A_{v(total)} = A_{v1} \times A_{v2} \times \cdots \times A_{vn}$$

In decibels:

$$A_{v(total)\text{ dB}} = A_{v1(\text{dB})} + A_{v2(\text{dB})} + \cdots + A_{vn(\text{dB})}$$

2. **Bandwidth Shrinkage for Identical Stages**: For n identical cascaded stages with lower and upper cut-off frequencies f_L and f_H:

- **Overall Lower Cut-off Frequency (f_{Ln})**: Increases as stages are added.

$$f_{Ln} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$

- **Overall Upper Cut-off Frequency (f_{Hn})**: Decreases as stages are added.

$$f_{Hn} = f_H \times \sqrt{2^{1/n} - 1}$$

3. **Overall Bandwidth**:

$$BW_{total} = f_{Hn} - f_{Ln}$$

Worked Example:

Calculating Gain and Bandwidth Shrinkage for a Two Stage Amplifier A single stage RC coupled amplifier has a voltage gain of 40, a lower cut-off frequency of 40 Hz, and an upper cut-off frequency of 2 MHz. Two such identical stages are cascaded. Calculate: 1. Overall voltage gain. 2. Overall lower cut-off frequency. 3. Overall upper cut-off frequency. 4. Overall bandwidth.

Solution:

1. **Overall Voltage Gain**:

$$A_{v(total)} = A_{v1} \times A_{v2} = 40 \times 40 = 1600$$

In decibels:

$$A_{v(total)\text{ dB}} = 20 \log_{10}(1600) \approx 64.08 \text{ dB}$$

2. **Overall Lower Cut-off Frequency (f_{L2})**: For $n = 2$ stages, the shrinkage factor is $\sqrt{2^{1/2} - 1} = \sqrt{\sqrt{2} - 1} = \sqrt{1.414 - 1} = \sqrt{0.414} \approx 0.643$.

$$f_{L2} = \frac{f_L}{\sqrt{2^{1/2} - 1}} = \frac{40}{0.643} \approx 62.2 \text{ Hz}$$

3. **Overall Upper Cut-off Frequency (f_{H2})**:

$$f_{H2} = f_H \times \sqrt{2^{1/2} - 1} = 2 \text{ MHz} \times 0.643 = 1.286 \text{ MHz}$$

4. **Overall Bandwidth**:

$$BW_{total} = f_{H2} - f_{L2} = 1286000 \text{ Hz} - 62.2 \text{ Hz} \approx 1.286 \text{ MHz}$$

Notice that the cascading of stages drastically increased the gain but noticeably reduced the overall bandwidth.

CHAPTER 3
Hybrid Parameters

3.1 h-parameters of a Two-Port Network

A two-port network can be completely characterized by a set of four parameters known as hybrid parameters or h-parameters. These are widely used because they are easily measurable and particularly suited for describing transistor behavior.

The fundamental equations for h-parameters in terms of input voltage (V_1), input current (I_1), output voltage (V_2), and output current (I_2) are:

$$V_1 = h_{11}I_1 + h_{12}V_2 \tag{3.1}$$
$$I_2 = h_{21}I_1 + h_{22}V_2 \tag{3.2}$$

Methodology:

Determining h-parameters of a Network To find the h-parameters of any resistive two-port network, use the following procedure:

1. **Short-Circuit the Output Port ($V_2 = 0$):** Connect a short across the output terminals. Apply a voltage V_1 at the input.
2. **Calculate h_{11} and h_{21}:**
   - Input Impedance: $h_{11} = \frac{V_1}{I_1}\Big|_{V_2=0}$ (in Ohms Ω)
   - Forward Current Gain: $h_{21} = \frac{I_2}{I_1}\Big|_{V_2=0}$ (dimensionless)
3. **Open-Circuit the Input Port ($I_1 = 0$):** Leave the input terminals open. Apply a voltage V_2 at the output.
4. **Calculate h_{12} and h_{22}:**
   - Reverse Voltage Gain: $h_{12} = \frac{V_1}{V_2}\Big|_{I_1=0}$ (dimensionless)
   - Output Admittance: $h_{22} = \frac{I_2}{V_2}\Big|_{I_1=0}$ (in Siemens S or Mho $\mho$)

Worked Example:

Calculate h-parameters for a T-Network Find the h-parameters for a T-network consisting of two series resistors $R_1 = 10\,\Omega$ and $R_2 = 20\,\Omega$ and a shunt resistor $R_3 = 30\,\Omega$ connected between the common terminals. **Step 1: Short the output port ($V_2 = 0$) and apply V_1.** When the output is shorted, R_2 is in parallel with the short circuit path, meaning R_3 and R_2 are in parallel. The input impedance is $h_{11} = R_1 + (R_2 \parallel R_3)$.

$$h_{11} = 10 + \frac{20 \times 30}{20 + 30} = 10 + \frac{600}{50} = 10 + 12 = 22\,\Omega$$

Now find I_2. The current I_1 divides between R_3 and R_2. Using the current divider rule, the current flowing

through R_2 (which is $-I_2$ because I_2 enters port 2) is:

$$-I_2 = I_1 \left(\frac{R_3}{R_2 + R_3} \right)$$

$$I_2 = -I_1 \left(\frac{30}{20 + 30} \right) = -0.6 I_1$$

Thus, $h_{21} = \frac{I_2}{I_1} = -0.6$.
Step 2: Open the input port ($I_1 = 0$) and apply V_2. With port 1 open, no current flows through R_1. The voltage at port 1 (V_1) is equal to the voltage drop across R_3. Using the voltage divider rule, the voltage across R_3 is:

$$V_1 = V_2 \left(\frac{R_3}{R_2 + R_3} \right) = V_2 \left(\frac{30}{20 + 30} \right) = 0.6 V_2$$

Thus, $h_{12} = \frac{V_1}{V_2} = 0.6$.
The admittance at the output port is determined by the total series resistance of R_2 and R_3.

$$h_{22} = \frac{I_2}{V_2} = \frac{1}{R_2 + R_3} = \frac{1}{50} = 0.02\, S$$

Final Answer: $h_{11} = 22\,\Omega$, $h_{12} = 0.6$, $h_{21} = -0.6$, $h_{22} = 0.02\, S$.

3.2 h-parameters for Transistor Amplifier

A transistor can be treated as a two-port network. The h-parameters for a transistor depend heavily on its configuration (Common Emitter, Common Base, or Common Collector). For a Common Emitter (CE) amplifier, the input is applied between the base and emitter (V_{be}, I_b) and the output is taken between the collector and emitter (V_{ce}, I_c).

The standard h-parameter equations for a CE configuration are given by:

$$V_{be} = h_{ie} I_b + h_{re} V_{ce} \tag{3.3}$$

$$I_c = h_{fe} I_b + h_{oe} V_{ce} \tag{3.4}$$

Methodology:

Notation of Transistor h-parameters The subscripts in transistor h-parameters follow a standard naming convention:

1. **First Subscript (Parameter Type):**
   - i: Input impedance (h_{11})
   - r: Reverse voltage transfer ratio (h_{12})
   - f: Forward current transfer ratio (h_{21})
   - o: Output admittance (h_{22})
2. **Second Subscript (Configuration):**
   - e: Common Emitter (e.g., h_{ie})
   - b: Common Base (e.g., h_{ib})
   - c: Common Collector (e.g., h_{ic})

Worked Example:

Identify Transistor Parameters A Common Emitter transistor has the following two-port parameters extracted from measurements: $h_{11} = 1.2\,\text{k}\Omega$, $h_{12} = 2 \times 10^{-4}$, $h_{21} = 60$, and $h_{22} = 25\,\mu\text{S}$. Write the corresponding CE transistor h-parameters using standard nomenclature.

Step 1: Match general h-parameters to specific transistor notation.

- h_{11} corresponds to input impedance: $h_{ie} = 1.2\,\text{k}\Omega$
- h_{12} corresponds to reverse voltage ratio: $h_{re} = 2 \times 10^{-4}$
- h_{21} corresponds to forward current ratio: $h_{fe} = 60$
- h_{22} corresponds to output admittance: $h_{oe} = 25\,\mu\text{S}$

Final Answer: $h_{ie} = 1.2\,\text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 60$, $h_{oe} = 25\,\mu\text{S}$.

3.3 Analysis of Transistor Amplifier using h-parameters

The exact analysis of a transistor amplifier involves calculating the Current Gain (A_i), Input Impedance (Z_i), Voltage Gain (A_v), and Output Impedance (Z_o) directly from the h-parameter equivalent circuit equations.

Methodology:

Exact Analysis of Transistor Amplifier Given an amplifier with load resistance R_L, source resistance R_s, and standard parameters (h_i, h_r, h_f, h_o):

1. **Current Gain (A_i):** The ratio of output current to input current.

$$A_i = \frac{-h_f}{1 + h_o R_L}$$

2. **Input Impedance (Z_i):** The total resistance looking into the input terminals.

$$Z_i = h_i + h_r A_i R_L$$

3. **Voltage Gain (A_v):** The ratio of output voltage to input voltage.

$$A_v = \frac{A_i R_L}{Z_i}$$

4. **Output Admittance (Y_o) and Impedance (Z_o):** Looking into the output terminals with the source voltage reduced to zero.

$$Y_o = h_o - \frac{h_f h_r}{h_i + R_s}$$

$$Z_o = \frac{1}{Y_o}$$

Worked Example:

Calculate Amplifier Performance Parameters A CE amplifier has the following parameters: $h_{ie} = 1.5\,\text{k}\Omega$, $h_{re} = 3 \times 10^{-4}$, $h_{fe} = 50$, $h_{oe} = 25\,\mu\text{S}$. The amplifier is connected to a load $R_L = 10\,\text{k}\Omega$ and driven by a source with internal resistance $R_s = 1\,\text{k}\Omega$. Calculate A_i, Z_i, A_v, and Z_o.
Step 1: Calculate Current Gain (A_i) Using the formula $A_i = \frac{-h_{fe}}{1+h_{oe}R_L}$:

$$h_{oe}R_L = (25 \times 10^{-6}) \times (10 \times 10^{3}) = 0.25$$

$$A_i = \frac{-50}{1 + 0.25} = \frac{-50}{1.25} = -40$$

Step 2: Calculate Input Impedance (Z_i) Using the formula $Z_i = h_{ie} + h_{re}A_iR_L$:

$$Z_i = 1500 + (3 \times 10^{-4}) \times (-40) \times 10000$$

$$Z_i = 1500 - 120 = 1380\,\Omega = 1.38\,\text{k}\Omega$$

Step 3: Calculate Voltage Gain (A_v) Using the formula $A_v = \frac{A_i R_L}{Z_i}$:

$$A_v = \frac{-40 \times 10000}{1380} = -289.86$$

Step 4: Calculate Output Admittance (Y_o) and Impedance (Z_o) Using the formula $Y_o = h_{oe} - \frac{h_{fe}h_{re}}{h_{ie}+R_s}$:

$$Y_o = 25 \times 10^{-6} - \frac{50 \times 3 \times 10^{-4}}{1500 + 1000}$$

$$Y_o = 25 \times 10^{-6} - \frac{0.015}{2500} = (25 - 6) \times 10^{-6} = 19\,\mu\text{S}$$

$$Z_o = \frac{1}{Y_o} = \frac{1}{19 \times 10^{-6}} = 52.63\,\text{k}\Omega$$

Final Answer: $A_i = -40$, $Z_i = 1.38\,\text{k}\Omega$, $A_v = -289.86$, $Z_o = 52.63\,\text{k}\Omega$.

Methodology:

Approximate Analysis of Transistor Amplifier In many practical applications, h_{re} is very small ($h_{re} \approx 0$) and $h_{oe}R_L$ is much less than 1 ($h_{oe}R_L \ll 1$). This leads to highly simplified formulas for quick performance estimation:

1. **Approximate Current Gain (A_i):**
$$A_i \approx -h_{fe}$$
2. **Approximate Input Impedance (Z_i):**
$$Z_i \approx h_{ie}$$
3. **Approximate Voltage Gain (A_v):**
$$A_v \approx \frac{-h_{fe}R_L}{h_{ie}}$$
4. **Approximate Output Impedance (Z_o):**
$$Z_o \approx \frac{1}{h_{oe}} \quad \text{or} \quad Z_o \approx \infty$$

Worked Example:

Calculate Amplifier Performance using Approximate Analysis Using the approximate method, calculate A_i, Z_i, A_v, and Z_o for a CE amplifier with $h_{ie} = 2\,\text{k}\Omega$, $h_{fe} = 100$, $h_{re} \approx 0$, $h_{oe} = 20\,\mu\text{S}$, and $R_L = 5\,\text{k}\Omega$. Compare the approximated voltage gain with the exact calculation.

Step 1: Calculate Approximate Values

- $A_i \approx -h_{fe} = -100$
- $Z_i \approx h_{ie} = 2\,\text{k}\Omega$
- $A_v \approx \frac{-h_{fe}R_L}{h_{ie}} = \frac{-100\times5000}{2000} = -250$
- $Z_o \approx \frac{1}{h_{oe}} = \frac{1}{20\times10^{-6}} = 50\,\text{k}\Omega$

Step 2: Calculate Exact Voltage Gain for Comparison First, find exact A_i:

$$A_i = \frac{-h_{fe}}{1 + h_{oe}R_L} = \frac{-100}{1 + (20 \times 10^{-6} \times 5000)} = \frac{-100}{1.1} = -90.9$$

Next, find exact Z_i. Since $h_{re} \approx 0$:

$$Z_i = h_{ie} + h_{re} A_i R_L = 2000 + 0 = 2\,\text{k}\Omega$$

Now, calculate exact A_v:

$$A_v = \frac{A_i R_L}{Z_i} = \frac{-90.9 \times 5000}{2000} = -227.25$$

Conclusion: The approximate method yields a voltage gain of -250, while the exact analysis gives -227.25. The approximation provides a rapid way to estimate bounds without computing complex fractions.

CHAPTER 4

Applications of Diodes and Transistors

4.1 Diode Wave-Shaping Circuits

4.1.1 Clipper Circuits

Methodology:

Analysis of Clipper Circuits Clipper circuits limit or clip a portion of the input AC signal without distorting the remaining part. The general steps to analyze a clipper circuit are:

1. **Identify the State of the Diode**: Determine the input voltage condition under which the diode is forward-biased (ON) or reverse-biased (OFF). For an ideal diode it turns ON when $V_{anode} > V_{cathode}$. For a practical diode it turns ON when $V_{anode} > V_{cathode} + V_d$ where V_d is the cut-in voltage.
2. **Equivalent Circuit for ON State**: Replace the forward-biased diode with its equivalent voltage drop V_d (or a short circuit if ideal). Calculate the output voltage V_{out} using Kirchhoff's Voltage Law (KVL).
3. **Equivalent Circuit for OFF State**: Replace the reverse-biased diode with an open circuit. Calculate the output voltage V_{out}.
4. **Plot the Output Waveform**: Graph V_{out} against time or input voltage V_{in} identifying the clipping levels.

Worked Example:

Biased Parallel Positive Clipper A biased parallel positive clipper uses a silicon diode ($V_d = 0.7$ V) connected in series with a DC battery of 4 V. The cathode is connected to the positive terminal of the battery. The input is a sine wave with a peak voltage of 10 V. Determine the output voltage waveform and maximum output voltage.

Solution:

1. **Determine Diode States**: The diode is in parallel with the output. The anode is connected to the input signal V_{in} through a resistor and the cathode is connected to a +4 V reference. The diode turns ON when $V_{in} > 4\text{ V} + 0.7\text{ V} = 4.7\text{ V}$. The diode is OFF when $V_{in} < 4.7$ V.
2. **Calculate V_{out} when Diode is ON**: When $V_{in} > 4.7$ V the diode is forward-biased. The output voltage is clamped to the sum of the battery voltage and diode drop.

$$V_{out} = 4\text{ V} + 0.7\text{ V} = 4.7\text{ V}$$

3. **Calculate V_{out} when Diode is OFF**: When $V_{in} < 4.7$ V the diode is open-circuited. Assuming no load V_{out} follows V_{in}.

$$V_{out} = V_{in}$$

4. **Maximum Output Voltage**: The output strictly follows the input until it reaches 4.7 V. The maximum output voltage is thus 4.7 V. The negative peak will be unclipped at -10 V.

4.1.2 Clamper Circuits

Methodology:

Analysis of Clamper Circuits Clamper circuits add a DC level to an AC signal without altering its shape. To analyze clamper circuits:

1. **Assume Ideal Capacitor**: The capacitor charges instantly to the maximum voltage when the diode is forward-biased and holds this charge when the diode is reverse-biased (large time constant $\tau = RC$).
2. **Identify the Charging Cycle**: Determine which half-cycle of the input signal forward-biases the diode.
3. **Calculate Capacitor Voltage**: Apply KVL during the ON half-cycle to find the voltage across the capacitor V_c.
4. **Calculate Output Voltage**: For the entire signal apply KVL in the output loop: $V_{out} = V_{in} \pm V_c$. The output waveform will be shifted up or down by V_c.

Worked Example:

Negative Clamper Circuit An input square wave alternating between +10 V and −10 V is applied to a negative clamper circuit using an ideal diode. Determine the capacitor voltage and sketch the peak output voltage values.
Solution:

1. **Identify the Charging Cycle**: The negative clamper has the diode cathode pointing towards the output. The diode is forward-biased during the positive half-cycle ($V_{in} = +10$ V).
2. **Calculate Capacitor Voltage**: During the positive half-cycle the diode acts as a short circuit (ideal). The capacitor charges to the peak input voltage. Applying KVL: $V_{in} - V_c = 0 \implies V_c = +10$ V. The capacitor retains this 10 V charge with the positive plate towards the input.
3. **Calculate Output Voltage**: The output voltage is given by $V_{out} = V_{in} - V_c$. During the positive half-cycle: $V_{out} = 10\text{ V} - 10\text{ V} = 0$ V. During the negative half-cycle: $V_{out} = -10\text{ V} - 10\text{ V} = -20$ V.
4. **Conclusion**: The output signal alternates between 0 V and −20 V. The entire waveform has been shifted down by 10 V.

4.2 Voltage Multiplier Circuits

Methodology:

Voltage Multiplier Calculations Voltage multipliers convert lower AC voltage to higher DC voltage using networks of capacitors and diodes.

1. **Voltage Doubler (Half-Wave)**: During the negative half-cycle C_1 charges to V_m (peak input voltage). During the positive half-cycle C_2 charges to $2V_m$. Output Voltage: $V_{out} = 2V_m$ Peak Inverse Voltage (PIV) for each diode: $PIV = 2V_m$.
2. **Voltage Tripler**: Uses three diodes and three capacitors. Output Voltage: $V_{out} = 3V_m$ (taken across C_1 and C_3). PIV for each diode: $PIV = 2V_m$.

Worked Example:

Voltage Doubler Output and PIV A transformer secondary provides an AC voltage of 24 V RMS to a half-wave voltage doubler circuit. Assuming ideal diodes calculate the DC output voltage and the minimum PIV rating required for the diodes.

Solution:

1. **Calculate Peak Input Voltage**:

$$V_m = V_{rms} \times \sqrt{2} = 24 \times 1.414 = 33.94 \text{ V}$$

2. **Calculate DC Output Voltage**: For a voltage doubler the output is twice the peak input voltage.

$$V_{out} = 2 \times V_m = 2 \times 33.94 = 67.88 \text{ V}$$

3. **Calculate Minimum PIV Rating**: The diodes in a voltage doubler must withstand twice the peak input voltage during their reverse-biased state.

$$PIV = 2V_m = 67.88 \text{ V}$$

4.3 Special Purpose Diodes and Optoelectronics

Methodology:

Optoelectronic Design Calculations Optoelectronic devices include indicating LEDs, IR LEDs, OLEDs, AMOLEDs and Seven Segment Displays. While IR LEDs emit non-visible light for communication, OLEDs (Organic LEDs) and AMOLEDs (Active-Matrix OLEDs) use organic compounds for high-contrast displays. Regardless of the technology standard design principles for current and voltage control apply.

1. **LED Series Resistor (for IR LED or Seven Segment)**: To limit the current through an LED a series resistor R_s is used.

$$R_s = \frac{V_s - V_{led}}{I_{led}}$$

where V_s is the supply voltage V_{led} is the forward voltage drop of the LED and I_{led} is the desired forward current.

2. **Opto-coupler Output Current**: An opto-coupler isolates input and output. The Current Transfer Ratio (CTR) defines its efficiency.

$$CTR = \frac{I_C}{I_F} \times 100\%$$

$$I_C = I_F \times \frac{CTR}{100}$$

where I_F is the forward current of the input LED and I_C is the collector current of the output phototransistor.

Worked Example:

Current Limiting Resistor for Seven Segment Display A common-anode Seven Segment Display is driven by a 5 V logic circuit. Each LED segment has a forward voltage drop of 2.2 V and requires 15 mA for optimal brightness. Calculate the required series resistor for each segment.
Solution:

1. **Identify Given Parameters**: $V_s = 5$ V $V_{led} = 2.2$ V $I_{led} = 15$ mA $= 0.015$ A

2. **Calculate Series Resistor**:

$$R_s = \frac{V_s - V_{led}}{I_{led}}$$

$$R_s = \frac{5 - 2.2}{0.015} = \frac{2.8}{0.015} = 186.67 \ \Omega$$

3. **Conclusion**: A standard resistor of 180 Ω or 200 Ω would be selected in practice.

Worked Example:

Optocoupler Current Transfer Ratio An opto-coupler has a guaranteed minimum CTR of 150%. If the input IR LED is driven by a forward current of 10 mA determine the minimum expected collector current at the output phototransistor.

Solution:

1. **Identify Given Parameters**: $I_F = 10$ mA $CTR = 150\%$
2. **Calculate Output Collector Current**:

$$I_C = I_F \times \frac{CTR}{100}$$

$$I_C = 10 \text{ mA} \times \frac{150}{100} = 10 \times 1.5 = 15 \text{ mA}$$

The minimum output current available to drive the next stage will be 15 mA.

4.3.1 Freewheeling and Switching Diodes

Methodology:

Selecting a Freewheeling Diode A freewheeling diode (flyback diode) is placed across an inductive load to dissipate the voltage spike generated when the load is switched off.

1. **Current Rating**: The diode must handle a forward current equal to the steady-state current I_L flowing through the inductor before switching.

$$I_D \geq I_L = \frac{V_s}{R_L}$$

2. **Voltage Rating**: The diode is reverse-biased during normal operation. Its PIV rating must exceed the supply voltage V_s.

$$PIV \geq V_s \times (\text{Safety Factor})$$

Switching diodes are chosen for their ultra-fast reverse recovery time for high-frequency switching.

Worked Example:

Freewheeling Diode Specification A relay coil with a resistance of 120 Ω and an inductance of 50 mH is powered by a 24 V DC supply. Determine the minimum forward current and reverse voltage ratings for a freewheeling diode placed across this coil.

Solution:

1. **Calculate Steady-State Current**: The current through the inductor just before switching off is:

$$I_L = \frac{V_s}{R_L} = \frac{24 \text{ V}}{120 \ \Omega} = 0.2 \text{ A} = 200 \text{ mA}$$

The diode must handle a peak forward current of at least 200 mA.

2. **Determine Reverse Voltage Rating**: During normal operation the diode is reverse-biased by the supply voltage. The reverse voltage rating must be greater than 24 V. Using a safety factor of 2 a rating of 48 V or higher is recommended.

4.4 Transistor Applications

4.4.1 Transistor as Tuned Amplifier

Methodology:

Tuned Amplifier Frequency Calculations A tuned amplifier uses a resonant LC circuit as its load to amplify a specific narrow band of frequencies.

1. **Resonant Frequency**: The frequency at which the LC tank circuit oscillates and provides maximum impedance (and thus maximum voltage gain).

$$f_r = \frac{1}{2\pi\sqrt{LC}}$$

2. **Quality Factor Q**: Determines the sharpness of the resonance.

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}}$$

where R is the effective series resistance of the inductor.

3. **Bandwidth**: The range of frequencies over which the gain is at least 70.7% of its maximum value.

$$BW = \frac{f_r}{Q}$$

Worked Example:

Single Tuned Amplifier Frequency Response A tuned amplifier has an LC tank circuit with an inductance of 100 μH a capacitance of 1000 pF and an effective coil resistance of 10 Ω. Calculate the resonant frequency the quality factor and the bandwidth.
Solution:

1. **Calculate Resonant Frequency**: $L = 100 \times 10^{-6}$ H $C = 1000 \times 10^{-12}$ F

$$f_r = \frac{1}{2\pi\sqrt{100 \times 10^{-6} \times 1000 \times 10^{-12}}} = \frac{1}{2\pi\sqrt{10^{-13}}}$$

$$f_r = \frac{1}{2\pi(3.162 \times 10^{-7})} \approx 503.3 \text{ kHz}$$

2. **Calculate Quality Factor Q**:

$$Q = \frac{1}{10}\sqrt{\frac{100 \times 10^{-6}}{1000 \times 10^{-12}}} = 0.1 \times \sqrt{10^5} = 0.1 \times 316.2 = 31.62$$

3. **Calculate Bandwidth**:

$$BW = \frac{f_r}{Q} = \frac{503.3 \text{ kHz}}{31.62} \approx 15.9 \text{ kHz}$$

4.4.2 Darlington Pair

Methodology:

Darlington Pair Calculations A Darlington pair consists of two bipolar junction transistors connected such that the emitter of the first transistor feeds the base of the second. This configuration provides a very high current gain.

1. **Overall Current Gain**:

$$\beta_{total} = \beta_1 \times \beta_2 + \beta_1 + \beta_2 \approx \beta_1 \times \beta_2$$

2. **Base-Emitter Voltage**:

$$V_{BE(total)} = V_{BE1} + V_{BE2} \approx 1.4 \text{ V (for silicon)}$$

3. **Emitter Current**:

$$I_E \approx I_C = \beta_{total} \times I_B$$

Worked Example:

Current Gain of a Darlington Pair Two identical silicon transistors with $\beta = 100$ are connected in a Darlington configuration. The input base current to the first transistor is 10 μA. Calculate the overall current gain the total emitter current and the base-emitter voltage drop.
Solution:

1. **Calculate Overall Current Gain**:

$$\beta_{total} \approx \beta_1 \times \beta_2 = 100 \times 100 = 10000$$

(Exact formula: $10000 + 100 + 100 = 10200$)

2. **Calculate Total Emitter Current**: Using the approximate total beta:

$$I_E \approx 10000 \times 10 \ \mu\text{A} = 100000 \ \mu\text{A} = 100 \text{ mA}$$

3. **Calculate Base-Emitter Voltage**: Since both are silicon transistors each has a V_{BE} of approx 0.7 V.

$$V_{BE(total)} = 0.7 \text{ V} + 0.7 \text{ V} = 1.4 \text{ V}$$

4.5 Relay Driver Circuits

Methodology:

Relay Driver Circuit Design Transistors and ICs (like TIP122 ULN2003 ULN2803) are used to drive high-current relays from low-current logic signals.

1. **Identify Load Current**: Determine the required relay coil current $I_C = V_{supply}/R_{coil}$.

2. **Determine Base Current for Saturation**:

$$I_B = \frac{I_C}{h_{FE(min)}}$$

Multiply I_B by an overdrive factor (typically 2 to 5) to ensure deep saturation.

3. **Calculate Base Resistor**:

$$R_B = \frac{V_{in} - V_{BE}}{I_{B(sat)}}$$

4. **Using Driver ICs**: ULN2003 (7 channels) and ULN2803 (8 channels) contain Darlington arrays with built-in base resistors and freewheeling diodes. Simply ensure that the per-channel load current does not exceed the IC's specification (usually 500 mA).

Worked Example:

Relay Driver using TIP122 A 12 V relay with a coil resistance of 150 Ω needs to be driven by a microcontroller outputting 5 V. A TIP122 Darlington transistor is chosen ($h_{FE(min)} = 1000$ and $V_{BE(sat)} = 2.5$ V). Calculate

the base resistor required using an overdrive factor of 3.
Solution:

1. **Calculate Relay Coil Current**:

$$I_C = \frac{V_{supply}}{R_{coil}} = \frac{12\text{ V}}{150\ \Omega} = 0.08\text{ A} = 80\text{ mA}$$

2. **Calculate Base Current for Saturation**: The minimum base current needed is:

$$I_{B(min)} = \frac{I_C}{h_{FE(min)}} = \frac{80\text{ mA}}{1000} = 0.08\text{ mA}$$

   Applying the overdrive factor of 3:

$$I_{B(sat)} = 3 \times 0.08\text{ mA} = 0.24\text{ mA}$$

3. **Calculate Base Resistor**:

$$R_B = \frac{V_{in} - V_{BE(sat)}}{I_{B(sat)}} = \frac{5\text{ V} - 2.5\text{ V}}{0.24 \times 10^{-3}\text{ A}}$$

$$R_B = \frac{2.5}{0.00024} = 10416\ \Omega \approx 10\text{ k}\Omega$$

   A standard 10 kΩ resistor can be safely used.

Worked Example:

Current Limit Calculation for ULN2003 A ULN2003 IC is used to drive 4 stepper motor coils simultaneously. If each coil has a resistance of 50 Ω and is driven by a 12 V supply determine if the ULN2003 can handle the load.
Solution:

1. **Calculate Current Per Channel**:

$$I_{channel} = \frac{V_{supply}}{R_{coil}} = \frac{12\text{ V}}{50\ \Omega} = 0.24\text{ A} = 240\text{ mA}$$

2. **Verify Per-Channel Specification**: The ULN2003 has a maximum current rating of 500 mA per channel. Since 240 mA $<$ 500 mA the per-channel load is acceptable.

3. **Verify Total Package Dissipation**: The total current flowing through the IC ground pin is 4×240 mA $= 960$ mA. Assuming a saturation voltage $V_{CE(sat)} = 1.0$ V at this current the total power dissipated is:

$$P_D = 4 \times (I_{channel} \times V_{CE(sat)}) = 4 \times (0.24\text{ A} \times 1.0\text{ V}) = 0.96\text{ W}$$

   The user must ensure that 0.96 W does not exceed the thermal limits of the specific package type. Heat dissipation is near the upper limit so adequate cooling or reducing the duty cycle is advisable.

CHAPTER 5

Regulated Power Supply

5.1 Working of Regulated Power Supply

A regulated power supply converts unregulated alternating current (AC) into a constant direct current (DC). The focus here is on the computational parameters used to evaluate its performance.

Methodology:

Regulated Power Supply Performance Formulas To evaluate a regulated power supply computationally:

1. **Percentage Voltage Regulation (% VR):** Measures the ability to maintain a constant output voltage despite changes in load.
$$\%VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$
Where V_{NL} is the no-load voltage and V_{FL} is the full-load voltage.

2. **Line Regulation:** Measures the change in output voltage for a given change in input line voltage.
$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

3. **Ripple Factor (γ):** Ratio of RMS AC component to DC value at the output.
$$\gamma = \frac{V_{ac(rms)}}{V_{dc}}$$

Worked Example:

Load Regulation Calculation A regulated power supply provides a no-load voltage of 12.2V. When a full load is connected the output drops to 11.9V. Calculate the percentage voltage regulation.
Solution:

1. Identify the given parameters: $V_{NL} = 12.2\text{V}$, $V_{FL} = 11.9\text{V}$.

2. Apply the voltage regulation formula:
$$\%VR = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100$$

3. Substitute the values:
$$\%VR = \frac{12.2 - 11.9}{11.9} \times 100$$
$$\%VR = \frac{0.3}{11.9} \times 100 \approx 2.52\%$$

The percentage voltage regulation is 2.52%.

5.2 Types of Fixed and Variable Voltage Regulators

Integrated Circuit (IC) voltage regulators provide stable DC output. They are classified into fixed and variable regulators.

Methodology:

Voltage Regulator Output Calculations **1. Fixed Voltage Regulators (78XX and 79XX Series):**

- The 78XX series provides a positive fixed voltage equal to XX volts.
- The 79XX series provides a negative fixed voltage equal to -XX volts.
- Power Dissipation: $P_D = (V_{in} - V_{out}) \times I_{load}$

2. Variable Voltage Regulators (LM317 Series):

- The LM317 allows adjustable positive voltage output using an external resistor divider network (R_1 and R_2).
- The output voltage is calculated using:

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2$$

- Typically $V_{ref} = 1.25\text{V}$. Since I_{adj} is very small (around $100\mu\text{A}$) it is often neglected for simplified calculation:

$$V_{out} \approx 1.25\left(1 + \frac{R_2}{R_1}\right)$$

Worked Example:

Variable Regulator Resistor Design Design an LM317 voltage regulator circuit to provide an output of 9V. Assume $R_1 = 240\Omega$ and neglect the adjustment pin current I_{adj}.
Solution:

1. Identify the given parameters: $V_{out} = 9\text{V}$, $R_1 = 240\Omega$, $V_{ref} = 1.25\text{V}$.
2. Write the simplified LM317 voltage formula:

$$V_{out} = 1.25\left(1 + \frac{R_2}{R_1}\right)$$

3. Substitute the known values:

$$9 = 1.25\left(1 + \frac{R_2}{240}\right)$$

4. Solve for the ratio $\frac{R_2}{240}$:

$$\frac{9}{1.25} = 1 + \frac{R_2}{240}$$
$$7.2 = 1 + \frac{R_2}{240}$$
$$6.2 = \frac{R_2}{240}$$

5. Calculate R_2:

$$R_2 = 6.2 \times 240 = 1488\Omega$$

A standard resistor value close to $1.5\text{k}\Omega$ can be used along with a potentiometer to finely tune the 9V output.

5.3 SMPS Applications and Computations

Switched Mode Power Supplies (SMPS) are used in computers and electronic appliances for highly efficient power conversion. Computations usually revolve around duty cycles in switching topologies.

Methodology:

SMPS Converter Topology Formulas An SMPS controls output voltage by rapidly switching an inductor/capacitor network.

1. **Duty Cycle (D):** The ratio of the ON time (T_{on}) to the total switching period (T).

$$D = \frac{T_{on}}{T}$$

2. **Buck Converter (Step-Down):**

$$V_{out} = D \times V_{in}$$

3. **Boost Converter (Step-Up):**

$$V_{out} = \frac{V_{in}}{1 - D}$$

Worked Example:

Buck Converter Output Calculation An SMPS employs a buck converter topology. The input voltage is 24V. The switching frequency is 50kHz and the transistor is turned ON for 8μs per cycle. Calculate the duty cycle and the output voltage.

Solution:

1. Find the total time period (T) from the switching frequency ($f = 50\text{kHz}$):

$$T = \frac{1}{f} = \frac{1}{50 \times 10^3} = 20\mu\text{s}$$

2. Calculate the duty cycle (D) using $T_{on} = 8\mu$s:

$$D = \frac{T_{on}}{T} = \frac{8\mu\text{s}}{20\mu\text{s}} = 0.4$$

3. Calculate the output voltage (V_{out}) for the buck converter:

$$V_{out} = D \times V_{in}$$

$$V_{out} = 0.4 \times 24\text{V} = 9.6\text{V}$$

The duty cycle is 40% and the output voltage is 9.6V.

5.4 UPS (Uninterruptible Power Supply) Battery Sizing

A UPS provides emergency power when the primary mains fail. The most important computational task for a UPS is sizing the battery bank required to support the load.

Methodology:

UPS Battery Sizing Algorithm To compute the required battery capacity in Ampere-hours (Ah) for a given load:

1. **Determine Total Real Power (Watts):**

$$\text{Power (W)} = \text{Apparent Power (VA)} \times \text{Power Factor (pf)}$$

2. **Calculate Total Energy Required (Watt-hours):**

$$\text{Energy (Wh)} = \text{Power (W)} \times \text{Backup Time (Hours)}$$

3. **Calculate Required Battery Capacity (Ah):** Account for the DC system voltage of the UPS and the efficiency of the inverter.

$$\text{Capacity (Ah)} = \frac{\text{Energy (Wh)}}{\text{DC System Voltage} \times \text{Inverter Efficiency}}$$

Worked Example:

UPS Battery Capacity Sizing A 2kVA UPS with a power factor of 0.8 is used to support a load. The system requires a backup time of 3 hours. The UPS operates on a 24V DC battery system and the inverter efficiency is 90%. Calculate the required battery capacity in Ah.
Solution:

1. Calculate the total real power in Watts:

$$\text{Power} = 2000\text{VA} \times 0.8 = 1600\text{W}$$

2. Calculate the total energy required for 3 hours:

$$\text{Energy} = 1600\text{W} \times 3\text{h} = 4800\text{Wh}$$

3. Calculate the battery capacity required, considering the 24V system and 0.9 efficiency:

$$\text{Capacity (Ah)} = \frac{4800}{24 \times 0.9}$$

$$\text{Capacity (Ah)} = \frac{4800}{21.6} \approx 222.2\text{Ah}$$

The system requires a battery capacity of at least 222.2 Ah. Typically two 12V 250Ah batteries in series would be selected for this application.

5.5 Working of Solar Battery Charger Circuits

Solar battery chargers utilize photovoltaic panels to charge battery banks. To properly design the circuit, one must calculate the expected charging currents and times.

Methodology:

Solar Panel Charging Parameters Calculations for solar battery charging assume ideal sunlight conditions to find nominal current and time.

1. **Maximum Charging Current (I_{charge}):**

$$I_{charge} = \frac{\text{Solar Panel Power (W)}}{\text{Battery Charging Voltage (V)}}$$

2. **Estimated Charging Time (T_{charge}):** To account for losses in the charge controller and battery

chemistry an efficiency factor (η, typically 0.8 to 0.85) is used.

$$T_{charge} = \frac{\text{Battery Capacity (Ah)}}{I_{charge} \times \eta}$$

Worked Example:

Solar Panel Charging Time Calculation A 150W solar panel is used to charge a 12V 50Ah lead-acid battery. The charging voltage is regulated to 14.4V by the charge controller. Assuming a system efficiency of 80% calculate the estimated time to fully charge a completely discharged battery.

Solution:

1. Calculate the maximum charging current provided by the panel at the regulation voltage:

$$I_{charge} = \frac{150\text{W}}{14.4\text{V}} \approx 10.42\text{A}$$

2. Calculate the estimated charging time considering 80% efficiency ($\eta = 0.8$):

$$T_{charge} = \frac{50\text{Ah}}{10.42\text{A} \times 0.8}$$

$$T_{charge} = \frac{50}{8.336} \approx 6.0 \text{ hours}$$

Under ideal peak sunlight conditions it will take approximately 6 hours to fully charge the battery.

Formulae

Appendix: Key Formulae

This appendix provides a quick reference to the key formulae and mathematical relationships discussed in this book.

Unit 1: Transistor Biasing and Basics

- **Collector Current (I_C):**
$$I_C = \beta I_B$$
where β is the common-emitter current gain and I_B is the base current.

- **Power Dissipation (P_D):**
$$P_D = V_{CE} I_C$$
where V_{CE} is the collector-emitter voltage and I_C is the collector current.

- **Voltage Divider Bias Base Voltage (V_B):**
$$V_B = V_{CC} \frac{R_2}{R_1 + R_2}$$
where V_{CC} is the supply voltage, and R_1 and R_2 form the base bias voltage divider network.

- **Emitter Current (I_E):**
$$I_E \approx \frac{V_B - 0.7\ \text{V}}{R_E}$$
assuming a standard silicon transistor with a base-emitter voltage drop of approximately 0.7 V.

Unit 2: Amplifiers and Frequency Response

- **AC Emitter Resistance (r'_e):**
$$r'_e = \frac{26\ \text{mV}}{I_E\ (\text{mA})}$$
where I_E is the DC emitter current in milliamperes.

- **Voltage Gain (A_v) of Common-Emitter Amplifier (bypassed R_E):**
$$A_v = -\frac{R_C \parallel R_L}{r'_e} = -\frac{r_c}{r'_e}$$
where $r_c = R_C \parallel R_L$ is the AC load resistance. The negative sign indicates a phase inversion.

- **Gain in Decibels (dB):**
$$A_{v(dB)} = 20 \log_{10}(|A_v|)$$
$$A_{p(dB)} = 10 \log_{10}(A_p)$$
where A_v is the voltage gain and $A_p = \frac{P_{out}}{P_{in}}$ is the power gain.

- **Cascaded Amplifier Gain:**

$$A_{v(total)} = A_{v1} \times A_{v2} \times \cdots \times A_{vn}$$
$$A_{v(total)\text{ dB}} = A_{v1(\text{dB})} + A_{v2(\text{dB})} + \cdots + A_{vn(\text{dB})}$$

- **Bandwidth (BW) and Gain-Bandwidth Product (GBW):**

$$BW = f_H - f_L$$
$$GBW = A_{mid} \times BW$$

where f_H is the upper cutoff frequency, f_L is the lower cutoff frequency, and A_{mid} is the mid-band gain.

- **Miller Capacitance (C_{Miller}):**

$$C_{Miller} = C_{bc}(1 + |A_v|)$$

where C_{bc} is the base-collector junction capacitance.

- **Total Input Capacitance ($C_{in(total)}$):**

$$C_{in(total)} = C_{be} + C_{Miller} + C_{stray(in)}$$

where C_{be} is the base-emitter capacitance and $C_{stray(in)}$ is the input stray capacitance.

- **Upper Cutoff Frequency (f_H):**

$$f_H = \frac{1}{2\pi R_{s(th)} C_{in(total)}}$$

where $R_{s(th)}$ is the Thevenin equivalent source resistance seen by the input capacitance.

- **Lower Cutoff Frequencies (due to coupling and bypass capacitors):**

$$f_{L1} = \frac{1}{2\pi R_{in} C_{c1}} \quad \text{(Input coupling)}$$
$$f_{L2} = \frac{1}{2\pi (R_{out} + R_L) C_{c2}} \quad \text{(Output coupling)}$$
$$f_{LE} = \frac{1}{2\pi R_{eq} C_E} \quad \text{(Emitter bypass)}$$

where R_{in} is input resistance, R_{out} is output resistance, R_{eq} is equivalent resistance at emitter, and C_{c1}, C_{c2}, C_E are the respective capacitors. The dominant lower cutoff frequency f_L is typically the highest of these.

- **Cascaded Cutoff Frequencies (n identical stages):**

$$f_{Ln} = \frac{f_L}{\sqrt{2^{1/n} - 1}}$$
$$f_{Hn} = f_H \times \sqrt{2^{1/n} - 1}$$
$$BW_{total} = f_{Hn} - f_{Ln}$$

where f_L and f_H are the cutoff frequencies of a single stage.

- **Transformer Coupling Reflected Impedance:**

$$R_{in(reflected)} = \left(\frac{N_1}{N_2}\right)^2 R_L = n^2 R_L$$

where $N_1/N_2 = n$ is the turns ratio of the transformer and R_L is the load resistance.

Unit 3: Hybrid Parameters

- **Output Admittance (h_{22} or h_{oe}):**

$$h_{22} = \left.\frac{I_2}{V_2}\right|_{I_1=0}$$

which is the ratio of output current to output voltage with the input open-circuited.

- **Current Gain (A_i):**

$$A_i = \frac{-h_{fe}}{1 + h_{oe}R_L}$$

where h_{fe} is the forward current gain and h_{oe} is the output admittance in common-emitter configuration.

- **Voltage Gain (A_v) in terms of Current Gain:**

$$A_v = \frac{A_i R_L}{Z_i}$$

where Z_i is the input impedance of the amplifier.

Unit 4: Wave Shaping and Multiplier Circuits

- **RC Time Constant (τ):**

$$\tau = RC$$

where R is resistance and C is capacitance.

- **Clipper Critical Voltage ($V_{critical}$):**

$$V_{critical} = V_B + V_k$$

where V_B is the bias voltage and V_k is the diode knee voltage (approx. 0.7 V for silicon).

- **Clamper Capacitor Voltage (V_C):**

$$V_C = \pm V_m + V_{bias}$$

where V_m is the peak input voltage and V_{bias} is an optional DC bias. The output voltage is $V_{out} = V_{in} - V_C$ (or $V_{in} + V_C$ depending on polarity).

- **Voltage Multipliers:**

$$V_{out} = 2V_m \quad \text{(Voltage Doubler)}$$
$$V_{out} = 3V_m \quad \text{(Voltage Tripler)}$$

where V_m is the peak input AC voltage.

Unit 5: Power Supplies and SMPS

- **Power and Energy Calculations:**

$$\text{Real Power (W)} = \text{Apparent Power (VA)} \times \text{Power Factor (pf)}$$
$$\text{Energy (Wh)} = \text{Power (W)} \times \text{Time (Hours)}$$

- **Battery Capacity and Charging:**

$$\text{Capacity (Ah)} = \frac{\text{Energy (Wh)}}{\text{DC Voltage} \times \text{Inverter Efficiency}}$$
$$I_{charge} = \frac{\text{Solar Panel Power (W)}}{\text{Battery Charging Voltage (V)}}$$
$$T_{charge} = \frac{\text{Battery Capacity (Ah)}}{I_{charge} \times \text{Efficiency } (\eta)}$$

- **Voltage Regulation:**

$$\%\text{Voltage Regulation (\% VR)} = \frac{V_{NL} - V_{FL}}{V_{FL}} \times 100\%$$
$$\text{Line Regulation} = \frac{\Delta V_{out}}{\Delta V_{in}}$$

  where V_{NL} is no-load voltage and V_{FL} is full-load voltage.

- **Adjustable Voltage Regulator (e.g., LM317):**

$$V_{out} = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + I_{adj}R_2 \approx 1.25\text{ V}\left(1 + \frac{R_2}{R_1}\right)$$

  where $V_{ref} \approx 1.25$ V and I_{adj} is typically negligible.

- **Switch-Mode Power Supply (SMPS) Basics:**

$$\text{Duty Cycle } (D) = \frac{T_{on}}{T} = T_{on} \times f$$
$$V_{out} = D \times V_{in} \quad \text{(Buck Converter)}$$
$$V_{out} = \frac{V_{in}}{1 - D} \quad \text{(Boost Converter)}$$

- **Ripple Factor (γ):**

$$\gamma = \frac{V_{ac(rms)}}{V_{dc}}$$

  where $V_{ac(rms)}$ is the RMS value of the AC component and V_{dc} is the DC component of the output voltage.